A novel method for sacrificial layer release in MEMS devices fabrication

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During the forming process of the free-standing structure or the functional cavity when releasing the high aspect ratio sacrificial layer, such structures tend to stick to the substrate due to capillary force. This paper describes the application of pull-in length conception as design rules to a novel 'dimpled' method in releasing sacrificial layer. Based on the conception of pull-in length in adhering phenomenon, the fabrication and releasing sacrificial layer methods using micro bumps based on the silicon substrate were presented. According to the thermal isolation performances of one kind of micro electromechanical system device thermal shear stress sensor, the sacrificial layers were validated to be successfully released.

Keywords: sacrificial layer, adhering, pull in length, bump

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1. Introduction

Stiction of microstructures to substrate is one of the main difficulties in surface micromachining due to the inherent proximity (less than a few microns) between structures and its underlying substrate. Many methods are used to resolve this problem. Some materials are chosen for a sacrificial process. Organic-based layers such as photoresist[1,2] and polyimide[3] are used as a sacrificial layer. Dry release technique employing oxygen plasma is used to remove them and eliminates stiction.[3] Electron beam cross-linked polymethyl methacrylate (PMMA) as sacrificial layer is reported.[4] Dendritic material such as hyperbranched polymer has also been reported as a high etch rate dry-release sacrificial layer allowing large-area and high aspect ratio release.[5] Another material polycrystalline silicon is commonly used as sacrificial layers and a dry fluorine-based (SF_6) plasma chemistry[6] or a gaseous phase of CIF_3 or XeF_2[7] are reported as releasing processes.

Surface modifier DDMS ($(CH_3)_2SiCl_2$) for stiction-free polysilicon surfaces is reported.[8] Also OTS ($CH_3(CH_2)_{17}SiCl_3$) and FDTS ($CF_3(CF_2)_7(CH_2)_2SiCl_3$) are reported as self-assembled monolayer coatings for the purpose of adhesion reduction.[9]

Other engineering solutions to stiction problem include surface roughening, super critical point drying, freeze-sublimation, and HF gas phase etching of sacrificial layers have been extensively reviewed.[10,11]

All the methods mentioned above have their own merits, but there also exist limitations of their application. Based on our commonly used structural layer, low pressure chemical vapour deposited silicon nitride, the sacrificial layer materials could not be chosen as photoresist, polyimide or PMMA because of their intolerance of high deposition temperature of silicon nitride. Polycrystalline silicon is also seldom chosen as sacrificial layer, because its low etching selectivity with respect to the structural layer silicon nitride and the silicon substrate. Carbon dioxide super critical point drying, replaced liquid freeze-sublimation, and HF gas phase etching of sacrificial layers have the drawbacks such as high carbon dioxide emission, insecurity of the high pressure and complex machine system, and otherwise HF gas phase etching needs to increase the temperature of the substrate in order to prevent HF gas condensation, which results in its inefficiency.

Even after the devices are released successfully, the devices may come in contact with the substrate in some cases. Anti-stiction support structures such as 'dimple' are commonly seen in releasing sacrificial layer in a micro electromechanical system (MEMS) device, for the distinct merit of keeping structure layer

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from having large-area surface contact with the substrate, and thus of its perdurable anti-stiction, especially in the cases that MEMS devices are used in the moist circumstance or movable structures with electric pad work under the static electric force, or during packaging, transportation, or by various reasons such as dropping, thermal distortion, charge accumulation, or over-range driving during operation. This method is first proposed by Fan[12] and widely used in multi-user MEMS processes (MUMPS) services.[13] It has been widely used for a long time,[14] but in most conventional cases, the dimples are formed on the side of structure layers such as cantilevers or diaphragm. Since smoothness and the intactness of the structural layer are desired for MEMS devices' performances, which would be inversely influenced by those dimples,[14,15] although Sandia SUMMIT (ultra-planar multi-level MEMS technology) process[16,17] has incorporated chemical mechanical planarization (CMP) for years to achieve flat structure layers with dimples, it brings serious requests to characteristics of CMP for achieving high quality structure layers. Additionally for one hand, to polish the structure layer (SiN_x or polysilicon) flatly, it should be deposited thickly according to the dimensions of the dimples[13,18] which adversely increases the stress inside the film; for the other hand, the flat structure layer could be complicatedly achieved by first polishing for forming dimples and then depositing the second layer on it.

Compared with all the methods mentioned above, we present a novel fabrication and releasing sacrificial layer method using obverse micro bumps based on the silicon substrate replacing inverse dimples. This method is based on the conception of pull-in length in adhering phenomena, which is the existent theory[19−21] but has seldom been reported to be applied to 'dimpled' statistical design rules.[12,13] For different structure layer materials, device's dimensions, and replaced liquids after etch, the pull-in lengths are different, which had better been initially determined from statistical design, and modified by experimental results later. Pull-in length is the length of physical contact between a cantilever or a cavity diaphragm and a substrate, when drying after removing the sacrificial layer. Compared with the method of dimples forming on the side of structure layers, micro bumps formed on the substrate does allow for a potentially smoother structural layer, because it brings the least influence to the figuration of the structural layer with sacrificial layer sandwiched, and would potentially improve devices' performances comparably. Additionally the structural layer can become flat due to inside stress release after the sacrificial layer is removed. Even using CMP, we can complete the flatness by easily smoothing the sacrificial layer, not the structural layer, so as to make it intact.

2. Principles and experiments

2.1. Structure design principles

The MEMS devices are usually based on free-standing movable cantilever or functional cavity on the substrate. In some cases, the dimensions of such structure, with high aspect ratio sacrificial layer, impel the adhesion during releasing. Micro bumps formed by silicon isotropic etching on the substrate under the cantilever or inside the cavity, where the distance between each two bump arrays is no more than the pull-in length, will exactly support the cantilever or the diaphragm of the cavity when it tends to adhere to the substrate, because space small than pull-in length will not lead to a physical contact between a cantilever or a cavity diaphragm and a substrate during drying process.

According to the theoretics about pull-in length for doubly clamped beams, and suggesting the influence of stress in the diaphragm is negligible to the pull-in length (see Fig. 1), when the structure is pulled toward the substrate as the liquid vanishes, we find that the pull-in length is[21]

$$L_{\rm pi} = 1.059 \left[\frac{8Ed^2h^3}{\gamma_l(1-\nu^2)(\cos\theta_1+\cos\theta_2)}\right]^{1/4}, \quad (1)$$

where $L_{\rm pi}$ is the pull-in length; E (= 180 GN/m^2) and ν (= 0.27) are the Young's modulus and Poisson's ratio of the diaphragm SiN_x respectively; $\gamma_{\rm l}$ (cyclohexane: 2.762×10^{-4} N/cm) is the liquid facial tension; d (= 2 μm) and h (= 1.5 μm) are the cavity depth and diaphragm thickness respectively, in which the two values are our usual designed values; θ_1, θ_2 are the contact angles, whose values are assumed to be zero, with the presupposition that the liquid is spreading on the surface. Since our last rinsed liquid replacing the sacrificial layer etchant is usually cyclohexane, the pull-in length is calculated to be 147 μm, The distance between two micro bumps should not be smaller than the pull-in length $L_{\rm pi}$. Take the thermal shear stress sensor for example,[22]

the cavity functioned as the adiabatic vacuum chamber, 200 μm×250 μm×1.5 μm in size, which is placed between the silicon nitride diaphragm and silicon substrate. The micro bumps inside the cavity can be designed as line array or point array, which are showed in Figs. 2(a) and 2(b). The exact bump height can be calculated by finite element analysis method simulation, which is related with sacrificial layer geometry, Young's modulus, Poisson's ratio, diaphragm thickness, cavity depth and liquid facial tension. However, the bump height can be designed not more than the maximum value $H_{\rm bump} = d_{\rm cavity} \times L_{\rm pi}/L_{\rm diaphragm}$ (eg. $H_{\rm bump} = 2 \times 147/200 = 1.47$ μm) (see Fig. 2(c)) for convenience of design.

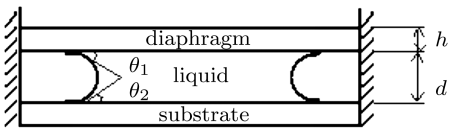


Fig. 1. Schematic diagram of the solid–liquid system.

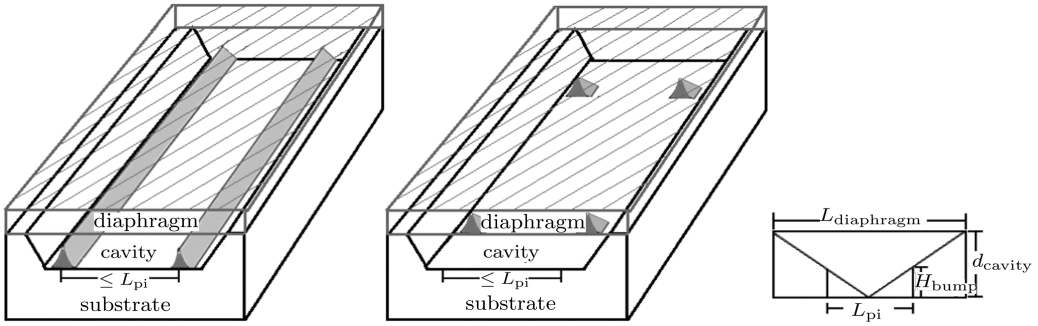


Fig. 2. The cavity with micro bumps (a) line array; (b) point array; (c) maximum bump height.

2.2. Micro bumps fabrication

According to Fig. 3, these micro bumps are formed by silicon isotropic etching in HNA (the system HF, HNO_3 and $HC_2H_3O_2$). The etching rate of silicon in 9 ml 40% HF, 75 ml 67% HNO_3, and 40 ml 99% $HC_2H_3O_2$ at room temperature (15 °C) is 3 μm/min. If the height of the bumps is designed to be about 1 μm, the distance between two close sides of each etching opening can be designed as 2 μm. First etch silicon by inductively coupled plasma (ICP) of just a small depth (for SF_6 ICP about 1–2 min) which is enough and can make it easier for HNA to isotropically etch the silicon substrate facing the ICP etched vertical silicon surface. Then we isotropically etch silicon in the HNA system in 18 s, and that etching fronts meet tangentially and crossly until the bumps form, whose scanning electron microscope (SEM) photo is showed in Fig. 4(a). Lastly the bumps are etched shortly (0.5 min) by reactive ion etch (RIE) for tip surface smoothing,

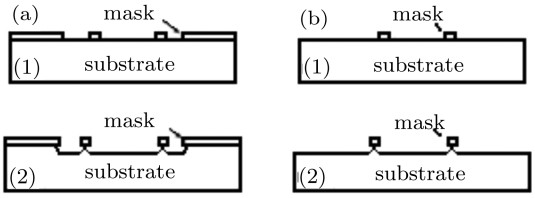


Fig. 3. Fabrication steps of the micro bumps array (a) for the cavity; (b) for the cantilever.

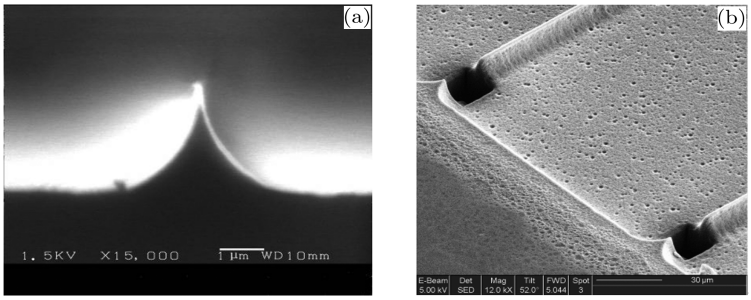


Fig. 4. The SEM and FIB photos of micro bumps (a) sharp shaped bump; (b) round shaped bumps.

whose focus ion beam (FIB) photo is showed in Fig. 4(b). Because it is found that the top of the bump is so sharp to break the cantilever or the cavity diaphragm when they are pulled towards to the substrate due to liquid capillary force. In Fig. 4(b) the holes formed by FIB can make it clear to see the side face of the bumps. The mask described in Fig. 3 can be photoresist for such short time etching, but for longer time etching, the mask should be chosen to withstand the HNA, e.g. nitride silicon.

2.3. Device of microfabrication

Figure 5 shows the schematic top view of a thermal shear stress sensor and side view corresponding to the cross line on the top. The sensing element, 5 μm×150 μm, 0.2 μm thick, is located at the centre of a cavity diaphragm, which is typically 200 μm×250 μm in area and 1.5 μm in thickness. The diaphragm is separated proximately from the bottom of the cavity by 2 μm in distance. Figure 6 illustrates the whole fabrication processes of the thermal shear stress sensor.

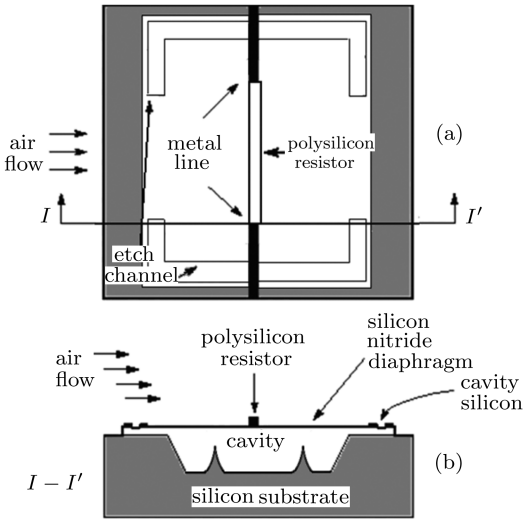


Fig. 5. Schematic top and side views of the thermal shear stress sensor.

The photoresist on bare silicon wafer is lithographically patterned to define the etching opening location and shape of the cavities. The photoresist baking the silicon is etched by ICP for just a small depth (for SF_6 ICP about 1–2 min) and then etched in 9 ml 40% HF, 75 ml 67% HNO_3, and 40 ml 99% $HC_2H_3O_2$ at room temperature (15 °C) in 18 s. The etching time is so short that the photoresist is not oxidated and it can be taken as the mask. Lastly the bumps are etched shortly (0.5 min) by RIE for tip surface smoothing. Micro bumps and cavity are formed. The bumps are about 1 μm in height.

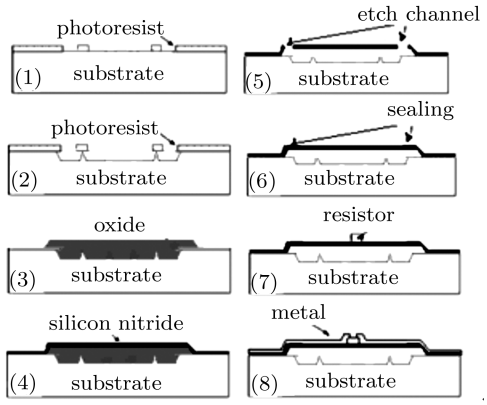


Fig. 6. Fabrication steps of the thermal shear stress sensor.

The third step to the eighth step of the fabrication can be referred to Ref. [23]. The performance of the sensor can be referred to Refs. [23] and [24]. The structure design of the releasing sacrificial layer and its forming control can be referred to parts of Subsections 2.1 and 2.2.

3. Sacrificial layer releasing demonstration

Since the cavity in the fabricated thermal shear stress sensor is sealed around, it is hard to get a 3-D view of the cavity to further validate that the adhering is not happened, but through testing the thermal isolation performances, it can be validated.

The thermal isolation of the cavities is evaluated by using a sensor that is 150 μm long and 5 μm wide with the nominal resistance being 50. Two cases of sensor structures are used for obtaining current-voltage characteristics (Fig. 7). In the first case, the resistor sits on top of a standard sealed cavity, with micro bumps inside. In the second case, the sensor element, identical with the first resistor in geometry and resistance, is deposited directly on top of silicon substrate, which will increase the thermal conduction between the thermal element and the substrate. This is equal to the case that the resistor rests on the diaphragm adhering to the substrate (see Fig. 7(c)).

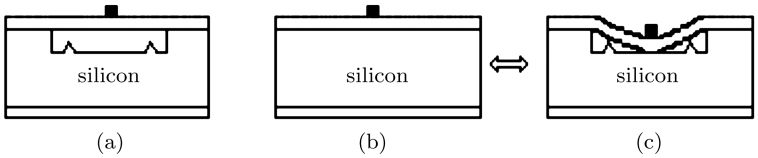


Fig. 7. Schematic diagrams. (a) Titanium-platinum alloy resistor located over a sealed cavity; (b) directly on top of the substrate (equal to the case (c) where diaphragm sticks to the substrate).

Results of I–V measurements by Keithley 4200SCS and Cascade RF-1 conducted in still air are shown in Fig. 8. The first resistor (located on the cavity) has the largest I–V-curve nonlinearity, proving that it experiences the most pronounced temperature rise due to ohmic heating among both structures, and it has the broken down voltage 2.5 V, 2.8 V or more, which causes permanent damage to the resistor. On the other hand, the I–V curve of the resistor directly over the silicon substrate is almost linear, indicating that the thermal conduction to the substrate dominates the heat transfer process and small temperature variation has been created. So it can be found that the thermal isolation for case 1 is better in comparison with that of case 2, and the conclusion can be made that in the case 1 the cavity diaphragm does not adhere to the substrate, which validates the design of the micro bumps.

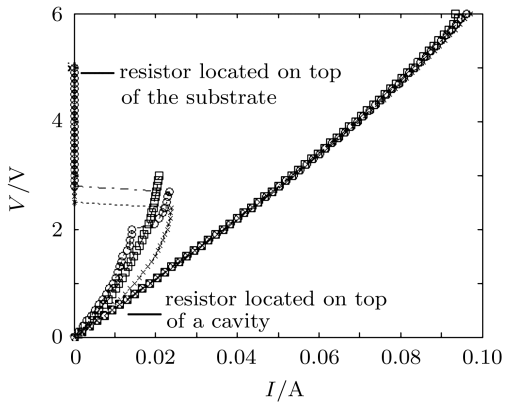


Fig. 8. The I–V characteristics of two resistors in Fig. 10.

4. Comparisons with other releasing methods

Our group has been doing long-term researches on releasing sacrificial layer during fabricating different kinds of MEMS devices. We have found that using anti-stiction supporting structures in suspended cantilevers or cavity diaphragms is an effective method for releasing sacrificial layer in the fabrication of MEMS devices. Such anti-stiction supporting structures include the commonly used inverted dimples and obverse silicon bumps described in this paper. To show the advantages of anti-stiction supporting structures and relative cons of inverted dimples techniques, experiments of releasing sacrificial layer by using super critical point drying ($SCCO_2$), freeze-sublimation, and anti-stiction supporting inverted dimples were done. It is found that $SCCO_2$ can not absolutely ensure the success of the releasing. In the symmetrical cantilever array with no bumps, one cantilever sticks to the substrate (see Fig. 9). Freeze-sublimation can effectively release the suspended cantilevers, which can be seen in Fabry–Perot (F–P) cavity[25] (see Fig. 10), but when this released device is put into moist circumstance, the cavity diaphragm sticks to the substrate (see Fig. 11).

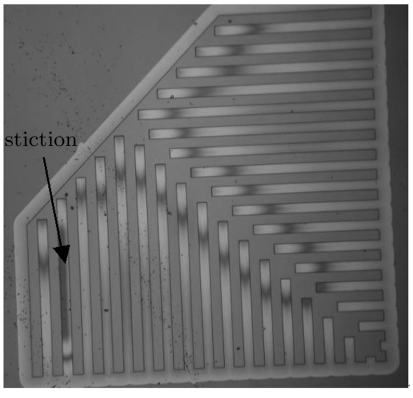


Fig. 9. Cantilevers with no bumps by using $SCCO_2$ meets the stiction with black pattern.

To make direct comparisons between methods of using inverted dimples and obverse silicon bumps, Fig. 12 is our SEM photo of wet released focal pixel array (FPA)[26,27] not by using $SCCO_2$ or freeze-sublimation techniques, in which the SiN_x cantilever is not flat with dimples below. If we use CMP to get a flat SiN_x layer, the thickness of the film should be thicker according to the dimensions of the dimples, but the film is thicker, the stress inside film is larger. Even in some kind of MEMS devices, the figurations of

suspended cantilevers or cavity diaphragms will essentially influence performances of the devices. Take the F–P cavity for example, the flatness of the top mirror directly influences its optical characteristics. To compare, micro bumps formed on the substrate does allow for a potential smoother structural layer, because the flatness can be completed by easily polishing the sacrificial layer, not the structural layer, so as to make it intact.

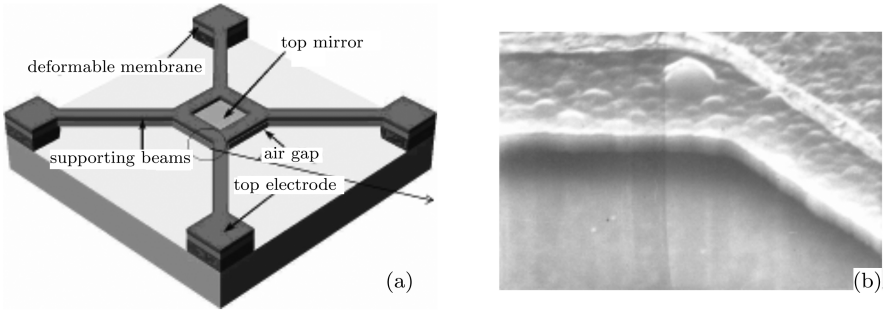


Fig. 10. The F–P cavity with no bumps using freeze-sublimation techniques. (a) F–P cavity structure; (b) photo of successful release.

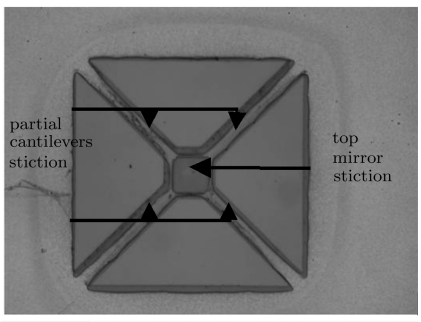


Fig. 11. Released F–P cavity meets stiction in moist circumstance.

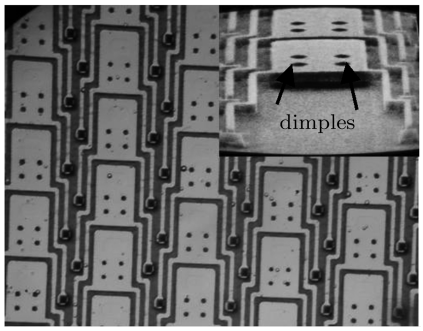


Fig. 12. The SEM photo of wet released FPA with dimples on side of the cantilevers.

5. Conclusions

The thermal isolation performances tested in Section 3 validate the cavity diaphragm does not adhere to the substrate, which thereby validates the design of micro bumps point array inside the cavity described in Fig. 2(b). It can be deduced that micro bumps line array could also be applied to the releasing sacrificial layer based on the discussion in this paper.

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