Effect of interface roughness on the carrier transport in germanium MOSFETs investigated by Monte Carlo method*

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Interface roughness strongly influences the performance of germanium metal–organic–semiconductor field effect transistors (MOSFETs). In this paper, a 2D full-band Monte Carlo simulator is used to study the impact of interface roughness scattering on electron and hole transport properties in long- and short- channel Ge MOSFETs inversion layers. The carrier effective mobility in the channel of Ge MOSFETs and the in non-equilibrium transport properties are investigated. Results show that both electron and hole mobility are strongly influenced by interface roughness scattering. The output curves for 50 nm channel-length double gate n and p Ge MOSFET show that the drive currents of n- and p-Ge MOSFETs have significant improvement compared with that of Si n- and p-MOSFETs with smooth interface between channel and gate dielectric. The 82% and 96% drive current enhancement are obtained for the n- and p-MOSFETs with the completely smooth interface. However, the enhancement decreases sharply with the increase of interface roughness. With the very rough interface, the drive currents of Ge MOSFETs are even less than that of Si MOSFETs. Moreover, the significant velocity overshoot also has been found in Ge MOSFETs.

Keywords: carrier transport, interface scattering, germanium MOSFETs, Monte Carlo
PACC: 7360J, 7210, 7340Q

1. Introduction

Due to its higher intrinsic mobility, germanium (Ge) is considered as a promising alternative to Silicon (Si).[1] Many experiments have reported significantly performances improvements of Ge and Ge-on-insulator MOSFETs especially for p-MOSFET.[2−11] Moreover, as pointed out by the experiments, Ge MOSFETs suffer from interface roughness and high defect densities which can substantially affect the carrier transports in the inversion layer. The interface roughness strongly influenced the performance of germanium MOSFETs.[12] Thus it is becomes important in investigation on the impact of the interface roughness scattering on the carrier mobility and the drive current of Ge MOSFETs in detail. In Ref. [13]–[15], sub-100 nm Ge MOSFETs devices have been investigated using some theoretical approaches within the non-equilibrium Green's function formalism and their performance benefits over Si n-MOSFETs were reported. However, most of these studies were based on the ballistic simulation and the constant effective mass approximation without scattering, which is still very important for carrier transport in the sub 100 nm MOSFETs. Bahniman Ghosh *et al.*[16] reported a Monte Carlo study of Ge n- and p-MOSFETs. Given the same value of the interface roughness scattering model parameters, they compared the carrier transport characteristics in Ge and Si channels. However, it was not well considered how the carrier transport properties can be affected by the interface roughness scattering.

In this paper, the impact of interface roughness scattering on electron and hole transport properties in long and short channel-length Ge MOSFETs inversion layers is carefully studied by a two-dimensional (2D) full-band Monte Carlo simulator.[17,18] The effect of the interface scattering on the carrier mobility is investigated by single-particle full-band Monte Carlo simulation for saving computation time, while the effect of the interface scattering on the drive current is studied by ensemble Monte Carlo simulation for the good self-consistent between Poisson equation and Boltzmann transport equation. The paper is or-

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ganized as follows. To begin with, the full-band Monte Carlo device simulator and scattering models will be introduced in detail. Then, the effect of the interface scattering on the carrier effective mobility in long channel-length Ge MOSFETs inversion layer is analysed. Furthermore, we analyse the impact of the interface roughness on the non-equilibrium transport in 50 nm channel-length double-gate Ge MOSFETs. Unlike Si there is not a universal mobility for Ge, so the Si universal mobility is used as a reference in our discussion. Finally, we will draw a conclusion for the whole paper.

2. Monte Carlo simulation

A 2D full-band Monte Carlo simulator[17,18] is used in this work. The full band structure of Ge is calculated using the non-local empirical pseudo-potential approach including spin–orbit interactions[19] and is stored as a form which can be easily used in simulation. Four conduction bands and three valence bands are involved for Ge. The detail of scattering mechanisms and the deformation potentials of Ge have been described in Refs. [20]–[22].

Two types of Monte Carlo algorithms including ensemble and single-particle Monte Carlo methods are employed. The ensemble Monte Carlo algorithm is a self-consistent method by means of solving the Poisson equation and Boltzmann equation. Accordingly, the evolution of an ensemble of particles is simulated starting from a given initial condition. The physical characteristics are obtained in terms of ensemble averages, giving rise to the name 'ensemble Monte Carlo'.[22] In single-particle Monte Carlo algorithm, a single particle is injected from some contact and propagates in a frozen electric field (initially taken from the drift diffusion (DD) or hydrodynamic(HD) device simulation), until it is absorbed at a contact. Then the next particle is simulated, and so on.

The carriers transport in bulk Ge is simulated by single-particle full-band Monte Carlo method and compared with the experimental data[23] as shown in Fig. 1 to verify the simulator and the physical models as well as the parameters of germanium. Our Monte Carlo simulation matches the experimental data without adjusting any fitting parameters.

Since the interface roughness scattering is a key issue when carriers transport through the channel in the inversion layer, accurate interface roughness scattering model and suitable value of adjustable parameters are in great need for accurate Monte Carlo simulation.

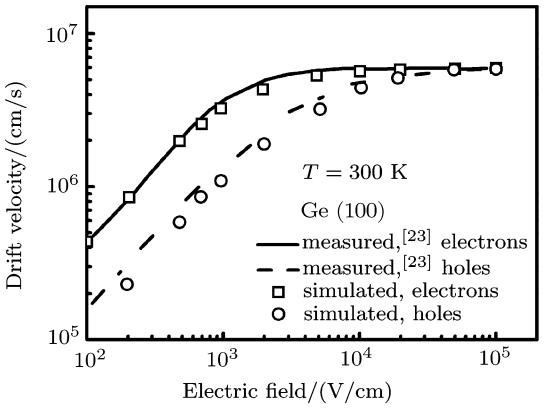


Fig. 1. Drift velocity of electron and hole in bulk Ge as a function of electric field.

We have implemented a compact interface roughness scattering model for full-band Monte Carlo simulation in our device simulator. The interface roughness scattering rate is modeled, similar to Ref. [24] and is given by

$$S_{\rm sr}(E_{\rm eff}) = 2\pi\frac{m^* e^2}{\hbar^3}\left(\frac{\varepsilon_{\rm ge}}{\varepsilon_{\rm ge}+\varepsilon_{\rm ox}}\right)\Delta^2 L^2 E_{\rm eff}^2, \qquad (1)$$

where Δ is the root mean square (rms) of the fluctuations amplitude and L is their correlation length (roughly the distance between fluctuations). The effective carrier mass and charge are denoted with m^* and e. $E_{\rm eff}$ is the effective field which can be calculated by various methods.[25,26] In this work, we evaluate the effective field as follows:[27]

$$E_{\rm eff} = \frac{\int E(z)n(z){\rm d}z}{\int n(z){\rm d}z}, \qquad (2)$$

where z direction is the transverse field direction, $n(z)$ is the inversion charge concentration and $E(z)$ is the local electric field. The average drift velocity is calculated for several values of the longitudinal electric field, and the low-field mobility is extracted from the relation of average drift velocity to longitudinal electric field.

Figure 2 shows simulated carriers mobility (symbols) versus the effective field in Si MOSFETs. The experimental mobility curves (lines)[25] are also plotted in the figure. From this figure, it can be seen that $\Delta = 0.13$ and 0.1 nm for electron and hole respectively can reproduce the universal experimental electron and hole mobility curve. So the interface roughness scattering model can be used in Ge MOSFETs by adjusting the parameters. In the following simulations, we will adjust the parameter Δ to investigate the impact

of interface roughness on carrier transport characteristics.

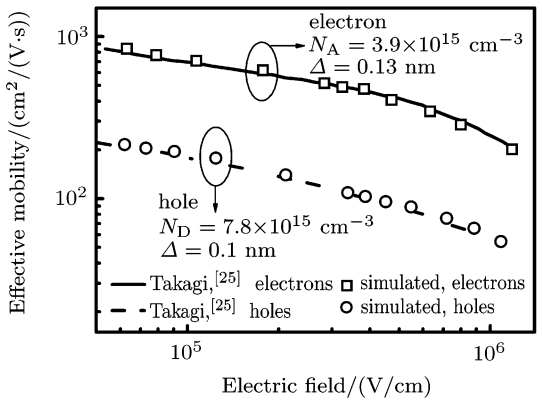


Fig. 2. Electron and hole mobility curves versus effective field in Si MOSFETs.

3. Carrier effective mobility

Compared with bulk Si, the low-field electron mobility in bulk Ge is doubled, and the hole mobility is four times larger. However, carrier effective mobility in the inversion layer of Ge MOSFETs is degraded compared to the bulk by interface roughness scattering. It is not completely clear how this advantage in bulk material could be kept in the inversion layer. In this section, the impact of interface roughness on carrier effective mobility will be investigated carefully. Figures 3 and 4 show the electron and hole effective mobility curves versus effective field for different Δ of interface roughness respectively. The Δ is varying from 0.0 (which means smooth interface) to 0.7 nm. Low channel impurity concentration (1×10^{15} cm^{-3}) is selected, the coulomb scattering can be neglected. It can be seen obviously that with smooth interface, both electron and hole effective mobilities are not sensitive to the effective field. While increasing the interface roughness, electron and hole effective mobilities under low effective field decrease very slightly because of the low interface roughness scattering rate. Under high effective field, electron and hole effective mobilities decrease very sharply since interface roughness scattering dominates the carrier transport property. Compared with the Si universal curves, with the smooth interface, electron and hole effective mobilities in Ge MOSFETs are over 10 and 20 times than those of Si. With the increase of interface roughness, this increase reduces. With very rough interface roughness, electron and hole effective mobilities become close to that of Si. In the worst case, electron and hole effective mobilities are smaller than those of Si at high effective field.

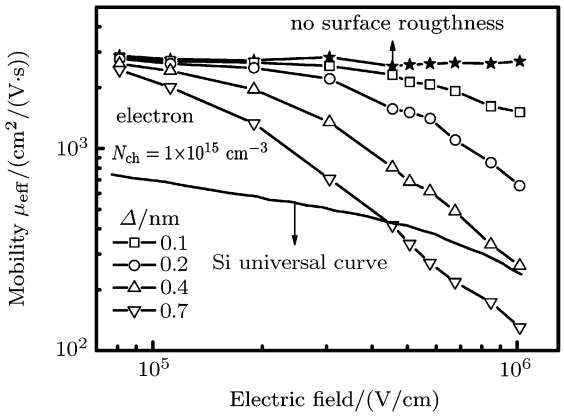


Fig. 3. Ge electron mobility curves versus effective field for different Δ of interface roughness.

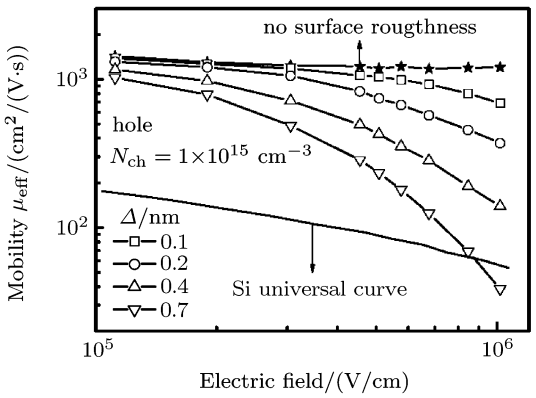


Fig. 4. Ge hole mobility curves versus effective field for different Δ of interface roughness.

4. Non-equilibrium transport

As MOSFETs are scaling into the sub 0.1 μm regime, carrier non-equilibrium transport such as velocity overshoot becomes more and more obvious, conventional simulation method (e.g. DD, HD) cannot accurately describe the characteristic of carrier transport. Here we use ensemble Monte Carlo simulation to investigate the impact of interface roughness on non-equilibrium transport in detail.

The 50 nm channel length double-gate n- and p-Ge MOSFET (which is shown in Fig. 5) are simulated. The device has a 1nm effective gate oxide thickness (EOT), with {100} interfaces and ⟨100⟩ transport directions. The source and drain doping is 5×10^{19} cm^{-3} which is close to the fabrication. The substrate doping is 1×10^{15} cm^{-3}, thus we can neglect the effect of Coulomb scattering in the channel. The germanium film thickness (T_{Ge}) is 20 nm which is less than 1/2 channel length (L_g), shoat channel effect (SCE) can be

well controlled. The source and drain extension distance (L_{SD}) is 15 nm for small parasitical resistance.

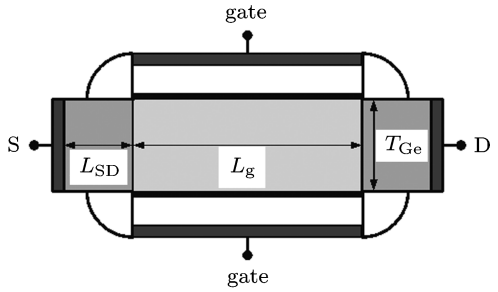


Fig. 5. Schematic cross-sectional view of 50 nm channel length double-gate Ge MOSFET structure.

Figure 6 shows the output characteristics of n- and p-double-gate Ge MOSFETs at $|V_{GS} - V_T| = 1$ V for different Δ of interface roughness. Si MOSFETs are also simulated for a comparation, with the Δ of Si equal to 0.13 and 0.1 nm for electron and hole respectively. From Fig. 6, it can be seen that the drain current is strongly related to the interface condition. For smooth interface, the drain current attains the maximum, which is about 75 and 50 A/cm for n- and p-MOSFETs respectively. With the increase of interface roughness, the drain current decreases rapidly. With very rough interface(Δ = 0.7 nm), Ge n- and p-MOSFETs have smaller drain current than the Si n- and p-MOSFETs.

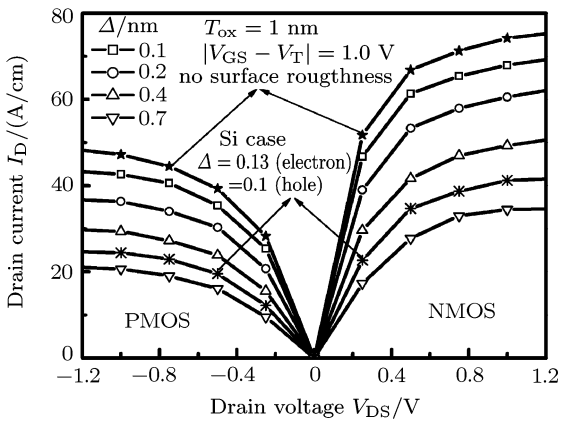


Fig. 6. Output characteristics of n- and p-double-gate Ge MOSFETs for different Δ of interface roughness.

In order to investigate how interface roughness affects the output characteristics in 50 nm channel-length double-gate Ge MOSFETs, we should pay more attention to the carrier transport in the channel. Figures 7 and 8 show respectively the average electron and hole velocity profiles from source to drain at $|V_{GS} - V_T| = |V_{DS}| = 1$ V. The dashed lines denote the saturation velocity in Ge material. It is obvious that there exists velocity overshoot almost in the channels both for electron and hole. The saturation velocity in Ge is smaller than in Si, however we can see that average carrier velocity in Ge channel may be larger than in Si channel due to the strong velocity overshoot. The results also show that interface roughness affects the velocity overshoot strongly.

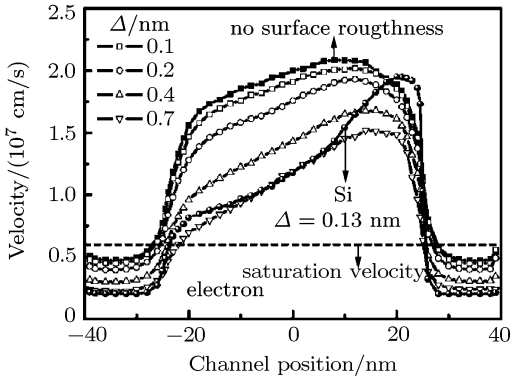


Fig. 7. Average electron velocity profile from source to drain in 50 nm gate-length double gate Ge n-MOSFETs, $|V_{GS} - V_T| = |V_{DS}| = 1$ V.

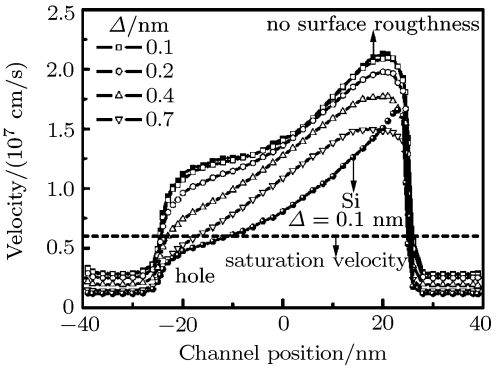


Fig. 8. Average hole velocity profile from source to drain in 50 nm gate-length double-gate Ge p-MOSFETs, $|V_{GS} - V_T| = |V_{DS}| = 1$ V.

Interface roughness affects the velocity profile in all the channels. With the increase of Δ of interface roughness, source-side and peak velocities both decrease as shown in Figs. 9 and 10. However, source-side velocity shows a stronger relation with interface roughness than peak velocity. Both electron and hole source-side velocities have about 60% decrease while Δ of interface roughness changes from 0 to 0.7 nm. And the decrease of electron and hole peak velocities is about 30%. It indicates that strong velocity overshoot in the drain side reduces the effect of interface roughness from another point of view. For comparison, the average electron velocity profile in Si MOSFETs is also shown in Figs. 7 and 8. Electron and hole

average velocities of Ge MOSFETs near the source side are higher than those of Si MOSFETs even the interface is very rough.

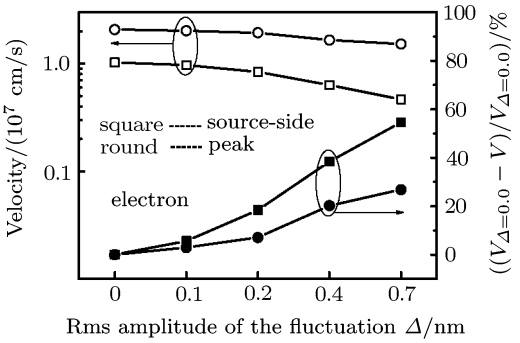


Fig. 9. Electron source-side and peak velocities versus Δ of interface roughness, $|V_{GS} - V_T| = |V_{DS}| = 1$ V.

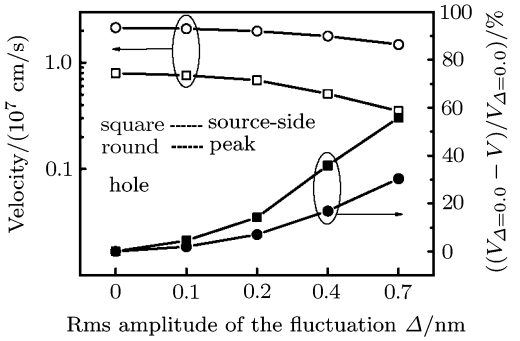


Fig. 10. Hole source-side and peak velocities versus Δ of interface roughness, $|V_{GS} - V_T| = |V_{DS}| = 1$ V.

As Lundstrom and Ren[1] has pointed out that the source-side velocity is decisive for the on-current whereas the velocity overshoot peak in the drain-side of the channel is of minor importance; in order to study how interface roughness affects the drive current, it is necessary to make an inspection of source-side velocity carefully. Figure 11 shows the source-side and peak velocity of electron and hole versus the drain current for different Δ of interface roughness respectively. The squares are the source-side velocities, while the circles are the peak velocities. It is clearly shown that the drain current is in proportion to the source-side velocity, and the drain current tends to zero when source-side velocity is zero.

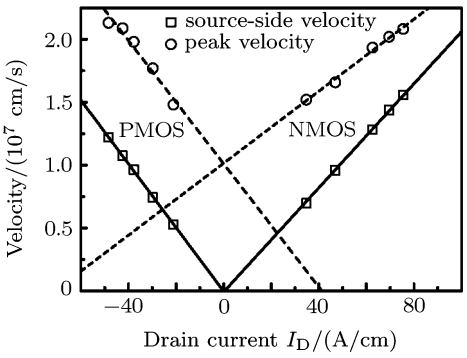


Fig. 11. The variation of source-side and peak velocities with drain current in Ge MOSFETs.

5. Conclusion

In this paper, the impact of interface roughness scattering on electron and hole transport properties in Ge MOSFETs inversion layers is carefully studied using a 2D full-band Monte Carlo simulator. Both electron and hole mobilities are strongly controlled by interface roughness scattering in long channel Ge MOSFETs. With a very rough interface, the drive current of Ge MOSFETs is even less than that of Si MOSFETs. The non-equilibrium transport is obvious in 50 nm Ge MOSFETs. The drive current is related to the increased carrier velocity in source side which supports the conclusion by Lundstrom and Ren[1] that the source-side velocity is decisive for the on-current whereas the velocity overshoot peak in the drain-side of the channel is of minor importance.

References

[1] Lundstrom M and Ren Z B 2002 *IEEE Trans. Electron Device* **49** 133
[2] Shang H L, Okorn-Schmidt H, Chan K K, Copel M, Ott J A, Kozlowski P M, Steen S E, Cordes S A, Wong H S P, Jones E C and Haensch W E 2002 *IEDM Tech. Dig.* San Francisco, CA, USA 8–11 Dec. 2002 p441
[3] Chui C O, Kim H, Chi D, Triplett B B, Mcintyre P C and Saraswat K C 2002 *IEDM Tech. Dig.* San Francisco, CA, USA 8–11 Dec. 2002 p437
[4] Whang S J, Lee S J, Gao F, Wu N, Zhu C X, Pan J S, Tang L J and Kwong D L 2004 *IEDM Tech. Dig.* San Francisco, CA, USA 13–15 Dec. 2004 p307
[5] Suzanne C Martin, Lorin M Hitt and James J Rosenberg 1989 *IEEE Electron Device Lett.* **10** 325
[6] Wu N, Zhang Q, Balasubramanian N, Chan D S H and Zhu C 2007 *IEEE Trans. Electron Devices* **54** 733
[7] Zhang Q, Huang J, Wu N, Chen G, Hong M, Bera L K and Zhu C 2006 *IEEE Electron Device Lett.* **27** 728
[8] Yu H Y, Ishibashi M, Park J H, Kobayashi M and Saraswat K C 2009 *IEEE Electron Device Lett.* **30** 675
[9] Romanjek K, Hutin L, Royer C L, Pouydebasque A, Jaud M A, Tabone C, Augendre E, Sanchez L, Hartmann J M, Grampeix H, Mazzocchi V, Soliveres S, Truche R, Clavelier L, Scheiblin P, Garros X, Reimbold G, Vinet

M, Boulanger F and Deleonibus S 2009 *Solid-State Electronics* **53** 723
[10] Kuzum D, Pethe A J, Krishnamohan T and Saraswat K C 2009 *IEEE Trans. Electron Devices* **56** 648
[11] Cheng C C, Chien C H, Luo G L, Lin C L, Chen H S, Liu J C, Kei C C, Hsiao C N and Chang C Y 2009 *IEEE Trans. Electron Devices* **56** 1681
[12] Toriumi A, Tabata T, Lee C H, Nishimura T, Kita K and Nagashio K 2009 *Microelectronic Engineering* **86** 1571
[13] Low T, Hou Y T, Li M F, Zhu C, Chin A, Samudra G, Chan L and Kwong D L 2003 *IEDM Tech. Dig.* Washington DC, USA 8–10 Dec. 2003 p691
[14] Rahman A, Ghosh A and Lundstrom M Washington DC, USA 8–10 Dec. 2003 *IEDM Tech Dig.* 2003 p471
[15] Laux S E 2004 *IEDM Tech Dig.* San Francisco, CA, USA 13–15 Dec. 2004 p135
[16] Ghosh B, Wang X, Fan X F, Register L F and Banerjee S K 2005 *IEEE Trans. Electron Devices* **52** 547
[17] Du G, Liu X Y, Xia Z L, Kang J F, Wang Y, Han R Q, Yu H Y and Kwong D L 2005 *IEEE Trans. Electron Devices* **52** 2258
[18] Du G, Liu X Y, L. Sun and Han R Q 2006 *Chin. Phys.* **15** 177
[19] Chelikowsky J R and Cohen M L 1976 *Phys. Rev.* B **14** 556
[20] Kunikiyo T, Takenaka M, Kamakura Y, Yamaji M, Morifuji M, Taniguchi K and Hamaguchi C 1994 *J. Appl. Phys.* **75** 297
[21] Thoma R, Peifer H J, Engl W L, Quade W, Brunetti R and Jacoboni C 1991 *J. Appl. Phys.* **69** 2300
[22] Jacoboni C and Reggiani L 1983 *Rev. Mod. Phys* **55** 645
[23] Sze S M 1981 *Physics of Semiconductor Devices* (2nd ed) (New York: Wiley) p46
[24] Grgee D, Jungemann C, Nguyen C D, Neinhus B and Meinerzhagen B 2004 *7th Int. Conf. on Solid-State and Integrated Circuits Technology Proceedings* Beijing, October 18–21, 2004 p991
[25] Takagi S, Toriumi A, Iwase M and Tango H 1994 *IEEE Trans. Electron Devices* **41** 2357
[26] Gamiz F, Lopez-Villanueva J A, Banqueri J, Carceller J E and Cartujo P 1995 *IEEE Trans. Electron Devices* **42** 258
[27] Gamiz F, Lopez-Villanueva J A, Roldan J B, Carceller J E and Cartujo P 1998 *IEEE Trans. Electron Devices* **45** 1122