Comparative studies of Ge and Si p-channel metal–oxide–semiconductor field-effect-transistors with HfSiON dielectric and TaN metal gate*

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Ge and Si p-channel metal–oxide–semiconductor field-effect-transistors (p-MOSFETs) with hafnium silicon oxynitride (HfSiON) gate dielectric and tantalum nitride (TaN) metal gate are fabricated. Self-isolated ring-type transistor structures with two masks are employed. W/TaN metal stacks are used as gate electrode and shadow masks of source/drain implantation separately. Capacitance–voltage curve hysteresis of Ge metal–oxide–semiconductor (MOS) capacitors may be caused by charge trapping centres in GeO_x ($1 < x < 2$). Effective hole mobilities of Ge and Si transistors are extracted by using a channel conductance method. The peak hole mobilities of Si and Ge transistors are 33.4 $cm^2/(V{\cdot}s)$ and 81.0 $cm^2/(V{\cdot}s)$, respectively. Ge transistor has a hole mobility 2.4 times higher than that of Si control sample.

Keywords: Ge substrate, transistor, HfSiON, hole mobility
PACC: 7340Q, 7325

1. Introduction

Historically, the first transistor was made on Ge,[1] but the low thermal stability and water solubility of Ge oxides made people choose Si because of the superior physical and electrical properties of silicon dioxide. When the feature size of metal–oxide–semiconductor field-effect-transistors (MOSFETs) is scaled down to sub-50 nm, the Si dioxide becomes so thin that direct tunneling results in high gate leakage current.[2] To solve this problem, high dielectric constant (high-K) materials are widely studied to replace Si dioxide.[3] Using high-K material as gate dielectric, Ge has received much attention again, as Ge has a large intrinsic carrier mobility. Ge metal–oxide–semiconductor (MOS) capacitors with HfO_2 high-K dielectric were reported.[4]

In the present paper, Ge and Si p-MOSFETs with hafnium silicon oxynitride (HfSiON) gate dielectric and tantalum nitride (TaN) metal gate are fabricated and investigated. The peak hole mobilities of Si and Ge transistors are 33.4 $cm^2/(V{\cdot}s)$ and 81.0 $cm^2/(V{\cdot}s)$, respectively. The hole mobility in Ge transistors is 2.4 times higher than that of Si transistors.

2. Device design and process development

To simplify the fabrication process, self-isolated ring-type transistor structures are employed.[5] The top view of a ring-type transistor structure is shown in Fig. 1.

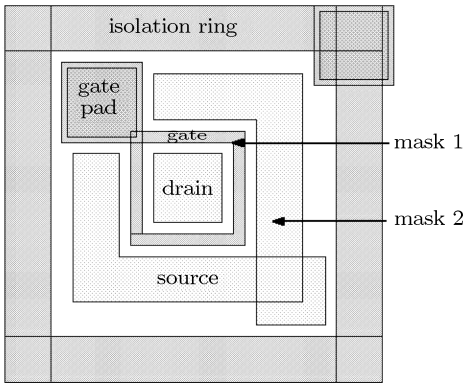


Fig. 1. The top view of a ring-type transistor structure.

Mask 1 is the gate and isolation ring pattern mask, while mask 2 is the source and drain contact pattern mask. Self-isolation can be achieved by grounding the source potential. The isolation ring on mask 1 is used to ensure, during self-aligned

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source/drain (S/D) implantation, that the source region in each ring MOSFET on the wafer is contained within the isolation ring and discontinuous with the source regions of its neighbouring MOSFETs.

Device operation of a ring type MOSFET is the same as that of a conventional rectangular MOSFET. However, the definition of the gate width is not straightforward. By applying the charge sheet model on a long-channel ring-type MOSFET,[6] the effective channel width $W_{\rm eff}$, could be extracted and shown as follows:

$$W_{\rm eff} = \frac{8L}{\ln\left(1+\frac{2L}{W_{\rm in}}\right)}, \quad (1)$$

where L is the gate length, and $W_{\rm in}$ is the inner width of gate ring. Gate length was drawn from 2 μm to 100 μm in our mask. Considering that the gate contact pad was drawn in the source region, the real gate width W is smaller than $W_{\rm eff}$ and can be written as follows:

$$W = W_{\rm eff} - \Delta W, \quad (2)$$

where ΔW is gate contact pad induced width correction parameter.

Ge p-MOSFETs were fabricated on (100) oriented n-type Ge substrates (Sb doped, with a resistivity of about 0.1–0.3 Ω·cm). The complete process flow was shown in Fig. 2. All the anneal treatments were performed in N_2 atmosphere. Ge wafers were cleaned by using cyclic H_2O_2 oxidation and HCl etch method.[7] HfSiON dielectric was then deposited by RF magnetron reactive sputtering.[8] Post deposition anneal (PDA) was performed at 400 °C for 1 min. TaN and W were sequentially sputter-deposited and patterned by using lift-off technique. After gate patterning, 4×10^{15} cm^{-2} BF_2 was implanted at 40 keV, followed by 400 °C, 40 min S/D dopant activation anneal (DAA) in a furnace. About 2000 Å (1 Å=0.1 nm) SiO_2 was deposited. S/D contact etching and contact metallization were combined into a single lithography step. After SiO_2 and HfSiON dielectric etching, Ti and Al was sequentially deposited on the wafers and then patterned by using lift-off technique. Finally, metallization anneal was performed at 300 °C for 20 min in the furnace.

Si control devices were fabricated by using the same masks for comparison. After cleaning Si wafer, native oxide was stripped in dilute HF (with IPA added) solution. PDA and DAA were performed at 700 °C for 60 s and 900 °C for 30 s, respectively. Finally, metallization anneal was performed at 400 °C for 40 min. All the other processes were the same as that for Ge transistors.

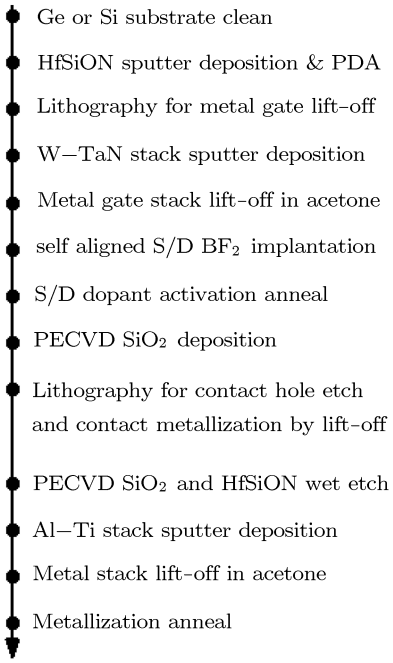


Fig. 2. Process flow of Ge and Si p-MOSFETs.

Capacitance–voltage (C–V) and current–voltage (I–V) curves were measured by using MDC 590 and Keithley 4200, respectively. Capacitance equivalent thickness ($T_{\rm ox}$) was extracted from the accumulation capacitance which was measured at 1 MHz.

TaN, a refractory and non-reactive metal nitride, was chosen as a gate electrode material. W was deposited on the top of TaN to prevent its oxidation during subsequent anneal steps. S/D regions were then formed by self-aligned BF_2 implantation. The energy of B atom in BF_2 with an energy of 40 keV was 9 keV. The projected range ($R_{\rm p}$) and standard deviation (σ) of B in W with energy of 9 keV were approximately 100 Å and 150 Å, respectively, while those of B in Ta were about 110 Å and 160 Å, respectively.[9] The atomic density of TaN is denser than that of Ta, so the projected range and standard deviation of B in TaN is smaller than that in Ta.[9,10] If the film thickness equals $R_{\rm p}+5\sigma$, only less than $1/10^6$ B atom can penetrate the film.[10] The thicknesses of W and TaN deposited were both 1000 Å, which were thicker than $R_{\rm p}+5\sigma$ of B in them. Figure 3 shows the C–V curves of Si MOS capacitors (with and without BF_2 implantations) with fully processed flow. After DAA, B atoms diffused laterally and the capacitor area was slightly reduced. The accumulation capacitance with

BF_2 implantation was smaller than that without BF_2 implantation, which may be caused by capacitor area reduction. The flat band voltages of the two cases were nearly the same, indicating that B atoms could not penetrate W/TaN metal stack after DAA.

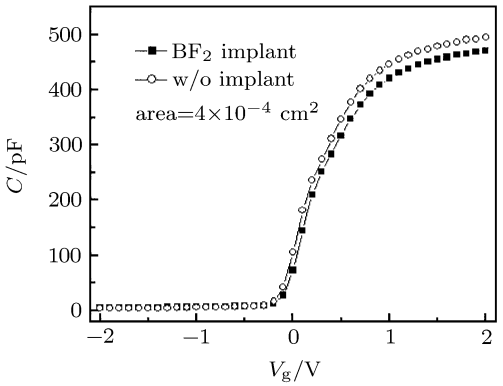


Fig. 3. C–V characteristics of Si MOS capacitors with fully processed flow. In w/o implant case, BF_2 implantation was omitted.

It is well known that HF can etch Si–O bond and HCl can etch Hf–O bond. In our experiment, dilute HF and HCl mixing solution was used to etch HfSiON dielectric. Si2p, Hf4f and N1s XPS spectra are shown in Fig. 4. HfSiON dielectric deposited on Si substrate was etched in the mixing solution for 1 min. The binding energy was calibrated with C1s=284.5 eV. As shown in Fig. 4, Hf4f peaks were not detected, indicating that HfSiON dielectric was etched completely. N1s peak with a bonding energy of 396.7 eV was detected, which may be Si–N bond.[11] It was believed that N atoms were piled up at the Si interface and bonded to Si atoms after DAA step.[12] It was clearly observed that the Si2p spectrum was composed of mainly bulk component (Si–Si bond) with a binding energy of 98.1 eV[11] and other chemical shifted components, which can be attributed to Si–O bond and Si–N bond with bonding energies of 101.2 eV and 102.1 eV, respectively. Our sample was exposed to the air for several days before XPS measurement, so oxide signal (Si–O bond) was observed in Si2p spectrum.

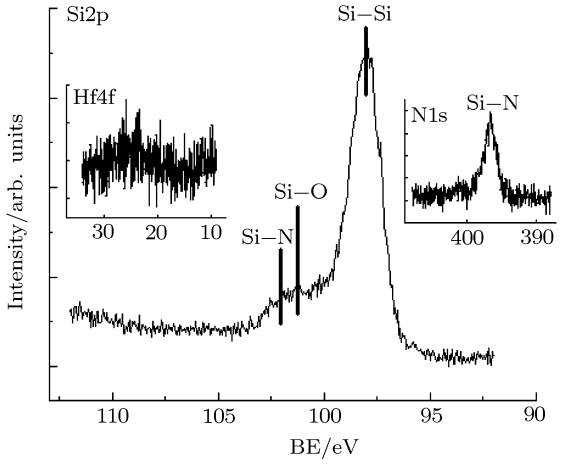


Fig. 4. XPS spectrum of Si2p after HfSiON wet etching. Hf4f and N1s spectra were also shown in the insert.

In order to study the behaviour of B activation in Ge, P^+/N diodes were fabricated by BF_2 implantation and annealed at different temperatures. I–V characteristics of the diodes are shown in Fig. 5. Without DAA, the diode shows significant reverse leakage. When the diode was annealed at 300 °C for 40 min, the reverse leakage current reduced a little, indicating insufficient B activation and defect annealing. When the diode was annealed at 400 °C for 40 min, the reverse leakage current was significantly reduced about 10^3 times. Well behaved P^+/N diode with $I_f/I_r = 10^4$ was obtained after 400 °C 40 min furnace anneal.

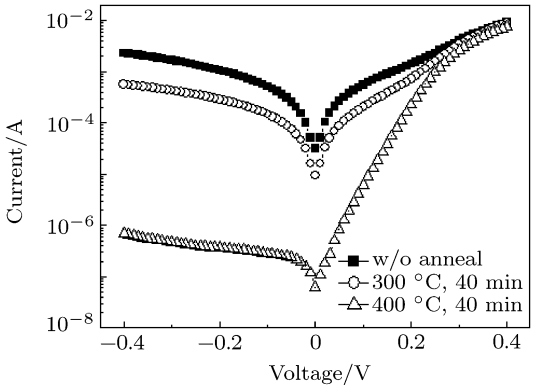


Fig. 5. I–V characteristics of Ge P^+/N diodes at different dopant activation temperatures.

3. Results and discussion

High resolution transmission electron microscopy (HRTEM) images of HfSiON dielectric deposited on Si and Ge substrates are shown in Figs. 6(a) and 6(b), respectively. In order to simulate the highest thermal budget in our process flow, PDA was performed at 900 °C for 30 s and 400 °C for 40 min on Si and Ge substrates, respectively. The thickness of HfSiON is about 4.8 nm. The interfacial SiO_2 layer on Si substrate is about 0.7 nm, while the interfacial GeO_x ($1 < x < 2$) layer on Ge substrate is about 1nm. Crystallization of HfSiON on Si substrate was never observed, indicating that it has very good thermal stability.

C–V curves of Si and Ge MOS capacitors are shown in Fig. 7.

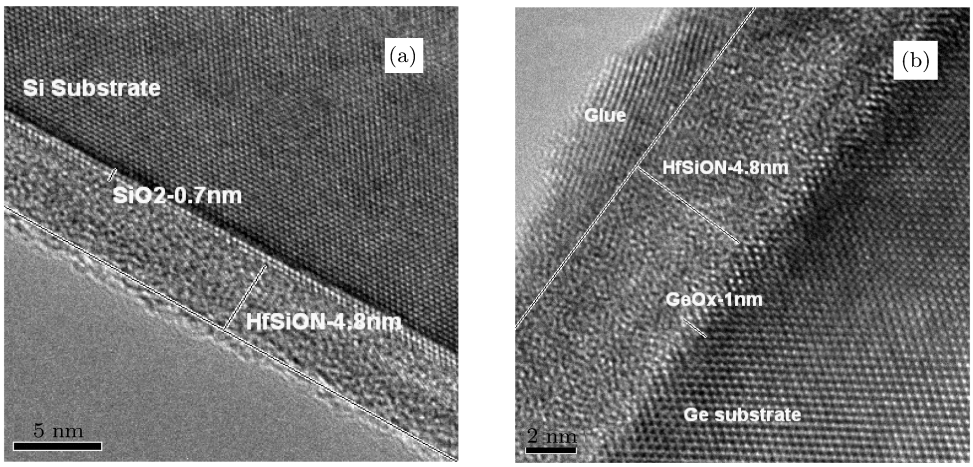


Fig. 6. HRTEM images of HfSiON dielectric deposited on Si (a) and Ge (b) substrates.

The voltage was swept in dual direction and the curve hysteresis is clearly seen. The hysteresis of Ge MOS capacitor (355 mV) is larger than that of Si MOS capacitor (32 mV), suggesting that a large number of charge trapping centres were present in GeO_x. Different from SiO_2, GeO_x has poor electrical property, which causes a significant hysteresis in Ge C–V curve as shown in Fig. 7.[13]

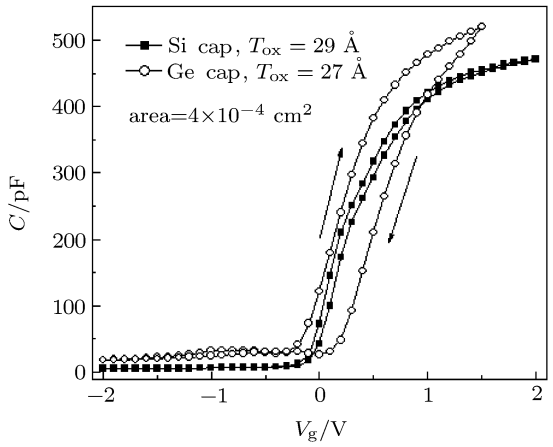


Fig. 7. C–V characteristics of Si and Ge MOS capacitors with fully processed flow. Gate voltage was swept in dual direction.

The measured transfer characteristics of Si and Ge p-MOSFETs are shown in Fig. 8(a) and 8(b), respectively. The transistor gate length is 10 μm and drain voltage was set to be −0.1 V. Both source (I_s) and drain (I_d) currents are shown in Fig. 8. The subthreshold slopes for Si and Ge p-MOSFETs are 123 mV/dec and 94 mV/dec, respectively. When the gate voltage is small (near 0 V), I_d is larger than I_s for Ge transistors, which may be caused by drain/substrate PN junction leakage. When the gate voltage is larger than 1 V, I_s is larger than I_d for Ge transistors, which may be caused by gate leakage

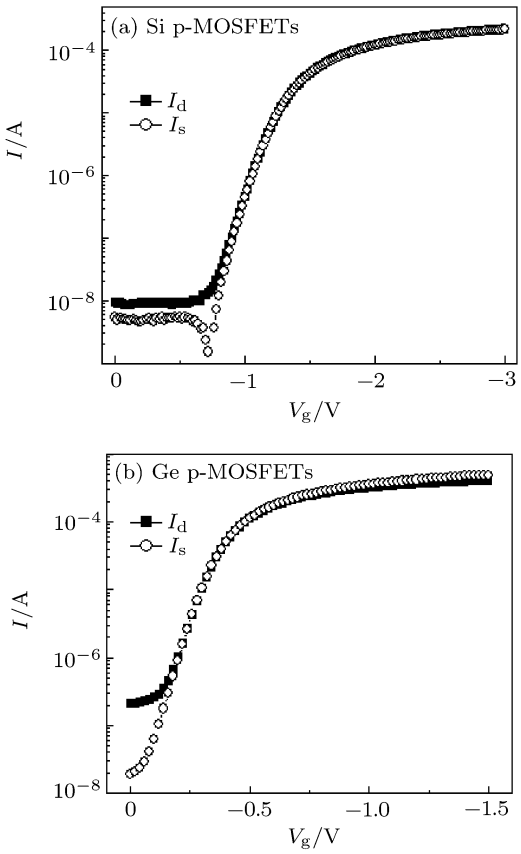


Fig. 8. $I-V_g$ transfer characteristics of Si (a) and Ge (b) p-MOSFETs. Both source (I_s) and drain (I_d) currents were shown in the figure. The transistor gate length is 10 μm and drain voltage was set to be −0.1 V.

current. As our gate contact was drawn in the source region, a large gate electrode area induces a large gate leakage current at high gate voltages.

Threshold voltage ($V_{\rm th}$) was extracted from the linear regime equation

$$I_d = \frac{W}{L}\mu_{\rm eff}C_{\rm ox}(V_{\rm gs} - V_{\rm th} - 0.5V_{\rm ds})V_{\rm ds}. \qquad (3)$$

As the drain voltage was small (−0.1 V), the intercept of $I_{\rm d} - V_{\rm gs}$ curve in linear scale was $V_{\rm th} + 0.5V_{\rm ds}$. Using this method, the values of $V_{\rm th}$ extracted for Si and Ge p-MOSFETs are −1.3 V and −0.3 V, respectively. The difference in $V_{\rm th}$ was mainly caused by the difference in bandgap between Si and Ge.

Ge and Si p-MOSFETs with gate lengths from 2 μm to 100 μm were all workable. The measured 10 μm gate length output characteristics of Si and Ge transistors are given in Figs. 9(a) and 9(b), respectively. All the transistors exhibit a reasonable turn-on behaviour and a relatively high saturation current. The saturation drain currents of Si and Ge p-MOSFETs are 0.43 μA/μm and 1.22 μA/μm at

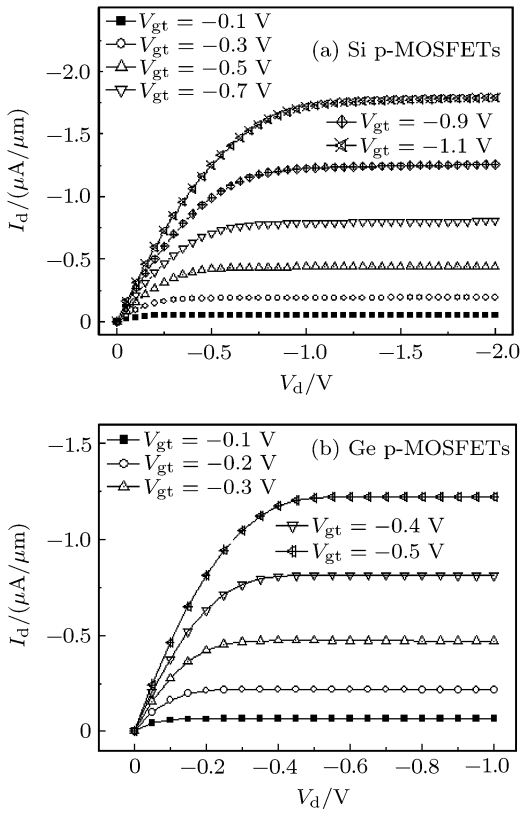


Fig. 9. $I_{\rm d} - V_{\rm d}$ output characteristics of Si (a) and Ge (b) p-MOSFETs at different gate overdrives ($V_{\rm gt} = V_{\rm gs} - V_{\rm th}$). The transistor gate length is 10 μm.

−0.5 V gate overdrive and −1 V drain voltage, respectively. On reducing the gate overdrive close to zero, the transistor characteristics started to be influenced by the gate leakage. At zero gate overdrive (not shown), the drain current and gate leakage current are of the same order of magnitude due to the relatively large gate electrode area for thin HfSiON gate dielectric.

Effective hole mobility was extracted by using the channel conductance method.[14] From Eq. (3), we can derive the following equations:

$$\mu_{\rm eff} = \frac{g_{\rm ds}}{\frac{W}{L}C_{\rm ox}(V_{\rm gt} - 0.5V_{\rm ds})}, \qquad (4)$$

where L is the gate length, W is the real gate width calculated from Eq. (3), $C_{\rm ox}$ is the gate oxide capacitance per unit area which can be measured from the MOS capacitor (shown in Fig. 7), $V_{\rm gt} = V_{\rm gs} - V_{\rm th}$, $V_{\rm th}$ is obtained from Eq. (2). In our $I_{\rm d} - V_{\rm g}$ test, $V_{\rm ds}$ was set to be −0.1 V. Once the drain current is measured, then the channel conductance ($g_{\rm ds} = I_{\rm d}/V_{\rm ds}$) can be calculated. Effective hole mobilities of Si and Ge transistors at different gate overdrives are shown in Fig. 10. The peak hole mobilities of Si and Ge transistors are 33.4 cm^2/(V·s) and 81.0 cm^2/(V·s), respectively. Ge transistors have a hole mobility 2.4 times higher than that of Si control sample. At high gate overdrives, mobilities of Si and Ge transistors are all degraded due to surface scattering, especially for Ge transistors. When the gate overdrive is 1 V (absolute value), the hole mobilities of Si and Ge transistors are 25.1 cm^2/(V·s) and 54.8 cm^2/(V·s), respectively. Even in this condition, Ge transistors have a hole mobility twice higher than that of Si control sample.

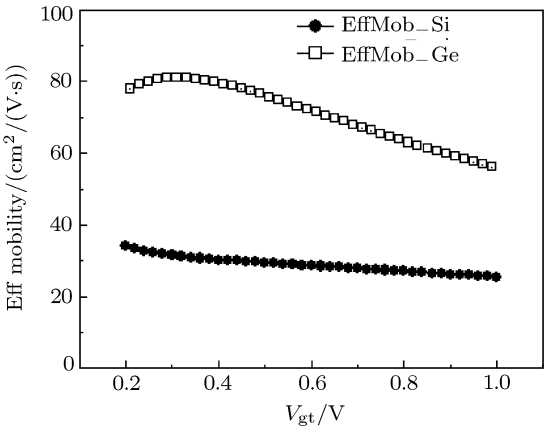


Fig. 10. Effective hole mobilities of Si and Ge transistors at different gate overdrives.

A few factors are believed to contribute to the degradation of hole mobility. Remote phonon scattering has been shown to be the main scattering mechanism present in Si high-K MOSFETs,[15] and it is

likely to occur with using HfSiON high-K dielectric on Ge substract. Also, charge trapping centres in GeO_x are likely to contribute to the degradation of hole mobility through increased Coulomb scattering.[16] In conclusion, at high gate overdrives, hole mobility of Ge transistor is reduced faster than that of Si transistor.

4. Conclusions

Ge and Si p-MOSFETs with HfSiON dielectric and TaN metal gate are fabricated. In order to simplify the fabrication process, self-isolated ring-type transistor structures with two masks are employed. W/TaN metal stacks are used as gate electrode and shadow masks of S/D implantation. HfSiON dielectric is etched in dilute HF and HCl mixing solution. Well behaved Ge and Si p-MOSFETs are demonstrated. Effective hole mobilities of Si and Ge transistors are extracted by using the channel conductance method. Ge transistors have a hole mobility 2.4 times higher than that of the Si control sample.

Acknowledgement

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