Capacitance characteristics of metal-oxide-semiconductor capacitors with a single layer of embedded nickel nanoparticles for the application of nonvolatile memory*

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This paper reports that metal-oxide-semiconductor (MOS) capacitors with a single layer of Ni nanoparticles were successfully fabricated by using electron-beam evaporation and rapid thermal annealing for application to nonvolatile memory. Experimental scanning electron microscopy images showed that Ni nanoparticles of about 5 nm in diameter were clearly embedded in the SiO_2 layer on p-type Si (100). Capacitance–voltage measurements of the MOS capacitor show large flat-band voltage shifts of 1.8 V, which indicate the presence of charge storage in the nickel nanoparticles. In addition, the charge-retention characteristics of MOS capacitors with Ni nanoparticles were investigated by using capacitance–time measurements. The results showed that there was a decay of the capacitance embedded with Ni nanoparticles for an electron charge after 10^4 s. But only a slight decay of the capacitance originating from hole charging was observed. The present results indicate that this technique is promising for the efficient formation or insertion of metal nanoparticles inside MOS structures.

Keywords: metal-oxide-semiconductor, capacitance–voltage, capacitance–time, Ni nanoparticles

PACC: 7340S, 7335C

1. Introduction

Nonvolatile memory devices with high density and high performance have attracted greater interest today due to the current mobile-information market demand. All kinds of semiconductor and metal nanoparticles, such as Si, Ge, Au, Co, and Ni, have been studied extensively for fabricating nonvolatile memory devices by making use of localized trap sites which result from their particular properties, including the Coulomb blockade effect and the controllable size of the nanoparticles.[1−14] Most studies have focused on fabricating semiconductor nanoparticles in metal-oxide-semiconductor (MOS) structures. However, fabrication with metal nanoparticles in MOS memory devices is considered more advantageous in many respects, because of the smaller operating voltages, faster write/erase speeds, and long retention times. Because metal has a larger work function than that of semiconductor, the MOS capacitor with metal nanoparticles is expected to have a deeper potential than that of semiconductor nanoparticles. For instance, Ni has a large work function of 5.0 eV, whereas the most used semiconductor material Si has an electron affinity of 4.05 eV.[15] The larger work-function of Ni provides a higher confinement barrier than that of Si nanoparticles, hence, the electrons captured by the Ni nanoparticles in the MOS structure find it more difficult to escape from the Ni nanoparticles than from the Si nanoparticles in the MOS structure.

With the advent of nanotechnologies, many deposition methods have been used for preparing metal nanoparticles in the MOS structure, such as thermal vapour deposition,[10] pulse-laser deposition,[16] sputter deposition,[17] and the Langmuir–Blodgett technique.[18] Here, we present the fabrication process and memory characteristics of a single layer of Ni nanoparticles embedded into MOS capacitors. The Ni

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nanoparticles were prepared by electron-beam evaporation (EBV) and rapid thermal annealing (RTA) on SiO_2/p-type Si substrates for application to nonvolatile nanocrystal memory. In this paper, the capacitance versus voltage (C–V) and capacitance versus time (C–T) measurements of a representative Ni nanoparticle-embedded MOS capacitor are characterized and discussed.

2. Experiment

The detailed process is illustrated in Fig. 1. The substrates were p-type (100) crystalline silicon. Firstly, each substrate was thoroughly cleaned with the standard RCA I process: treatment with a 1:2:6 solution of NH_4OH (25%), H_2O_2 (30%), and water at 80 °C for 10 min. Then, a SiO_2 tunnel-oxide layer of about 4 nm thick was deposited on the P–Si substrate using dry oxidization at 800 °C for 15 min in an ambience of mixed gas (O_2 mixed with Ar).[19] Here, the thickness of the tunnel layer was estimated from the quartz crystal thickness monitor on EBV. Second, Ni film about 3-nm thick was deposited on the SiO_2 tunnel oxide-layer by the EBV method. Here, evaporated Ni was initially melted in a water-cooled crucible by using an electron beam bent in a magnetic field. Electrons were emitted from a tungsten cathode with 8-kV high tension applied. The process was performed at a 5×10^{-4} Pa vacuum. The evaporation rate was 0.5 nm·min^{-1} and the evaporation current was 25 mA. The thickness of the growing metal layer was estimated by using an oscillating quartz plate placed at the same distance from the crucible as the sample (≈10 cm). Subsequently, the sample was moved into an RTA chamber. RTA was performed at 850 °C for 20 s in N_2 ambience. After this RTA process, the Ni thin film was transferred to a single layer of Ni nanoparticles. Then, a top control SiO_2 layer about 10-nm thick was deposited by the EBV method. Finally, Al gate electrodes were deposited by the EBV at room temperature. The size of the gate electrode was 2.82×10^{-3} cm^{-2}. The size and morphology changes of Ni nanoparticles after deposition of the Al electrode were negligible because of the room temperature deposition process. The MOS capacitors embedded with Ni nanoparticles and the MOS capacitors without Ni nanoparticles (which served as a reference sample) were fabricated for this study. The C–V and the C–T measurements were made with a precision LCR meter (HP4285A).

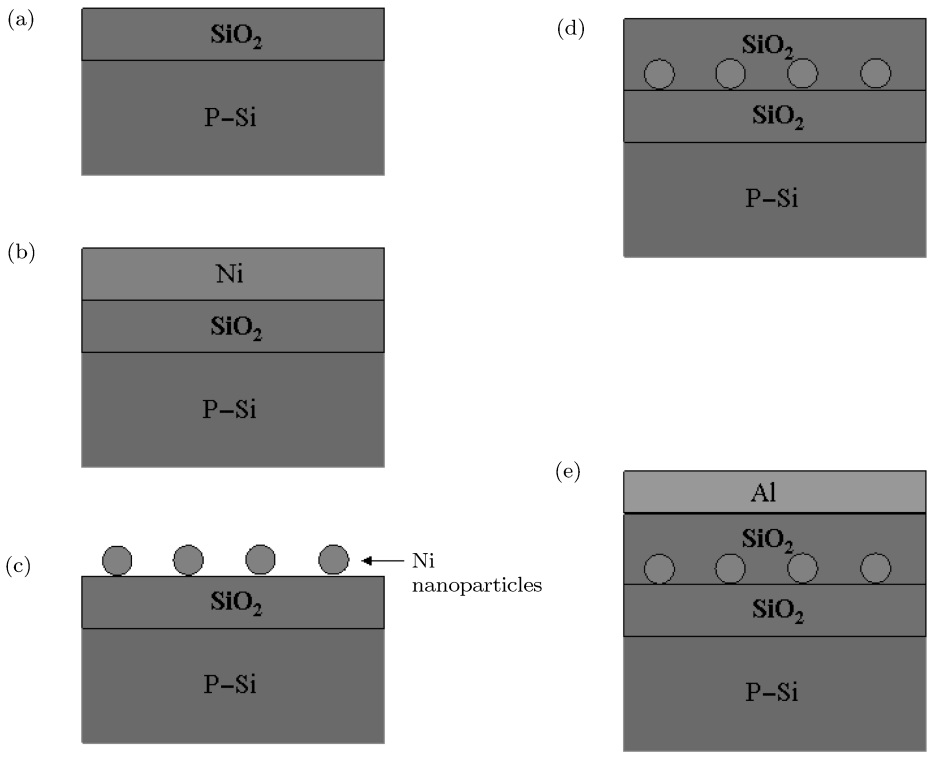


Fig. 1. Detailed process for fabricating Ni nanoparticle-embedded MOS capacitor. (a) A 4-nm layer of SiO_2 tunnel oxide was deposited on P–Si substrate. (b) A 3-nm layer of Ni was deposited on SiO_2 tunnel-oxide layer. (c) The Ni nanoparticles were fabricated by RTA. (d) A 10-nm layer of SiO_2 tunnel oxide was deposited. (e) The Al gate electrode was deposited.

3. Results and discussion

Figure 2 shows a scanning electron microscopy (SEM) image of Ni nanoparticles prepared by the EBV and RTA methods. From this image, one can see that a single layer of nanoparticles was deposited on the oxide layer surface. The average diameter of the nanoparticles is about 5 nm and the density is $\sim 1\times10^{12}/\mathrm{cm}^2$. In this SEM image, the nanoparticles are well separated from each other and the average separation between two neighbouring Ni nanoparticles is approximately 5 nm.

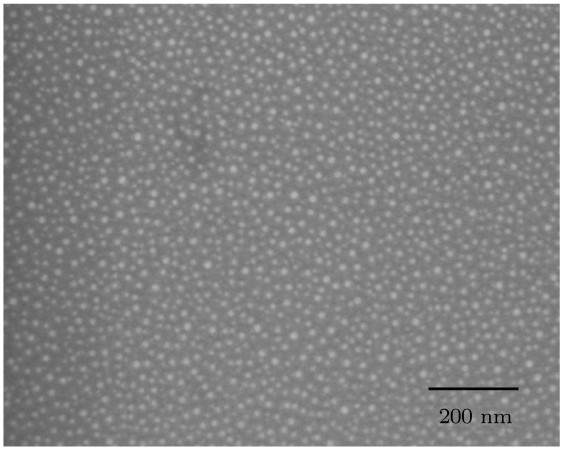


Fig. 2. SEM image of Ni nanoparticles (5 nm in diameter).

Figure 3 shows the C–V theoretical curve of the MOS capacitor described in Refs. [20] and [21] and our experimental results of MOS capacitors with Ni nanoparticles at four different scanning frequencies. The scanning frequencies are 1 kHz, 10 kHz, 100 kHz and 1000 kHz. As seen, our experiments accord well with the theoretical curve. It is confirmed that our MOS structure can be used for memory. In this result, the flat-band voltage shifts to more negative voltage for the positive charge in the oxide layer and the interface state with positive charge between Ni film and the oxide layer (or tunnel layer).[22] These positive charges affect the flat-band voltage. Figure 4 shows C–V curves measured at a frequency of 1 MHz and at a sweep rate of 0.1 $\mathrm{V\cdot s^{-1}}$ for both samples with (sample B) or without Ni (sample A) nanoparticles. The gate voltage was swept from a negative voltage of -4.5 V to a positive voltage of 5.5 V. For sample A, the backward C–V curve nearly overlaps the forward C–V curve, and no clear flat-band voltage shift can be observed. This result indicates that the densities of defects and interfacial states between the control and tunnelling oxide or SiO_2 and P–Si substrate are small. On the other hand, the C–V curve of sample B obtained for the MOS capacitor embedded with Ni nanoparticles demonstrates a flat-band voltage shift of about 1.8 V, which originates mainly from the presence of Ni nanoparticles, rather than the existence of positively charged interfacial states between the interfaces. The C–V characteristics of a single layer of Ni nanoparticle-embedded MOS capacitor studied at four different sweep ranges are shown in Fig. 5. As is clearly observed, the window of the flat-band voltage shifts from 0.8 V at the sweep range -1.5 V$\sim$+5.5 V to 1.8 V at the sweep range -4.5 V$\sim$+5.5 V. When a positive voltage is applied at the gate, electrons from the substrate tunnel to the nanoparticles through the thin tunnel-oxide layer which causes a shift in the C–V curves toward positive voltages. If a negative voltage is applied at the gate, holes tunnel from the substrate to the nanoparticles, or electrons tunnel from the nanoparticles to the substrate which causes a shift in the C–V curves toward negative voltages. Moreover, clockwise hysteresis is observed for all the C–V curves.

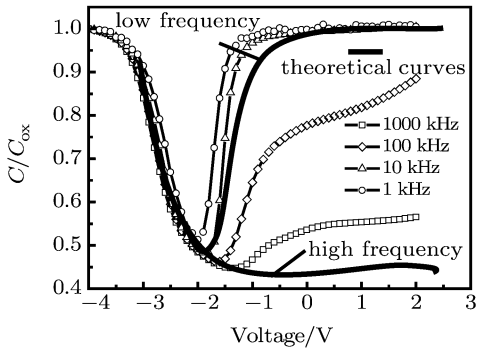


Fig. 3. The C–V theoretical curves (Refs. [20] and [21]) and our experimental C–V curves of MOS. Here, C is the MOS capacitance, C_{ox} is the capacitance of the oxide layer.

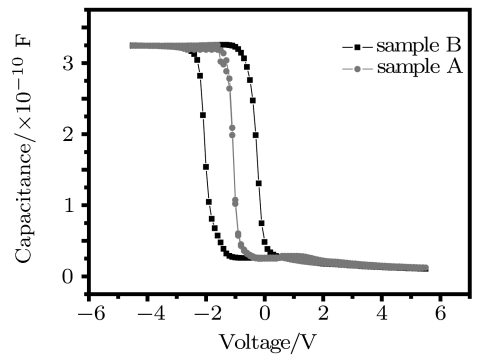


Fig. 4. The C–V curves for MOS capacitors with or without Ni nanoparticles.

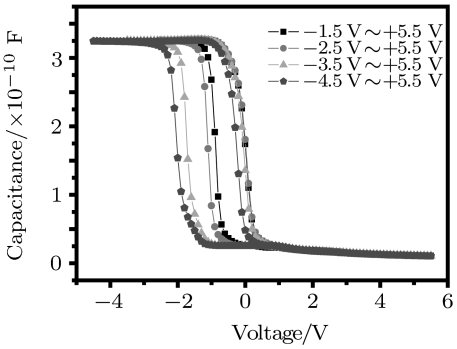


Fig. 5. The C–V curves of the MOS capacitor embedded with Ni nanoparticles in different sweep-voltage ranges.

To investigate the charge storage and retention characteristic of this MOS capacitor embedded with Ni nanoparticles for memory applications, C–T measurements were performed at room temperature, as shown in Fig. 6. The charge loss was monitored at zero gate voltage after the sample was fully charged at an applied bias of ±4 V (electron and hole charging) for 10 s. There are two decay regimes for electron charge in Fig. 6: the first is the initial fast decay; the second is the subsequent slow decay. It is well known that there are four possible discharging paths for electrons in this MOS structure: discharging from Ni nanoparticles to the control gate through the control oxide layer; discharging from the lateral channel of the Ni nanoparticles;[23] discharging from the Coulomb repulsion between electrons confined in nanoparticles,[24] and discharging from the Ni nanoparticles to the substrate through the tunnel-oxide layer. Here, the 10-nm thick control layer is 2.5 times thicker than the tunnelling layer, so discharging current through the control layer can be neglected. The second possible mechanism may be ruled out, because the lateral channel of Ni nanoparticles cannot be formed due to the 5-nm separation between them. Hence, we suggest that the Coulomb repulsion between the confined electrons and the tunnelling electrons from the Ni nanoparticles to the substrate through the tunnel-oxide layer are the origin of the decay. A large number of electrons are confined in Ni nanoparticles after the sample was charged at an applied bias. Then the Coulomb repulsion is increased to the fast charge loss. This is a primary mechanism which can explain the initial fast decay. Subsequently, the Coulomb repulsion is reduced with the electron loss, the electrons tunnelling from the Ni nanoparticles to the substrate through the tunnel-oxide layer. It may take considerable time. The subsequent slow decay is due to this electron tunnel process. Although there was a decay of the capacitance embedded with Ni nanoparticles for electron charge, only a slight decay of this MOS capacitance for hole charge can be observed in Fig. 7. The tunnelling probability $\Gamma(E)$ is described by the relation[25]

$$\Gamma(E) = \exp\left[-\frac{8\pi\sqrt{2m_{\rm ox}}}{3qhE_{\rm ox}} \cdot (\Phi_{\rm B} - E)^{3/2} - (\Phi_{\rm B} - E_{\rm ox} \cdot t_{\rm ox} - E)^{3/2}\right], \quad (1)$$

where $m_{\rm ox}$ is the effective mass of carriers in the oxide, $E_{\rm ox}$ is the electric field in the tunnelling oxide, $\Phi_{\rm B}$ is the barrier height, h is Planck's constant and E represents the energy level. Here, the carriers were holes. Because hole discharging in the Ni nanoparticles at the beginning of the discharging process reduces the electric field, $\Gamma(E)$ and as a result the discharge rate decrease with time. A possible explanation for this result could be the existence of deep donor or acceptor states that were formed by Ni diffusion in the dielectric layer. In the case of Au, the result has been reported by S.J. Pearton *et al.*[26]

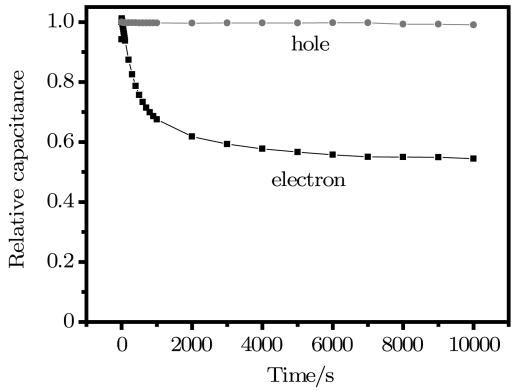


Fig. 6. The C–T curves of the MOS capacitor embedded with Ni nanoparticles.

4. Conclusion

We have presented memory characteristics of a single layer of Ni nanoparticles embedded into MOS capacitors fabricated by using EBV and RTA. The average diameter of Ni nanoparticles is about 5 nm and the estimated density is about $10^{12}/\text{cm}^2$. From the C–V curves of the MOS capacitor, the flat-band voltage shift is 1.8 V at the sweep range −4.5 V∼+5.5 V. A typical hysteresis in the C–V curve due to the charging effect in Ni nanoparticles was clearly observed. In addition, the charge retention characteristics of MOS capacitors were investigated by using C–I measurements. There was a decay of the capacitance embedded with Ni nanoparticles for an electron charge after 10^4 s, and the capacitance for a hole charge was not changed. These results indicate that this method would be an efficient technique for fabrication of nonvolatile memory.

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