Study on the drain bias effect on negative bias temperature instability degradation of an ultra-short p-channel metal-oxide-semiconductor field-effect transistor*

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This paper studies the effect of drain bias on ultra-short p-channel metal-oxide-semiconductor field-effect transistor (PMOSFET) degradation during negative bias temperature (NBT) stress. When a relatively large gate voltage is applied, the degradation magnitude is much more than the drain voltage which is the same as the gate voltage supplied, and the time exponent gets larger than that of the NBT instability (NBTI). With decreasing drain voltage, the degradation magnitude and the time exponent all get smaller. At some values of the drain voltage, the degradation magnitude is even smaller than that of NBTI, and when the drain voltage gets small enough, the exhibition of degradation becomes very similar to the NBTI degradation. When a relatively large drain voltage is applied, with decreasing gate voltage, the degradation magnitude gets smaller. However, the time exponent becomes larger. With the help of electric field simulation, this paper concludes that the degradation magnitude is determined by the vertical electric field of the oxide, the amount of hot holes generated by the strong channel lateral electric field at the gate/drain overlap region, and the time exponent is mainly controlled by localized damage caused by the lateral electric field of the oxide in the gate/drain overlap region where hot carriers are produced.

Keywords: negative bias temperature instability, drain bias, electric field, localized damage

PACC: 7340Q, 7300, 7220J

1. Introduction

Device degradation caused by negative bias temperature instability (NBTI) is a serious problem in ultra-deep sub-micrometre metal-oxide semiconductor field-effect transistors (MOSFETs).[1−5] The NBTI is an effect which occurs in p-channel metal-oxide-semiconductor field-effect transistors (PMOSFETs) under negative gate bias stress and at high temperature. It can lead to the increase of $V_{\rm th}$ and the degradation of $I_{\rm d}$ and $G_{\rm m}$. As NBTI has been one of the most important reliability concerns for modern integrated circuits (ICs) and is receivingmore and more attention, much work has been done on it up to now. The effect of different conditions, such as adding substrate voltage stress[6,7] or drain voltage stress,[8−11] has been studied, and many reasonable models have been brought forward. Woltjer R *et al.* reported that when the gate voltage stress is lower than that of the drain in PMOSFETs, degradation is mainly caused by the generation of negative charges and interface traps caused by electron injection.[12] Doyle thought that under high temperature and channel hot carrier (HC) stress, the NBTI and HC mechanisms act independently and in separate regions of the device.[13] Tsuchiya proposed that there are two HC injected oxide regions during HC injection (HCI) stress.[14] Kufluoglu attributed the degradation of HCI to the reaction of holes and Si–H bonds and the two-dimensional diffusion of H related species. However, there is no uniform mechanism for the combined degradation of HCI and NBTI. In this paper, in order to study the mechanism in detail, different gate and drain voltages are concerned and the effect of hot holes on NBTI degradation is studied. We found that the electric field of the gate/drain overlap region is essential to the degradation of the combined gate and drain stress.

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2. Devices and experiments

The PMOSFETs used in this study are composed of surface channels. They were manufactured by a 90-nanometre process technology with lightly doped drain (LDD) structure and a shallow trench isolation (STI) scheme. The scales of devices used here are 10 μm/0.1 μm. The oxide is about 1.4 nm in physical thickness with the decoupled-plasma-nitridation (DPN) process. An Agilent B1500A, a high precision semiconductor parameter analyser, was used to complete the tests, and all stress testing was performed at 120 °C in a dark box. The parameters of the devices are extracted at interval interruptions. Figure 1 shows the schematics of the combination of NBTI and HCI stress. In the experiments of this study, gate voltage stress $V_{\rm gstress} = -1.8$ V/-1.4 V/-1.0 V and drain voltage stress $V_{\rm dstress} = -1.8$ V/-1.4 V/-1.0 V are applied to the devices and other terminals are grounded. Then the combined effect of NBTI and HCI is studied.

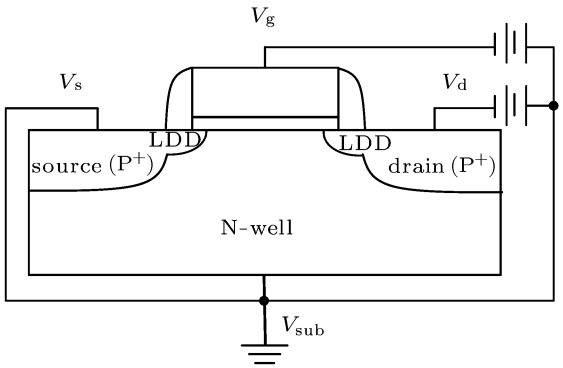


Fig. 1. Schematic of NBTI combined with drain voltage stress.

3. Results and discussion

Figure 2 shows the threshold voltage shift under different drain voltage stresses with $V_{\rm gstress} = -1.8$ V. The drain voltage stresses are -1.8 V/-1.4 V/-1.0 V respectively. With the decrease of $V_{\rm dstress}$, the degradation magnitude and the time exponent n both become smaller and are even reduced to almost the same as that of NBTI.

The time exponents under different drain voltage stresses with $V_{\rm gstress} = -1.8$ V are shown in Fig. 3. When the drain voltage stress reaches -1.0 V or -1.4 V from the NBTI state, the time exponent becomes larger. When it equals -1.8 V, the increase slope of n is enhanced greatly.

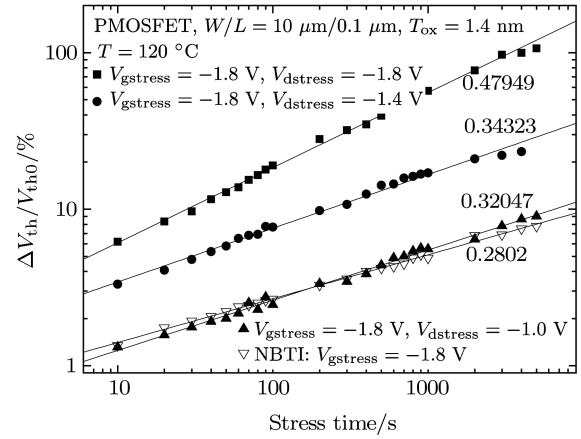


Fig. 2. The threshold voltage shift under different drain voltage stresses with $V_{\rm gstress} = -1.8$ V. With the decrease of $V_{\rm dstress}$, the degradation magnitude and the time exponent become smaller.

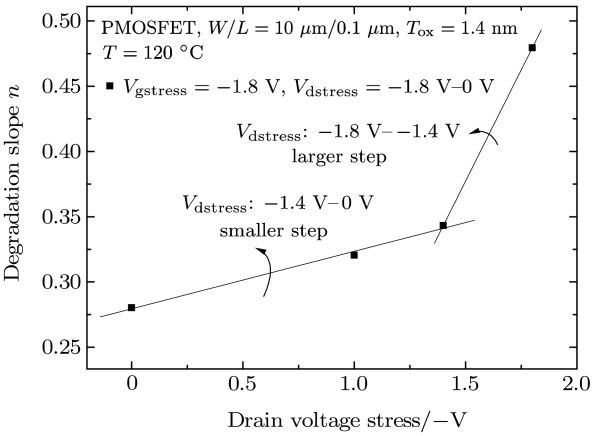


Fig. 3. The time exponents under different drain voltage stresses with $V_{\rm gstress} = -1.8$ V.

Figure 4 shows the degradation of parameters under the conditions of $V_{\rm gstress} = V_{\rm dstress} = -1.8$ V.

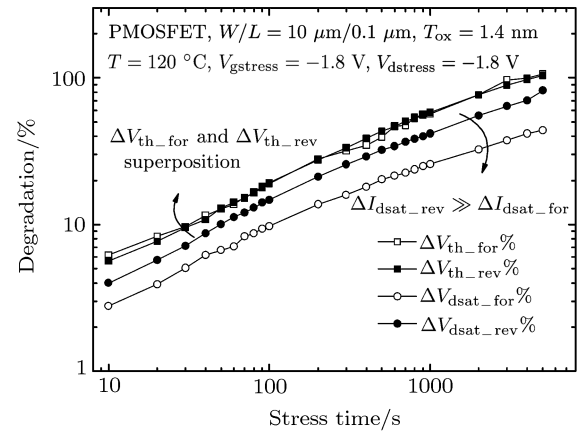


Fig. 4. The degradation of threshold voltage and saturated drain current as a function of time under stress conditions of $V_{\rm gstress} = -1.8$ V and $V_{\rm dstress} = -1.8$ V.

The threshold voltages extracted from the forward linear drain current by the maximum transconductor method $V_{\rm th_for}$ and the reverse $V_{\rm th_rev}$ are almost the same. However, there is a clear difference between the forward and reverse saturated drain currents. The degradation of reverse saturated drain current $I_{\rm dsat_rev}$ is larger than $I_{\rm dsat_for}$ and shows more damage in the near-drain region.[13]

The ratio of $I_{\rm dsat_rev}$ and $I_{\rm dsat_for}$ can reveal the degree of localization damage in the near-drain region.[13] Figure 5 shows the ratio under different drain voltage stresses. From Fig. 5, we can see that with a decrease of the drain voltage stress, the ratio of $I_{\rm dsat_rev}$ and $I_{\rm dsat_for}$ decreases which shows that the localization damage degree in the overlap region of the gate/drain becomes smaller.

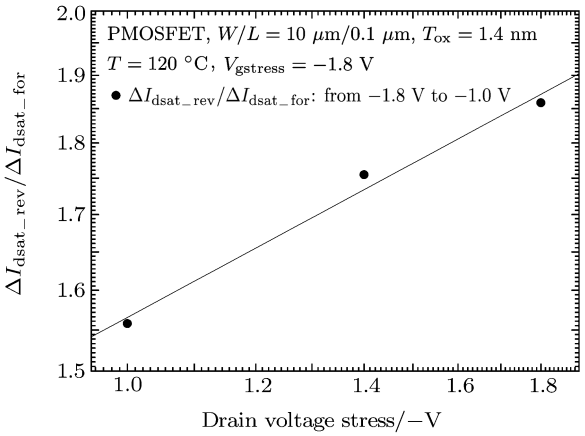


Fig. 5. The ratio of $\Delta I_{\rm dsat_rev}$ and $\Delta I_{\rm dsat_for}$ under different drain voltage stresses.

When drain voltage stress is involved, there are always hot carriers generated to seriously affect the degradation. The higher the drain voltage is, the higher the peak of the lateral electric field in the near-drain channel region $E_{\rm cl}$ is, as shown in Fig. 6, in which the values of lateral electric field are obtained through a simulation with the software Silvaco. Some holes from the inverted channel can gain kinetic energy from the lateral electric field and become hot holes. The hot holes can lead to the generation of impact ionization in the gate/drain overlap region where the peak of the lateral electric field is. Then an amount of hot holes from the impact ionization electron–hole pairs can overcome the Si–SiO_2 barrier height and inject into the oxide. With the increase of the drain voltage stress, more hot holes are generated and the damage in the drain region is enhanced. Therefore, the degradation under the conditions $V_{\rm gstress} = V_{\rm dstress}$ −1.8 V is most serious. However, the time exponent n is not only affected by the amount of hot holes, but also by the lateral electric field of oxide in the gate/drain overlap region $E_{\rm oxl}$ due to the $V_{\rm gstress} - V_{\rm dstress}$ difference. Through simulation by Silvaco, the lateral electric fields of oxide in the gate/drain overlap region are shown in Fig. 7. With the decrease of drain voltage stress, the peak of $E_{\rm oxl}$ increases. Then, there is a greater tendency for the hot holes to move in the lateral direction in the overlap region oxide. Fewer hot holes and a larger lateral damage area cause less localized damage. Then the two-dimensional effect becomes smaller which makes the time exponent n get smaller.[15]

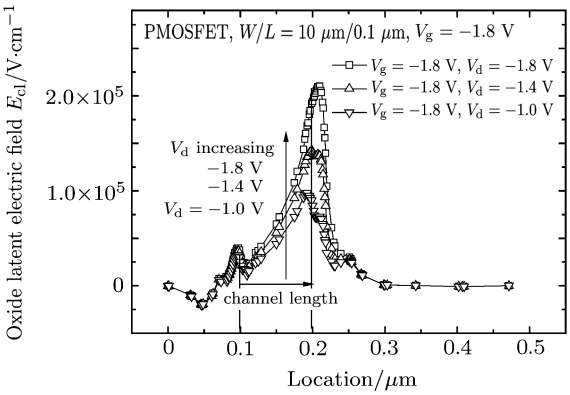


Fig. 6. The lateral electric field in the near-drain channel region.

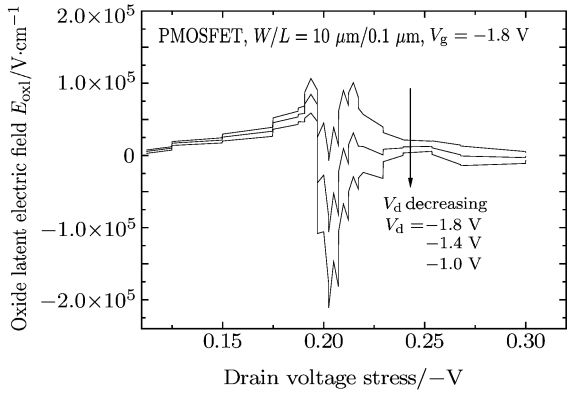


Fig. 7. The lateral electric field of oxide in the gate/drain overlap region due to the $V_{\rm gstress} - V_{\rm dstress}$ difference.

However, at high temperature, the NBTI effect still plays an important role in the degradation during the combined drain voltage stress. The NBTI degradation is mostly caused by the formation of positive charges and interface traps which is mainly controlled by the vertical electric field of the channel region.[13] When the drain voltages are relatively high, the vertical electric fields of the drain side are reduced and

are not very different under different drain voltages as shown in Fig. 8. Therefore, the degradations caused by NBTI are almost the same under these conditions, and the degradation difference is due to the different hot hole damage in the near-drain region which is consistent with the analysis above. However, when the drain voltage further decreases, some different phenomena occur. When the drain voltage gets to −0.5 V, the vertical electric field of the oxide gets larger while the lateral electric field peak in the near-drain channel region gets smaller. The latter leads to fewer HCs and thus less damage in the drain region. Though the vertical electric field in the channel region increases, the total degradation caused by the combined drain voltage effect still declines. By comparison with the degradation of NBTI only, as the vertical electric field of the channel region is smaller than that of NBTI, and the HC effect cannot compensate at all, the degradation of NBTI combined with drain voltage −0.5 V gets smaller than that of NBTI. When the drain voltage gets to be −0.05 V, the electric fields in all regions are almost the same as that of NBTI. Therefore, the two degradations are almost the same, as shown in Fig. 9.

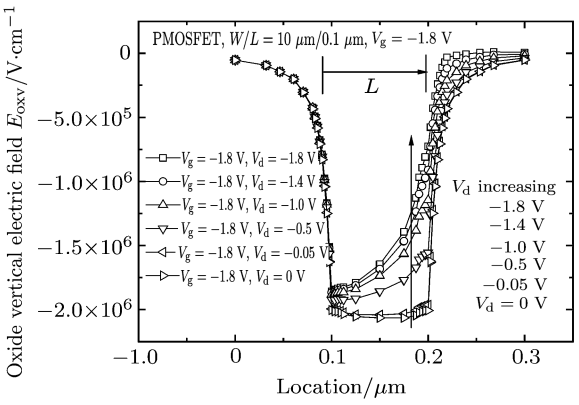


Fig. 8. The vertical electric field of oxide in the channel region.

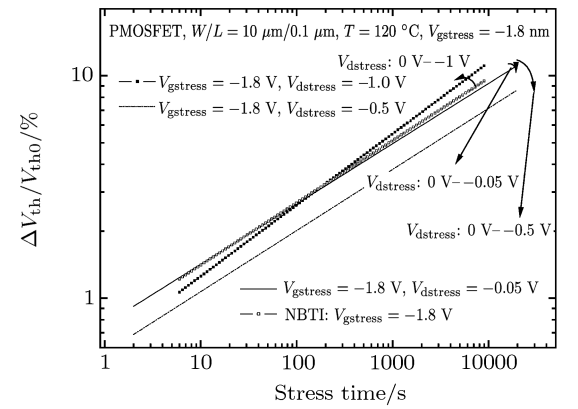


Fig. 9. The threshold voltage shift under different relatively smaller drain voltage stresses with $V_{gstress} = -1.8$ V.

In the above, we studied the degradation of NBTI combined with a drain voltage smaller than the gate voltage. Next, we will also show the results with gate voltage smaller than the drain voltage. Figure 10 shows the threshold voltage shift under different gate voltage stresses with $V_{dstress} = -1.8$ V. The gate voltage stresses are −1.8 V/−1.4 V/−1.0 V respectively. With the decrease of $V_{gstress}$, the degradation magnitude becomes much smaller and the time exponent n gets larger. By comparison with the degradation of NBTI only, we can see that the gate voltage stress determines the magnitude when $V_{gstress}$ gets smaller than that of NBTI. The larger the difference between $V_{gstress}$ and $V_{dstress}$ is, the larger the time exponent n is. At lower gate voltage stress, the vertical electric field in the oxide gets much smaller, as shown in Fig. 11; this fact leads to the decreased degradation. The lateral electric fields of the channel in the drain region and that of the oxide in the gate/drain overlap region all get larger with the decrease of gate voltage stress, and the time exponent n increases. Under these conditions, the direction of the lateral electric fields of the oxide in the gate/drain overlap region is opposite to that discussed above, as shown in Fig. 12.

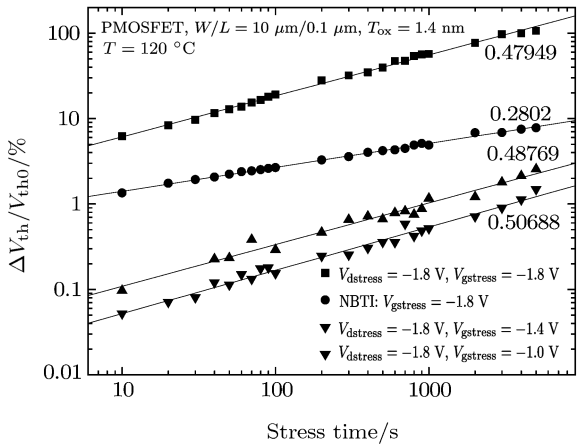


Fig. 10. The threshold voltage shift under NBTI and different relatively smaller gate voltage stresses with $V_{dstress} = -1.8$ V.

Therefore, the carriers tending to move in the lateral direction in the overlap region oxide are not holes but electrons and the holes may inject into the oxide in a more localized region. In our experiments, the results are different from previous studies,[12] and exhibit positive charge degradation. As the devices used here are ultra-short devices, the channel region controlled by the gate voltage stress and the near-drain

region controlled by the combined gate and drain voltage stresses cannot be distinguished clearly. The holes injected into the oxide of the channel region caused by gate voltage stress can neutralize part of the electrons injected into the oxide of the near-drain region caused by the lateral electric field of the oxide. Therefore, the effect of electrons on the degradation is decreased and the localized holes injected into the oxide near-drain region make the time exponents larger.

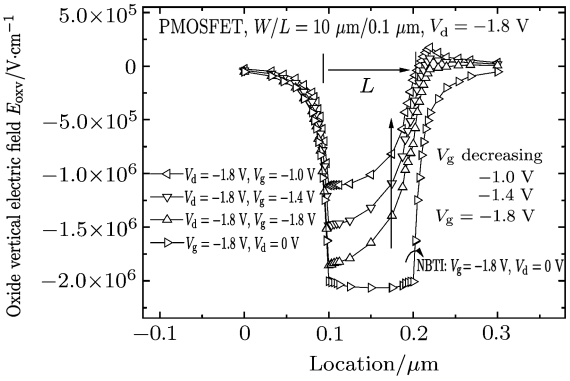


Fig. 11. The vertical electric field of oxide in the channel region.

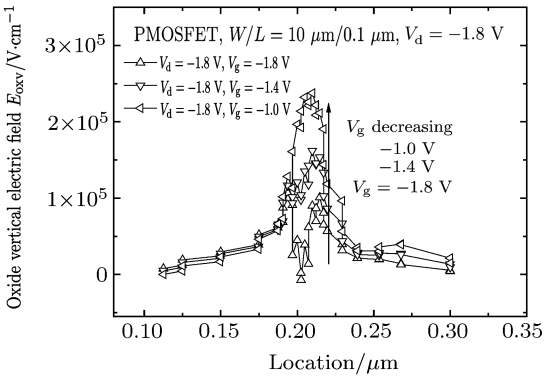


Fig. 12. The lateral electric field of oxide in the gate/drain overlap region due to the $V_{gstress} - V_{dstress}$ difference.

Figure 13 shows the ratio of ΔI_{dsat_rev} and ΔI_{dsat_for} under different gate voltage stresses. With a decrease of the gate voltage stress, the ratio of ΔI_{dsat_rev} and ΔI_{dsat_for} increases which shows that the localization damage degree in the overlap region of the gate/drain becomes larger, and is consistent with the analysis above.

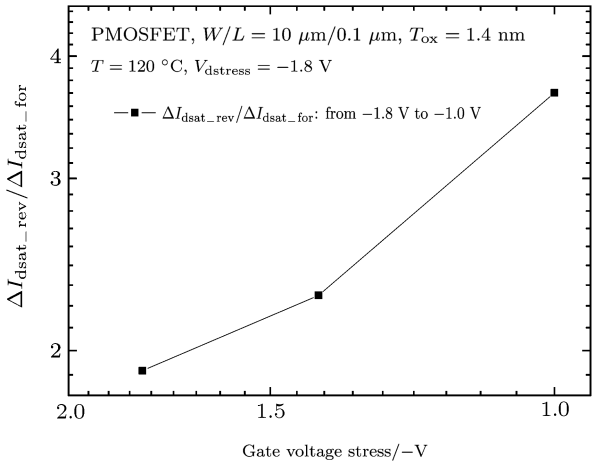


Fig. 13. The ratio of ΔI_{dsat_rev} and ΔI_{dsat_for} under different gate voltage stresses.

4. Conclusions

In this study, we studied the effect of drain bias on ultra-short PMOSFET degradation during NBTI stress. When a relatively large constant gate voltage is applied, the degradation magnitude and the time exponent, with a drain voltage which is the same as the gate voltage supplied, get larger than that of NBTI only. The degradation magnitude is enhanced by the HC effect and the larger time exponent is mainly caused by the greater localization damage. With the decrease of drain voltage, both of the above get smaller, and when the drain voltage further decreases, the degradation magnitude is even smaller than that of NBTI. When the drain voltage gets small enough, the difference between the degradation of NBTI and that combined with drain voltage stress can be ignored as the electric field condition is almost the same as that of NBTI. When a relatively large drain voltage is applied, with the decrease of gate voltage, the vertical electric field of the oxide gets smaller, and the hot carrier effect cannot compensate at all; then the degradation magnitude declines. However, in ultra-short devices, the holes injected into the oxide in the channel region can neutralize the electrons injected by the lateral field of the oxide in the near-drain region, and give degradation caused by positive charges, which is different from previous studies, and the time exponent becomes a little larger.

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