An oxide/silicon core/shell nanowire metal-oxide semiconductor field-effect transistor*

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This paper studies an oxide/silicon core/shell nanowire MOSFET (OS-CSNM). Through three-dimensional device simulations, we have demonstrated that the OS-CSNM has a lower leakage current and higher I_{on}/I_{off} ratio after introducing the oxide core into a traditional nanowire MOSFET (TNM). The oxide/silicon OS-CSNM structure suppresses threshold voltage roll-off, drain induced barrier lowering and subthreshold swing degradation. Smaller intrinsic device delay is also observed in OS-CSNM in comparison with that of TNM.

Keywords: core/shell, nanowire, nanowire MOSFET

PACC: 7340N, 7340T, 6140M

1. Introduction

The continuous reduction of conventional planar metal-oxide semiconductor field-effect transistor (MOSFET) dimensions into the nanoscale regime has encountered many barriers such as the short channel effect (SCE) and gate tunneling. Among the emerging non-classical device structures, surrounding-gate or nanowire MOSFETs offer the best electrostatic integrity.[1] Recently top-down[2,3] and bottom-up[4] approaches have been reported to fabricate gate-all-around silicon nanowire MOSFETs. The small volume and low leakage current of nanowire MOSFETs make them attractive for high density memory arrays and logic chips.[5,6] In addition, heterogeneous material systems like high-K gate dielectric and metal gate electrode have to be integrated as well to provide lower off state current and higher I_{on}/I_{off} ratio.[7]

The core/shell nanowire was first reported in Ref. [8] where radial heterostructure, e.g. Ge/Si core/shell structure, was utilized to form a depletion mode transistor. The homogeneous core/shell nanowire transistor and interesting nanoscale device may be easily fabricated, although it has not been reported so far in the literature. In this work a novel homogeneous radial oxide/silicon core/shell nanowire MOSFET (OS-CSNM) is studied to improve the device performance of a traditional nanowire MOSFET (TNM) and provide a more scalable transistor structure in the nanoscale CMOS era. Through three-dimensional (3D) device simulations, the superiority of the OS-CSNM over TNM is demonstrated.

2. Device structure and simulation

The schematic structure and cross section of the OS-CSNM is shown in Fig. 1. In the schematic structure R is the total radius of the body, t_{ox} is the gate oxide thickness. In the cross section view layers from the inside out are oxide, silicon channel, gate oxide and gate electrode and r_0 is the radius of the oxide core. It is formed by introducing an oxide core into the body region of a TNM while keeping the other structural configuration unchanged. The channel is assumed to be undoped. The source/drain (S/D) regions are heavily doped without additional parasitic resistance reduction structures (e.g. silicide or raised S/D[9]). The gate electrode wraps around the body

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region and S/D contacts are assumed to be idealy Ohmic. As the core/shell structure is very similar to the TNM with an additional oxide core, a similar process as described in Ref. [3] with pre-defined oxide pillar may be used to fabricate the device.

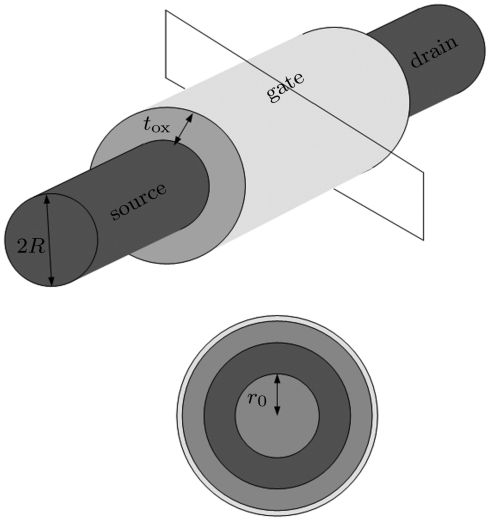


Fig. 1. Schematic structure and cross section of the oxide/silicon CSNM.

The 3D device simulations were performed with Sentaurus.[10] Careful parameter calibration[11] in the technology computer aided design (TCAD) framework has been performed according to data of TNM reported in Ref. [12]. Despite the structural difference between OS-CSNM and TNM, we expect that the fundamental physics which governs the device behaviour will still be followed. Nanowires with different shell radii (mainly $R = 10$ nm is used) together with different core radii ($r_0 = 3$, 5, 7, 8 nm) are studied. Simulations on TNMs are also performed for comparison. The quantum correction model is included in the case where the silicon film is thinner than 10 nm.[13]

3. Results and discussion

3.1. Higher I_{on}/I_{off} ratio

Figure 2 plots the transfer characteristics of long channel OS-CSNMs ($L = 100$ nm) with different core radii together with that of TNMs. The inset in Fig. 2 shows the parameter calibration results. As observed from the figure, the leakage currents of the OS-CSNMs are reduced in comparison with those of the TNMs. Increasing the radius of the oxide core further reduces the off current. For example, when the radius of the core oxide is 5 nm, the off current is about half that of the corresponding TNM.

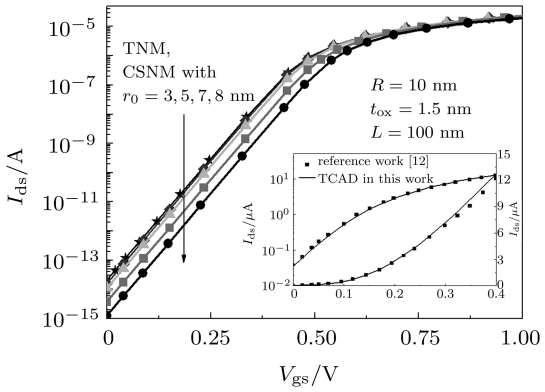


Fig. 2. Transfer characteristics of the OS-CSNMs in comparison with that of TNM. The inset shows the parameter calibration results.

When the core oxide becomes 8 nm, the reduction factor is nearly 17 and the I_{on}/I_{off} ratio is improved by more than one order of magnitude. Qualitatively, the introduced oxide core blocks the leakage current in a TNM at the centre of the channel.[14] However, our preliminary modelling work on this OS-CSNM suggests that the structural change only partially explains this improvement in I_{on}/I_{off} ratio (with the factor being about $R^2/(R^2 - r_0^2)$). Extra enhancement of the ratio is due to quantum mechanical effects (QME) which increase the threshold voltage and reduce the off state current of most nanowire MOSFETs.[15] The OS-CSNM is actually a combination of ultra thin body silicon on insulator (SOI)[16] and gate-all-around structure that realizes the advantages of both. Meanwhile, the on current of the OS-CSNM is slightly reduced. However, the reduction is relatively small since the carriers mainly accumulate about 1∼2 nm apart from the channel surface due to the quantum effect[17] in the strong inversion region.

3.2. Improved scalability

As the OS-CSNM is a hybrid of gate-all-around and ultra thin body structure, very good gate control over the channel is expected. Figure 3 plots the threshold voltage (extracted by the constant current method) versus channel length of the OS-CSNM and that of the TNM for comparison. For the same channel length and radius, the magnitude of the threshold voltage of OS-CSNM is larger than that of TNM due to the reduced channel volume and QME. It can be seen from the figure that for the same channel radius

of the nanowire devices, increasing the core oxide radii suppresses the threshold voltage roll-off significantly.

Figure 4 plots the subthreshold swing and the drain induced barrier lowering (DIBL) versus channel length for the same devices simulated in Fig. 3. With the increase in the oxide core radii, subthreshold swing degradation and the drain induced barrier lowering are suppressed. In general, the OS-CSNM has better scalability than that of TNM with the same channel length.

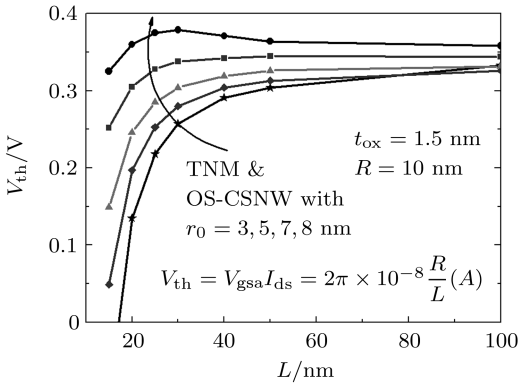


Fig. 3. Threshold voltage roll-off versus channel length of both OS-CSNM and TNM.

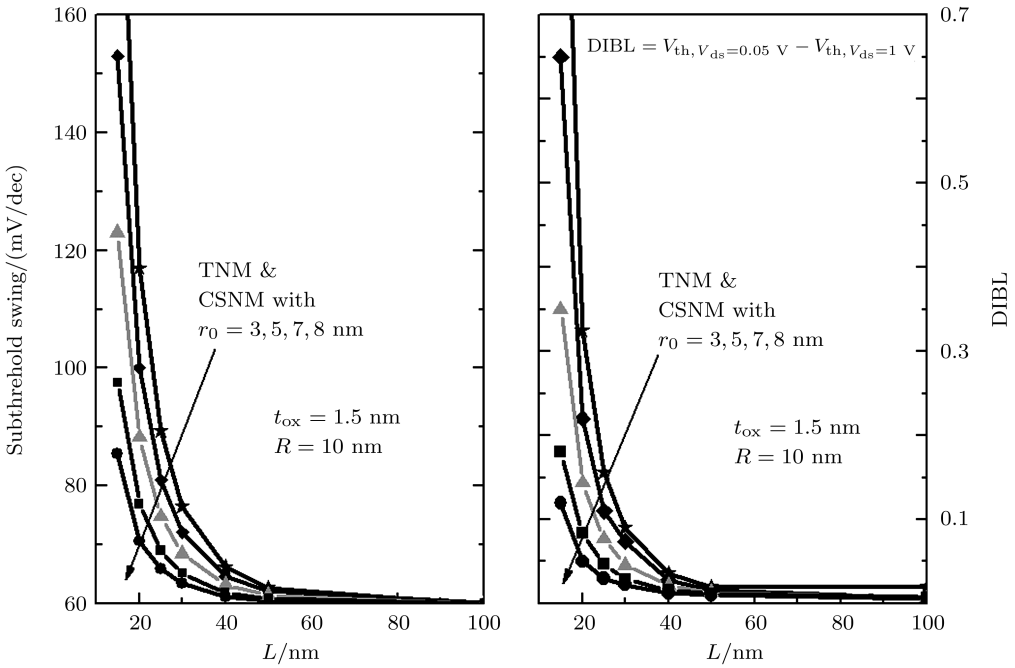


Fig. 4. Subthreshold swing & DIBL versus channel length of both CSNW and TNM.

3.3. Additional benefits

For a specified level of SCE or DIBL, larger radii can be used for an OS-CSNM in comparison with a TNM at the same channel length. As a result, the need to aggressively reduce the radii of TNMs to control SCE is relaxed. The current drive, which is proportional to the silicon channel perimeter, can be increased by using a larger nanowire radius. Despite the loading due to the gate capacitance increasing ac-

cordingly, smaller intrinsic device delay ($\tau \approx CV/I$) is obtained from the OS-CSNM structure according to the device simulation. For example, with equal DIBL at a channel length of $L = 20$ nm, $\tau = 0.043$ ps for the TNM with $R = 4$ nm and $\tau = 0.036$ ps for OS-CSNM with $R = 10$ nm, $r_0 = 8$ nm are obtained.

4. Conclusions

In this paper a homogeneous radial OS-CSNM is proposed as an extension to traditional nanowire devices. The 3D device simulations indicate that proposed devices have lower leakage current and improve the $I_{\rm on}/I_{\rm off}$ ratio by more than one order of magnitude. Gate control over the channel of OS-CSNM is improved, leading to better scalability. Smaller intrinsic delay can also be achieved with the proposed structure. The OS-CSNM relaxes the urgent need to reduce the traditional nanowire diameter and provides an option for ultimate device scaling.

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