Simulation research on offset field-plate used as edge termination in 4H–SiC merged PiN-Schottky diodes*

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A new structure of 4H–silicon carbide (SiC) merged PiN-Schottky (MPS) diodes with offset field-plate (FP) as edge termination is developed. To understand the influences of 4H–SiC MPS diodes with offset FP on the characteristics, simulations have been done by using ISE TCAD. Related factors of offset FP have been studied as well to optimise the reverse characteristics of 4H–SiC MPS diodes. The simulation results show that the device using offset FP can create a higher blocking voltage under reverse bias as compared with that using field guard rings. Besides, the offset FP does not cause any extra steps in the manufacture of MPS diodes.

Keywords: 4H–SiC, merged PiN-Schottky, offset field-plate, reverse characteristics

PACC: 7330, 7340G, 7340N

1. Introduction

SiC has attracted substantial interest in high power and high temperature applications due to its wide band-gap and thermal conductivity, because it has a high critical breakdown electric field and high thermal conductivity (~ 4.9 W/cm·K). SiC-based devices are believed to replace silicon-based devices in the market of high power devices. Because of their large bandgap, SiC PiN diodes, however, may not show a true advantage over SiC Schottky barrier diodes (SBDs) in terms of on-state conduction loss for lower voltage (1–3 kV) applications.[1] However, SiC PiN diodes have the clear advantage of having much lower reverse leakage currents. In terms of off-state performance, SiC SBDs tend to show much higher leakage currents because Schottky barrier heights are generally substantially smaller than the bandgap of SiC (3.26 eV for 4H–SiC). Hence, a diode, which possesses the best features of the SBD and PiN, is needed. Such a device is formed by merging a PiN and SBD into a single structure, called a merged PiN-Schottky (MPS) diode. It combines the forward characteristics of the Schottky diode with the reverse property of the PiN diode, and the tradeoff between the device reverse leakage current and the forward voltage drop can be obtained because the device reverse characteristics are determined by PN junctions of the device instead of the Schottky barrier height.

To create a higher reverse blocking voltage, edge termination is required. Recently, several 4H–SiC MPS diodes have been reported by different groups.[2−4] The field guard ring (FGR) is an edge termination structure that has been used in 4H–SiC MPS diodes, which introduces dynamically negative charge along the surface of an n-type voltage blocking layer.[5] However, FGR has a shortcoming that it is very sensitive to the charges formed in the passivation layer. Since it can hardly prevent either positive or negative charges from leaving the passivation layer during the oxidizing process, it is necessary to find a way to counteract this effect, which brings us an adding FP over the passivation layer.[6] Figure 1 shows the structure of the MPS diodes with offset FP as edge termination.

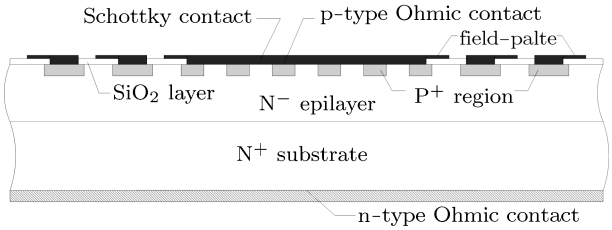


Fig. 1. Schematic cross section of the MPS diodes with offset FP as edge termination.

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In this paper, we study the effect of the offset FP on the blocking voltage and the mechanism of the blocking voltage reduction.

2. Analysis of the offset FP

Charges in the passivation layer have a strong impact on depletion layer spreading.[7] As shown in Fig. 2, for n-type substrate devices, negative charges cause the light doping side of the depletion layer to spread farther while positive charges block the spreading boundary. For p-type substrate devices, the influences will be in reverse. In Fig. 2(a), the existence of negative charges weakens the electric field crowding effect, leading to a higher blocking voltage.

In the device fabrication process, positive charges cannot be avoided in thermal oxidation. These positive charges include: (i) movable positive charges caused by contamination, such as sodium, potassium and hydrogen ions, and (ii) fixed charges located in the vicinity of 20 nm from the SiC/SiO_2 interface.

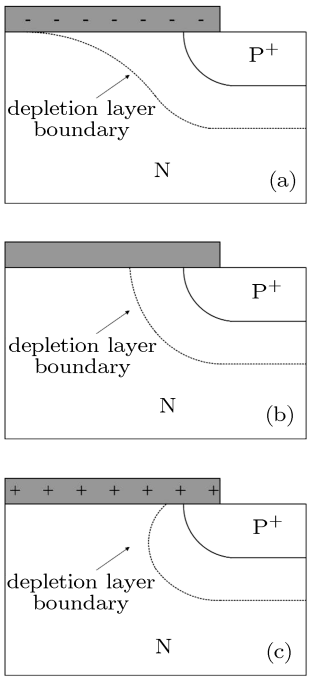


Fig. 2. Influence of surface charges on depletion layer spreading at the edge of a planar junction: (a) negative charges (b) without charges (c) positive charges.

As can be seen in Fig. 2(c), because of the positive charges located in the vicinity of dozens of nanometers from the Si/SiO_2 interface, the electron density at the SiC surface is much higher than that in the bulk, and the shape of the depletion layer is narrowed down at the surface. Under reverse bias, in the n-side of the PN junction, the electrical field strength at the SiC surface is higher than elsewhere, so too high an electrical field strength will cause breakdown of devices at the surface. Therefore, the breakdown voltage is lower than the ideal one with no charges in the SiO_2 layer.

3. Simulations and results

3.1. Device structure

The structure of the device used for the simulation is shown in Fig. 1. Parameters considered in the simulations are shown in Fig. 3. In the structure, FP consists of a Schottky metal-overlap over a SiO_2 layer, with length L. In the FGR structure, the parameters investigated are the ring width w and the distance between two nearest guard rings d. For the MPS part, the PN junction width is denoted as m, and the Schottky region width is denoted as s.

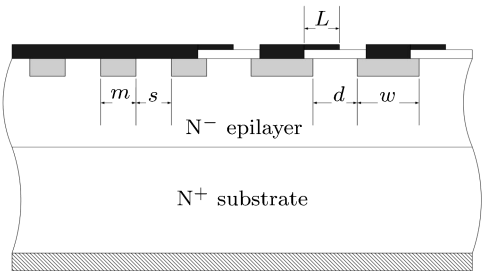


Fig. 3. Parameters of the offset-FP MPS structure.

3.2. Models and parameters

Simulations were carried out using the two-dimensional device simulators ISE-DESSIS. The program includes Shockley–Read–Hall and Auger recombination, carrier-dependent lifetimes, high field saturation and avalanche models.[8]

The basic drift–diffusion equations are as follows:[9]

Poisson's equation:

$$\varepsilon\nabla^2\psi = -q(p - n + N_{\rm D}^{+} - N_{\rm A}^{-}) - \rho_{\rm s}; \qquad (1)$$

Continuity equation:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \boldsymbol{J}_{\rm n} - U_{\rm n} = F_{\rm n}(\psi, n, p)\ ,$$
$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla \boldsymbol{J}_{\rm p} - U_{\rm p} = F_{\rm p}(\psi, n, p)\ ; \qquad (2)$$

Carrier transport equation:

$$\boldsymbol{J}_{\rm n} = q\mu_{\rm n}\boldsymbol{E}_{\rm n}n + qD_{\rm n}\nabla \boldsymbol{n},$$
$$\boldsymbol{J}_{\rm p} = q\mu_{\rm p}\boldsymbol{E}_{\rm p}p - qD_{\rm p}\nabla \boldsymbol{p}. \qquad (3)$$

Here ψ is defined as the intrinsic Fermi potential. $N_{\rm D}^{+}$ and $N_{\rm A}^{-}$ are the ionized impurity concentrations, $\rho_{\rm s}$ is the surface charge density, and $\mu_{\rm n}$ ($\mu_{\rm p}$) is the electron (hole) mobility.

3.3. Simulation results and discussions

According to a simulation that has been done for studying MPS characteristics,[10,11] m is chosen to be 4 μm, s is set to 2 μm, the epilayer is doped to 1.65×10^{15} cm^{-3}, the p regions are all set to 1×10^{18} cm^{-3}, the Schottky barrier is set to 1.26 eV.[12] The optimum thickness of the FP dielectric is: (i) it should be sufficiently thick so that the electric field inside the insulator will not exceed the breakdown strength of the dielectric and (ii) it should be sufficiently thin so that the FP can influence the electric field distribution inside the semiconductor and provide sufficient field relief at the corner. SiO_2 layer has a fixed thickness value of 1 μm. Figure 4 shows the influence of the charges in the SiO_2 layer on the reverse characteristics of the MPS diode terminated by FGR; in this case, only one single ring is used in the structure, and the w is set to 10 μm, d to 6 μm. It can be seen that the curve with charges 1×10^{11} cm^{-2} in the SiO_2 layer has a breakdown voltage of 140 V, lower than that without charge in the SiO_2 layer (the breakdown voltage is defined as the voltage at which the current increases rapidly).

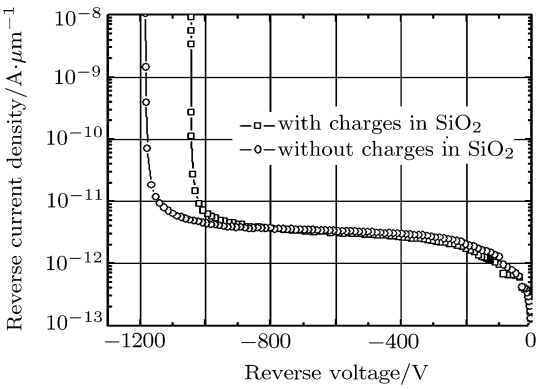


Fig. 4. Simulated reverse characteristics of an MPS diode with and without charges in the SiO_2 layer.

To eliminate the negative impact that has been inspected previously, FP is added. The distance between two nearest guard rings d is an important parameter influencing the offset FP. It can be seen in Fig. 5 that with increasing d from 6 μm to 10 μm, the breakdown voltage is getting lower. This is because, as the distance between two FGRs gets bigger, the effect of the rings in extending the electric field gets weaker. However, as Fig. 5 shows, with reducing d, the increment of breakdown voltage is remarkably getting smaller. Since smaller d will not act effectively on increasing breakdown voltage, and too small d will increase the difficulty in the manufacture, 6 μm is chosen to be the fixed value of d in the simulations below.

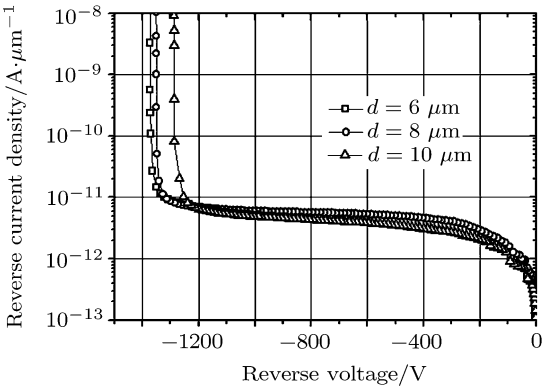


Fig. 5. Simulated reverse characteristics of an MPS diode terminated by offset FP for different distances between two FGRs.

From Fig. 6, it can be seen that the breakdown voltage increases with increasing FP length from 0 to 3 μm; after that, the breakdown voltage drops and reaches a stable value about 1325 V when L is 5 μm or 6 μm. This is because when L is longer than 3 μm, the avalanche happens at the edge of the FP; once L reaches 5 μm, the electric field is distributed by the second circle of offset FP efficiently which keeps the breakdown value stable. We expected that electric fields at the offset FP reach relative values close to each other under breakdown state. As can be seen in Fig. 7, the MPS diode terminated by offset FP (L = 5 μm, d = 6 μm, m = 10 μm) has a much smoother electric field line as

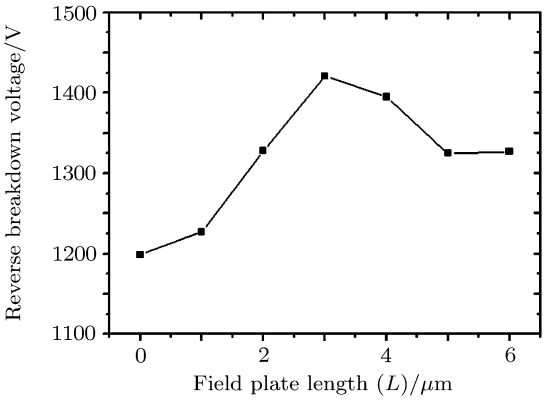


Fig. 6. Variation of breakdown voltage with FP length.

compared with that only using FGR as a termination. The results show that the highest breakdown voltage occurs at $L = 3$ μm; in this case the avalanche almost simultaneously happens at the corner of the PN junction and along the edge of the FP of the first circle of the offset FP.

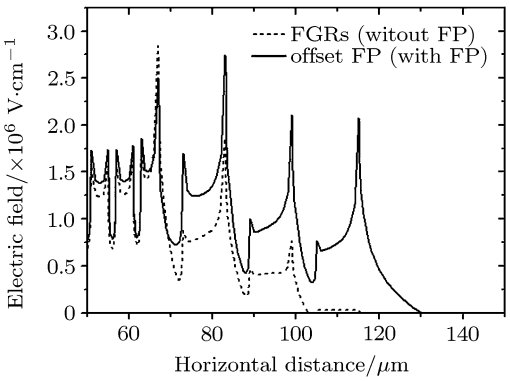


Fig. 7. Simulated reverse characteristics of an MPS diode terminated by offset FP and FGR.

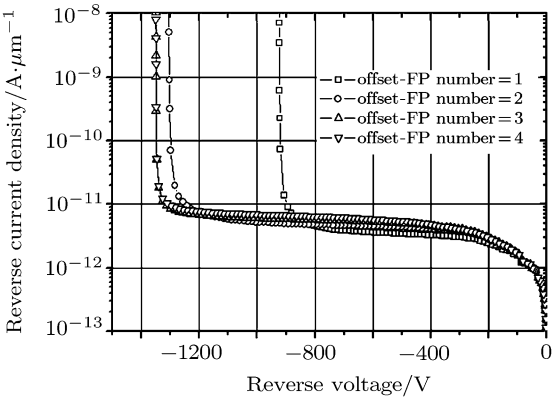


Fig. 8. Simulated reverse characteristics of an MPS diode terminated by offset FP for different offset FP numbers.

As can be seen in Fig. 8, the breakdown voltage does not increase with the number of the offset FPs when it increases from 3 to 4. The reason is that as the number of the offset FPs increases, the circles outside will not redistribute the electric field, and the avalanche will happen in the inside circles before the outside circle can have an effective influence on the extending of the electric field line.

In the simulations described previously, the offset FP is distributed in equidistance, thus it is convenient to use the exhaustive method in the research. As the results show, the highest breakdown voltage is up to 1421 V, which is about 81% of the planar PiN junction with the same area of anode. The reverse characteristics of FP in the non-equidistance design are better than that in the equidistance design,[6] so the breakdown voltage will be increased more in the non-equidistance design.

4. Summary

A new structure of 4H–SiC MPS diodes with offset FP as edge termination has been developed in this paper. With FP lying over the passivation layer, the negative effect of the charges on this layer will be counteracted. The simulated results indicate that the characteristics of the SiC MPS diode are remarkably improved with offset FP. A structure with the highest breakdown voltage of 1421 V has been achieved using the offset FP with equidistance. As the structure suggests, it will not need any extra technical steps in the manufacture.

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