# Study of a 4H–SiC epitaxial n-channel MOSFET*

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Epitaxial channel metal-oxide semiconductor field-effect transistors (MOSFETs) have been proposed as one possible way to avoid the problem of low inversion layers in traditional MOSFETs. This paper presents an equation of maximum depletion width modified which is more accurate than the original equation. A 4H–SiC epitaxial n-channel MOSFET using two-dimensional simulator ISE is simulated. Optimized structure would be realized based on the simulated results for increasing channel mobility.

**Keywords:** SiC, epitaxial layer, MOSFET, mobility

**PACC:** 7280, 7330, 7340S, 7220

## 1. Introduction

The excellent physical properties of silicon carbide (SiC) and the fact that its native oxide is $SiO_2$ render it ideally suited for the fabrication of high-voltage and high-temperature metal-oxide semiconductor field-effect transistors (MOSFETs). At present, however, SiC inversion-mode MOSFETs suffer from low inversion channel mobility and gate oxide reliability problems. The major reasons[1,2] for low channel mobility are attributed to interface state and surface roughness through trapping and scattering effects for the carriers. In addition, surface roughness may also give rise to the concerns of gate oxide reliability. This is mainly due to the heavy dose implantation and high-temperature annealing at the source/drain region.[3]

Various methods have been proposed to improve the quality of the MOS interface. Nevertheless, the inversion layer mobility reported so far is still too low for practical application of MOSFETs. One possible solution for the improvement of the channel mobility is to keep electrons away from the $SiO_2$/SiC interface. But the above-mentioned problems arising from implantation and high-temperature annealing are still existed for the buried channel (BC) structure by ion implantation.

Epitaxial channel MOSFETs have been proposed as one possible way to avoid the problem of low inversion layers in traditional MOSFETs.[4,5] In such a device, the conduction of current consists of the majority carriers in a physical channel, which have much higher carrier mobility, in comparison with the minority carriers in an inversion layer. In addition, no implantation and high-temperature annealing is performed. In this study a 4H–SiC epitaxial n-channel MOSFET using two-dimensional (2D) simulator ISE is simulated. The device structure may be optimized based on these results for elevating channel mobility.

## 2. Device structure

The depth of the n-type channel layer ($D_{\rm ch}$) is important for epitaxial channel MOSFETs. It is designed to be less than or equal to the maximum depletion of a MOS capacitor if the depletion width penetrating into the channel layer arising from PN junction is negligible. The maximum depletion of a MOS capacitor is given by[6]

$$x_{s\,\max} = \left(-\frac{4\varepsilon_s \psi_{\rm B}}{qN_{\rm D}^+}\right)^{1/2}, \tag{1}$$

where $\varepsilon_{\rm s}$ is the permittivity of SiC, $\psi_{\rm B}$ is the potential difference between the Fermi level $E_{\rm F}$ and the intrinsic Fermi level $E_{\rm i}$ (negative for n-type substrate) and $N_{\rm D}^+$ is the concentration of the ionized donor. Incomplete ionization of SiC material must be accounted for calculating $\psi_{\rm B}$, which is given by

$$\psi_{\rm B} = -\frac{k_{\rm B}T}{q}\ln\left(\frac{\beta N_{\rm D}}{n_{\rm i}}\right), \tag{2}$$

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where $\beta$ is the impurity ionization ratio in the semiconductor which is about 90% for $N_{\rm D} = 1\times10^{17}$ cm$^{-3}$. But $x_{\rm s\,max}$ should be over valuated if $N_{\rm D}^{+}$ in Eq. (1) is still equal to $\beta N_{\rm D}$, because almost completely ionized donor impurity in the depletion region is induced by stronger electric field at strong inversion. The design of device structure is affected by the error. So equation (1) is modified by

$$x_{\rm s\ max} = \left(-\frac{4\varepsilon_{\rm rs}\varepsilon_0\psi_{\rm B}}{qN_{\rm D}}\right)^{1/2} = \left(\frac{4\varepsilon_{\rm rs}\varepsilon_0 k_{\rm B}T}{q^2N_{\rm D}}\ln\left(\frac{N_{\rm D}\beta}{n_{\rm i}}\right)\right)^{1/2}. \quad (3)$$

The schematic structure of a 4H–SiC epitaxial n-channel MOSFET determined by Eq. (3) is shown in Fig. 1.

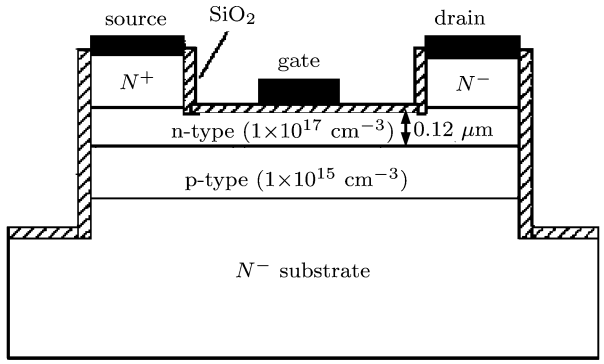



**Fig. 1.** Schematic structure of a simulated 4H–SiC epitaxial n-channel MOSFET.

## 3. Model

In this paper the device mentioned above is simulated by using two-dimensional (2D) simulator ISE. Different models should be chosen for different materials and structures. An incomplete ionization model for incomplete ionization of SiC material is chosen. Mobility models include bulk mobility ($\mu_{\rm b}$) and surface mobility degradation models ($\mu_{\rm s}$).[7] The bulk mobility model describes the scattering effect of lattice and impurity ions. Surface scattering is important for a MOSFET which leads to the degradation of the surface mobility. The effect of surface scattering on mobility is operated through the transverse field ($F_{\perp}$). This transverse field is induced by gate voltage and interface charges.

$$\frac{1}{\mu} = \frac{1}{\mu_{\rm b}} + \frac{1}{\mu_{\rm s}(F_{\perp})}. \quad (4)$$

## 4. Results and discussion

This device is simulated with 2-$\mu$m channel length, 20-nm oxide thickness and a channel concentration ($N_{\rm D}$) of $1\times10^{17}$ cm$^{-3}$. The distribution of $N_{\rm D}^{+}$ of the n-channel layer at different surface states is shown in Fig. 2, by which the field-induced ionization effect is confirmed. Donor impurity is almost completely ionized at the pinched-off state ($V_{\rm G} = V_{\rm P}$).

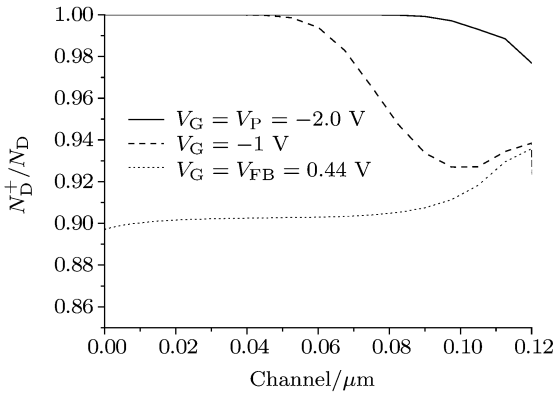



**Fig. 2.** The distribution of $N_{\rm D}^{+}$ of the n-channel layer at different surface states.

The $I_{\rm DS}$–$V_{\rm G}$ characteristics of the device at room temperature, $V_{\rm DS} = 50$ mV, and $V_{\rm FB} = 0$ (flat band voltage) are shown in Fig. 3. The effect of surface scattering on the device is presented by a comparison between the $I_{\rm DS}$–$V_{\rm G}$ curve with and without the surface scattering effect. The channel mobility of this device is rarely affected by surface scattering because channel electrons are away from the $SiO_2$/SiC interface at depletion mode, namely buried channel mode. Also, channel mobility at accumulation state is greatly degraded by surface scattering. The device should operate at depletion mode for increasing channel mobility.

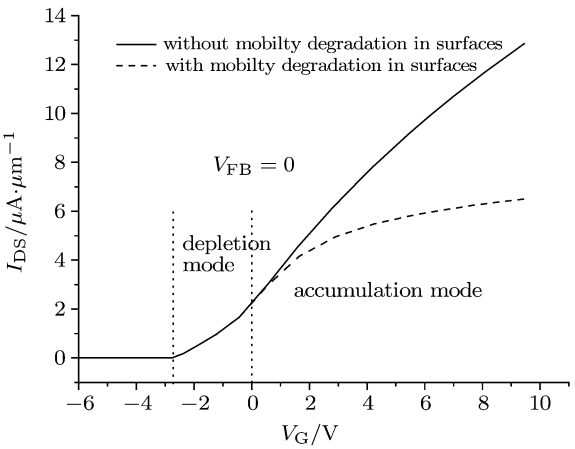



**Fig. 3.** Drain current versus gate voltage at $V_{\rm DS}$ = 50 mV, $V_{\rm FB} = 0$.

The effect of interface state density on $I_{DS}$–$V_G$ characteristics is shown in Fig. 4. In SiC MOS structure, the interfacial traps in the upper half of the bandgap are believed to be acceptor-like in nature. Interface charges are negative at flat band, depletion and accumulation state. Thus, interface state density $D_{it}$ is defined for the upper bandgap acceptor states. Flat band voltage shifts to the opposite direction for negative interface charges. But the pinched-off voltage is almost unchanged. The field-effect mobility obtained from the $I_{DS}$–$V_{GS}$ curve is reduced due to the presence of negative interface charge, which is more obvious at accumulation mode.

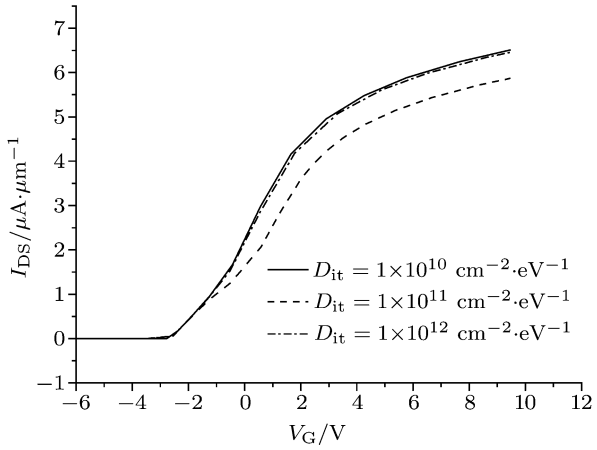



**Fig. 4.** Drain current versus gate voltage at different interface state densities.

Figure 5 shows that taking into account different n-channel layer concentrations must satisfy the term of the maximum depletion which is greater than the channel-layer depth. For example, the maximum depletion for $N_D = 2\times10^{17}$ cm$^{-3}$ is equal to 0.128 $\mu$m ($> 0.12$ $\mu$m) calculated by Eq. (3). The voltage range operated at buried channel mode is expanded because the pinched-off voltage of the device decreases with increasing channel-layer concentration. But increase of channel-layer concentration should lead to deterioration of the sub-threshold characteristic. Also, the off-state current of this device reaches saturation after strong inversion of the surface, in comparison with the traditional inversion-mode MOSFET, which increases with channel-layer concentration. The rate of on/off-current is only $10^3$ for $N_D = 2\times10^{17}$ cm$^{-3}$. So $N_D$ should be traded off between the operating range of buried channel mode and sub-threshold characteristics.

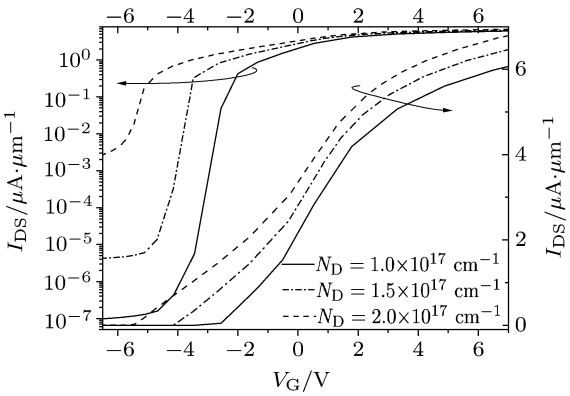



**Fig. 5.** Drain current versus gate voltage at different n-channel layer concentrations.

## 5. Summary

Epitaxial channel MOSFETs have been proposed as one possible way to avoid the problem of low inversion layers in traditional MOSFETs. In this paper, the equation of maximum depletion width is modified which can be used in the accurate design of device structure. A 4H–SiC epitaxial n-channel MOSFET using 2D simulator ISE is simulated. The results of the simulation show that this structure of MOSFET has good immunity from the effect of surface scattering on the channel mobility of this device at depletion mode. The field-effect mobility is reduced due to interface state at accumulation mode. The operating range of buried channel mode is expanded with increasing channel-layer concentration which leads to deterioration of off-state and sub-threshold characteristics. Optimized structure would be realized based on these results for increasing channel mobility.

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