A new structure and its analytical model for the vertical interface electric field of a partial-SOI high voltage device*

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A new partial-SOI (PSOI) high voltage device structure called a CI PSOI (charge island PSOI) is proposed for the first time in this paper. The device is characterized by a charge island layer on the interface of the top silicon layer and the dielectric buried layer in which a series of equidistant high concentration n^+-regions is inserted. Inversion holes resulting from the vertical electric field are located in the spacing between two neighbouring n^+-regions on the interface by the force with ionized donors in the undepleted n^+-regions, and therefore effectively enhance the electric field of the dielectric buried layer (E_I) and increase the breakdown voltage (BV), thereby alleviating the self-heating effect (SHE) by the silicon window under the source. An analytical model of the vertical interface electric field for the CI PSOI is presented and the analytical results are in good agreement with the 2D simulation results. The BV and E_I of the CI PSOI LDMOS increase to 631 V and 584 V/μm from 246 V and 85.8 V/μm for the conventional PSOI with a lower SHE, respectively. The effects of the structure parameters on the device characteristics are analysed for the proposed device in detail.

Keywords: interface charges, breakdown voltage, partial-SOI, self-heating effect

PACC: 7340T, 7300, 7340L

1. Introduction

Silicon on insulator (SOI) material presents some advantages compared with traditional bulk substrates, and therefore has attracted considerable attention in the area of VLSI applications. There are two major concerns in the development of SOI technology, i.e. increasing the breakdown voltage (BV) and reducing the self-heating effect (SHE). Some studies have been carried out to solve the former problem.[1−4] Enhancing the electric field of the dielectric buried layer is an effective method to increase BV by enhancing dielectric layer field (ENDIF)[5,6] and several new structures have been developed by ENDIF.[7−11] Moreover, partial-SOI (PSOI) technology can be used to reduce SHE due to its silicon window connecting the active region to the substrate, which offers a heat conduction path, thereby achieving a high BV.[12−15] In the present paper, a new interface charge island structure of a high voltage device on PSOI (CI PSOI) and an analytical model of the vertical interface electric field are proposed for the first time. The operation of CI PSOI is different from all the above-mentioned structures and it provides a new and effective method to enhance the electric field of the dielectric buried layer by introducing interface charges and so increasing BV, reducing SHE at the same time. The effects of structure parameters on the BV and the SHE are analysed and compared with those of the conventional PSOI and SOI.

2. Structure and model

The CI PSOI LDMOS and its mechanism are shown in Fig. 1. Equidistant high concentration n^+-regions are made on the interface of the top silicon layer and the dielectric buried layer (SiO_2) (a CI cell is shown in Fig. 1(b)), and there is a silicon window under the source. t_S, t_I , t_{sub}, t_p and t_C denote the thickness of the top silicon layer, the thickness of the dielectric buried layer, the thickness of the substrate layer, the thickness of the p-top layer, and the thickness of the interface n^+-regions, L_d, L_W, L_E and L_H are the length of the drift region, the length of the silicon window, the length of the interface n^+-regions, and the spacing of two neighbouring n^+-regions, N_d, N_p, N_{n^+} and N_{sub} are the impurity concentration of the drift region, the impurity concentration of the p-top layer, the impurity concentration of the interface

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n^+-regions, and the impurity concentration of the substrate layer, respectively, where the concentration of the p-top layer meets the Gaussian distribution in the vertical direction and N_p are actually the surface concentrations. When a high positive voltage V_d is applied to the drain while the source, gate and substrate are grounded, the inversion holes are formed in the spacing of equidistant n^+-regions by the vertical electric field (E_V) and located on the top interface by the combined operation of Coulomb's forces with the ionized donors in the undepleted n^+-regions and the force from the lateral electric field (E_L), as illustrated in Fig. 1(b).

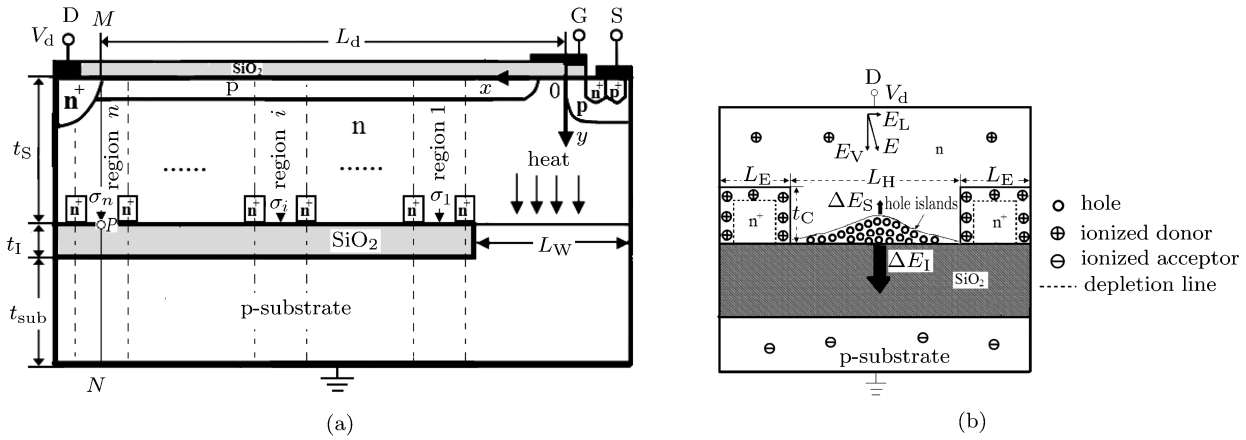


Fig. 1. Device structure with the mechanism of CI PSOI LDMOS. (a) Device structure. (b) A CI cell and work mechanism. E_L and E_V are lateral and vertical electric fields, respectively.

For an optimized device in the lateral direction, BV lies on the vertical BV ($V_{B,V}$), and then, BV is nearly interrelated with the electric field distribution under the drain (along MN in Fig. 1(a)), especially the electric fields $E_{S,P}$ and $E_{I,P}$ on the interface (at P point in Fig. 1(a)), where $E_{S,P}$ and $E_{I,P}$ are the electric fields in the silicon and dielectric buried layer at the P point, respectively. Suppose that the charges are uniformly distributed in each CI cell, and divide the device ($x > L_W$) into n regions as shown in Fig. 1(a): the first CI cell with interface charge density σ_1 is region 1, while the last CI cell (under the drain) with interface charge density $\sigma_n = \sigma_{Ld}$ is region n. When a high positive voltage V_d is applied to the drain while the source, gate and substrate are grounded, the 2D potential $\phi(x,y)$ in the drift region can be written as $\phi(x,y) = \omega(x,y) + \varphi(x,y)$, where $\omega(x,y)$ and $\varphi(x,y)$ are the contributions of V_d and depleted impurities in drift region, respectively, in which $\varphi(x,y)$ satisfies the 2D Poisson equation

$$\frac{\partial^2 \varphi(x,y)}{\partial x^2} + \frac{\partial^2 \varphi(x,y)}{\partial y^2} = -\frac{qN_d}{\varepsilon_S}, \quad 0 \le x \le L_d, 0 \le y \le t_S, \tag{1}$$

where ε_S is the permittivity of silicon and q is the electron charge. For fully-depleted drift region, the vertical electric field in the top silicon layer satisfies

$$E_y(x,y) = -\frac{\partial \varphi(x,y)}{\partial y} = \psi_1(x) + \psi_2(x)y, \quad 0 \le x \le L_d, 0 \le y \le t_S. \tag{2}$$

The boundary conditions for Eq. (2) are given by

$$\left.\frac{\partial \varphi(x,y)}{\partial y}\right|_{y=t_0} = 0, \tag{3a}$$

$$\varphi(0,0) = 0, \quad \varphi(L_d,0) = V_d, \tag{3b}$$

$$\frac{\varepsilon_I[\varphi(x,t_S) - \varphi(x,t_S+t_I)]}{t_I} = -\left.\frac{\partial \varphi(x,y)}{\partial y}\varepsilon_S\right|_{y=t_S} + q\sigma_I(x), \tag{3b}$$

where ε_I is the permittivity of the dielectric buried layer (SiO_2), and Eq. (3c) is based on the continuity of electric displacement on the interface ($y = t_S$). Solving Eq. (2) with the boundary conditions yields

$$\varphi(x,y) = -\frac{1}{2}\psi_2(x)y^2 + \psi_2(x)t^2 + \frac{q\sigma_i(x)t_I}{\varepsilon_I} + \varphi(x,t_S+t_I), \tag{4}$$

where $t = \sqrt{\frac{1}{2}t_{\rm S}^2 + \frac{\varepsilon_{\rm S}}{\varepsilon_{\rm I}}t_{\rm S}t_{\rm I}}$ is the characteristic thickness of SOI/PSOI devices. From Eq. (4), the surface potential distribution ($y = 0$) is obtained as

$$\varphi(x,0) = -\psi_2(x)t^2 + \frac{q\sigma_i(x)t_{\rm I}}{\varepsilon_{\rm I}} + \varphi(x, t_{\rm S}+t_{\rm I}) \quad (5)$$

and so,

$$\psi_2(x) = \frac{\varepsilon_{\rm I}\varphi(x,0) - t_{\rm I}q\sigma_i(x) - \varepsilon_{\rm I}\varphi(x,t_{\rm S}+t_{\rm I})}{\varepsilon_{\rm I}t^2}. \quad (6)$$

With Eq. (6), Eq. (4) yields

$$\varphi(x,y) = \frac{q\sigma_i(x)t_{\rm I} + \varepsilon_{\rm I}\varphi(x,t_{\rm S}+t_{\rm I}) - \varepsilon_{\rm I}\varphi(x,0)}{2\varepsilon_{\rm I}t^2}y^2 + \varphi(x,0). \quad (7)$$

From Eq. (7), the electric potential distribution under the drain (along line MN) can be obtained as

$$\varphi(L_{\rm d},y) = \frac{q\sigma_{\rm I}(L_{\rm d})t_{\rm I} + \varepsilon_{\rm I}\varphi(L_{\rm d},t_{\rm S}+t_{\rm I}) - \varepsilon_{\rm I}\varphi(L_{\rm d},0)}{2\varepsilon_{\rm I}t^2}y^2 + \varphi(L_{\rm d},0). \quad (8)$$

From Eq. (8), the vertical electric field under the drain (along line MN) is derived as

$$E_y(L_{\rm d},y) = \frac{\varepsilon_{\rm I}\varphi(L_{\rm d},0) - q\sigma_i(L_{\rm d})t_{\rm I} - \varepsilon_{\rm I}\varphi(L_{\rm d},t_{\rm S}+t_{\rm I})}{\varepsilon_{\rm I}t^2}y. \quad (9)$$

With Eq. (9) and Gauss-theory on the interface, the electric fields in the silicon and dielectric buried layer (at the P point) $E_{\rm P,S}$ and $E_{\rm P,I}$ are obtained respectively as

$$E_{\rm S,P} = \frac{V_{\rm d} - \varphi(L_{\rm d},t_{\rm S}+t_{\rm I})}{t^2}t_{\rm S} - \frac{t_{\rm I}t_{\rm S}q\sigma_{\rm L_d}}{\varepsilon_{\rm I}t^2}, \quad (10)$$

$$E_{\rm I,P} = \frac{\varepsilon_{\rm S}t_{\rm S}}{\varepsilon_{\rm I}t^2}[V_{\rm d} - \varphi(L_{\rm d},t_{\rm S}+t_{\rm I})] + \frac{t_{\rm S}^2q\sigma_{\rm L_d}}{2\varepsilon_{\rm I}t^2}. \quad (11)$$

From Eqs. (10) and (11), interface charge $\sigma_{\rm Ld}$ in the proposed CI PSOI can enhance $E_{\rm I,P}$ in comparison with the conventional PSOI ($\sigma_{\rm Ld} = 0$), while shielding the silicon layer electric field $E_{\rm S,P}$ from prematurely breaking down the silicon layer (shown as $\Delta E_{\rm I}$ and $\Delta E_{\rm S}$ in Fig. 1(b), respectively). All these will contribute to a high BV. At the same time, the silicon window provides an electric path between the active region and the substrate and reduces SHE. Moreover, with $\sigma_{\rm Ld} = 0$, Eqs. (10) and (11) can be used for the conventional PSOI.

The interface hole accumulating operation of the proposed CI PSOI is completely different from those in Refs. [9]–[11] in which the dielectric layer/trenches are used to prevent the holes from being extracted by the lateral electric field. In addition, only an additional process of phosphor implantation before bonding is needed to form CI PSOI, and its fabrication process is much simpler than those for fabricating the structures in Refs. [9]–[11] and fully compatible with conventional CMOS/SOI technology.

3. Results and discussion

Two-dimensional device simulations[1)] for the proposed CI PSOI LDMOS specified in Table 1 are performed to verify the device operation.

Table 1. Device parameters used in the simulation.

device parameters	CI PSOI	Con. PSOI
drift length, $L_{\rm d}$	40–100 μm	40–100 μm
thickness of top silicon layer, $t_{\rm S}$	5 μm	5 μm
thickness of dielectric buried layer, $t_{\rm I}$	1 μm	1 μm
thickness of p-top layer,$t_{\rm p}$	0.5, 1, 1.5 μm	–
thickness of p-substrate layer, $t_{\rm sub}$	30 μm	30 μm
p-substrate concentration, $N_{\rm sub}$	(1–10)$\times10^{14}$ cm^{-3}	(1–10)$\times10^{14}$ cm^{-3}
thickness of interface n$^+$-region, $t_{\rm C}$	0–1μm	–
interface n$^+$-region length, $L_{\rm E}$	0–1.5 μm	–
spacing of two neighbouring interface n$^+$-region, $L_{\rm H}$	1–4 μm	–
interface n$^+$-region concentration , $N_{\rm n+}$	(0.08–3)$\times10^{19}$ cm^{-3}	–

Figure 2 shows the hole distribution for CI PSOI at breakdown with $t_{\rm S} = 5$ μm, $t_{\rm I} = 1$ μm, $t_{\rm sub} = 30\mu$m, $t_{\rm p} = 1$ μm, $L_{\rm d} = 80$ μm, $t_{\rm C} = L_{\rm E} = 0.5$ μm, $L_{\rm H} = 2$ μm, $L_{\rm W} = 15$ μm, $N_{\rm d} = 1\times10^{15}$ cm^{-3}, $N_{\rm p} = 1.65\times10^{16}$ cm^{-3}, $N_{\rm n^+} = 1\times10^{19}$ cm^{-3}, and $N_{\rm sub} = 3\times10^{14}$ cm^{-3}. Figure 2(a) is the three-dimensional hole distribution, and it is clear that there are high concentration holes ($> 1\times10^{18}$ cm^{-3}) distributed on the interface between the top silicon layer and the dielectric buried layer whose density linearly increases from the

[1)] TMA MEDICI 4.2. Palo Alto CA: Technology Modeling Associates Inc.

source to the drain with potential. The inset shows the hole distribution in the CI cell under the drain. Figure 2(b) gives the hole distribution in the CI cell under the drain with different vertical distances, and it is obvious that the nearer to the interface, the higher the hole concentration is, and the inversion layer is about 90 nm. From Eqs. (10) and (11), the interface holes in the ultra-thin inversion layer should effectively enhance $E_{\mathrm{I,P}}$ and increase BV.

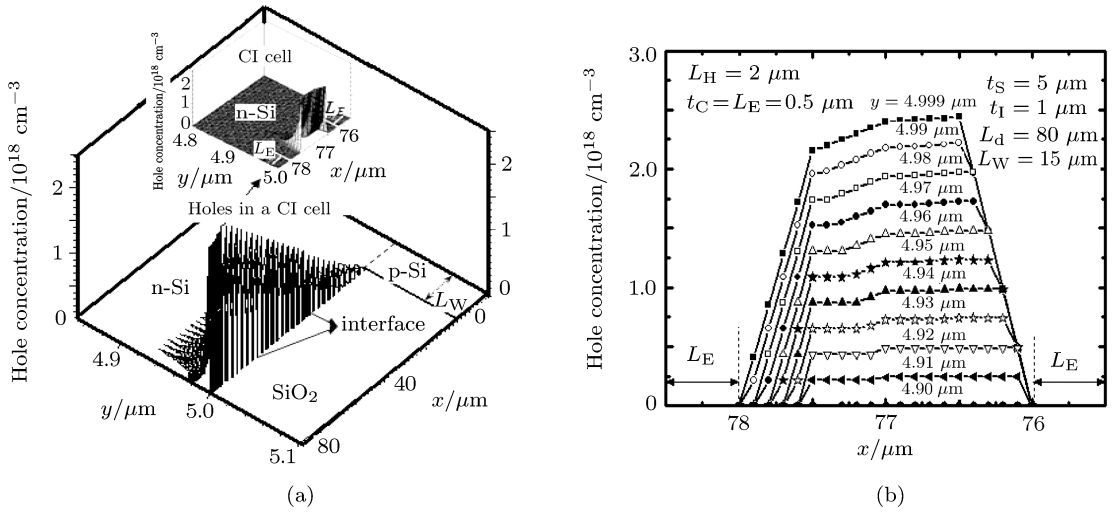


Fig. 2. Hole distribution for CI PSOI LDMOS at breakdown ($t_{\mathrm{S}} = 5$ μm, $t_{\mathrm{I}} = 1$ μm, $t_{\mathrm{sub}} = 30\mu$m, $t_{\mathrm{p}} = 1$ μm, $L_{\mathrm{d}} = 80$ μm, $t_{\mathrm{C}} = L_{\mathrm{E}} = 0.5$ μm, $L_{\mathrm{H}} = 2$ μm, $L_{\mathrm{W}} = 15$ μm, $N_{\mathrm{d}} = 1 \times 10^{15}$ cm^{-3}, $N_{\mathrm{p}} = 1.65 \times 10^{16}$ cm^{-3}, $N_{\mathrm{n+}} = 1 \times 10^{19}$ cm^{-3}, and $N_{\mathrm{sub}} = 3 \times 10^{14}$ cm^{-3}). Panel (a) shows three-dimensional hole distribution, where the inset indicates the hole distribution in the CI cell under the drain, and panel (b) displays hole distribution in the CI cell under the drain with different vertical distances.

Figure 3 shows electric fields and potential distributions for the CI PSOI and the conventional PSOI. Figure 3(a) gives the dependences of the applied voltage V_{d} on the interface electric fields of the silicon layer $E_{\mathrm{S,P}}$ ($y = 4.999$ μm) and the dielectric buried layer $E_{\mathrm{I,P}}$ ($y = 5.001$ μm) in the CI cell under the drain ($x = 80$ μm, along MN). It can be seen that due to the increase of the self-adaptive holes with V_{d}, $E_{\mathrm{I,P}}$ is continuously enhanced, and at the same time, $E_{\mathrm{S,P}}$ is reduced to less than 4 V/μm. However, because of the absence of interface charges, $E_{\mathrm{I,P}}$ of the conventional PSOI is always limited by the dependence of $E_{\mathrm{I,P}} = \varepsilon_{\mathrm{S}} E_{\mathrm{S,P}}/\varepsilon_{\mathrm{I}}$ from Eqs. (10) and (11), and $E_{\mathrm{S,P}}$ rapidly reaches a silicon critical electric field of about 30 V/μm (breakdown point, BP). Figure 3(b) illustrates the vertical electric field distributions and the potential distributions at breakdown for the CI PSOI and the conventional PSOI. It can be seen that $E_{\mathrm{I,P}}$ of CI PSOI increases from 85.8 V/μm of the conventional PSOI to 584 V/μm due to the enhancement effect of the inversion charges ($\Delta E_{\mathrm{I,P}} = 498.2$ V/μm). Moreover, inversion charges reduce the silicon layer electric field on the interface to 3.1 V/μm and avoid prematurely breaking down the silicon layer for the CI PSOI. All the above-mentioned results in a high BV of 631 V for CI PSOI compared with 246 V for the conventional PSOI. Moreover, more than 90% of the BV for CI PSOI is shared by the dielectric buried layer ($V_{\mathrm{I}} = t_{\mathrm{I}} E_{\mathrm{I,P}} = 584$ V), which can be seen from the potential distributions shown in Fig. 3(b), and V_{I} is dominant in the BV. The simulation results are in agreement with the analytical results from Eqs. (10) and (11) in Fig. 3. Therefore, it can be concluded that the interface charges accumulated by the proposed CI PSOI can assuredly enhance $E_{\mathrm{I,P}}$ and increase BV.

Figure 4 illustrates the equipotential contours at breakdown for the CI PSOI and conventional PSOI with $t_{\mathrm{S}} = 5$ μm, $t_{\mathrm{I}} = 1$ μm, $t_{\mathrm{sub}} = 30$ μm, $L_{\mathrm{d}} = 80$ μm, $L_{\mathrm{W}} = 15$ μm and $N_{\mathrm{sub}} = 3 \times 10^{14}$ cm^{-3}. Because of the electric field modulating effect by the interface charges, the equipotential contours of the CI PSOI are more uniform than those of the conventional PSOI, which means a high lateral BV for the CI PSOI compared with the conventional PSOI. In addition, for the conventional SOI device ($L_{\mathrm{W}} = 0$) with the same t_{S}, t_{I} and L_{d}, BV is only 195 V because of the lake of voltages shared by the substrate layer.

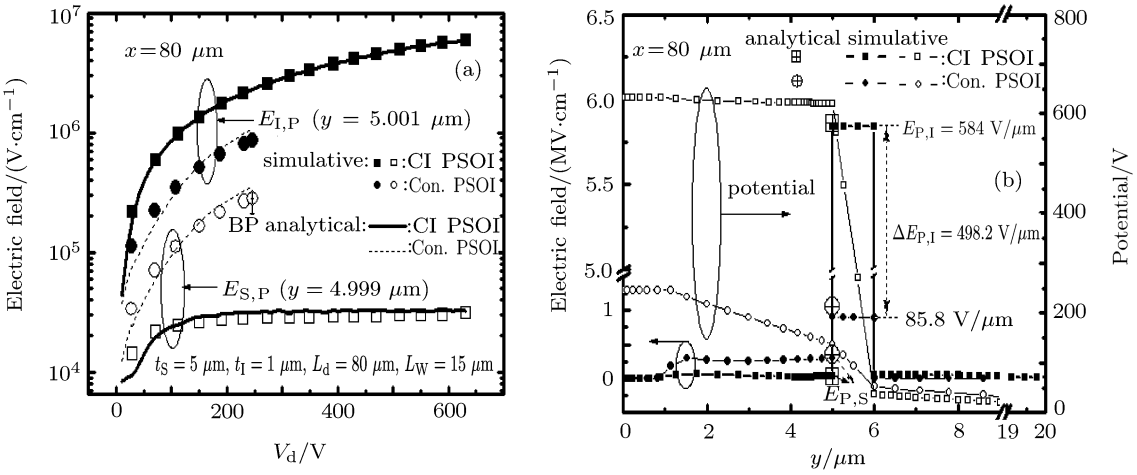


Fig. 3. Electric fields and potentials for the CI PSOI and the conventional PSOI. Panel (a) shows dependences of applied voltage $V_{\rm d}$ on the interface electric field (at the P point) under the drain in the silicon layer $E_{\rm S,P}$ ($y = 4.999$ μm) and the dielectric buried layer $E_{\rm I,P}$ ($y = 5.001$ μm) for the CI PSOI and the conventional PSOI. Panel (b) exhibits vertical electric field distributions and potential distributions under the drain($x = 80\mu$m, along MN).

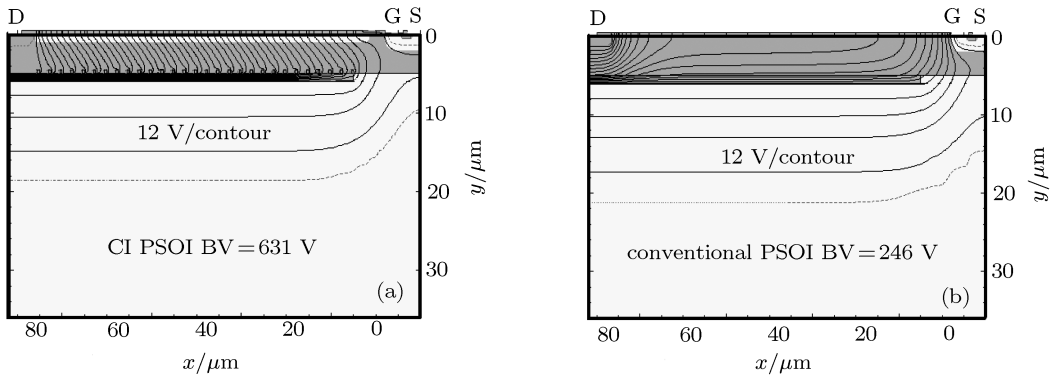


Fig. 4. Equipotential contour distributions ($t_{\rm S} = 5$ μm, $t_{\rm I} = 1$ μm, $t_{\rm sub} = 30$ μm, $L_{\rm d} = 80\mu$m, $L_{\rm W} = 15$ μm and $N_{\rm sub} = 3 \times 10^{14}$ cm^{-3}). Panel (a) shows the equipotential contour distribution of the CI PSOI ($N_{\rm d} = 1\times10^{15}$ cm^{-3}), where the device parameters are the same as those in Fig. 2. Panel (b) exhibits the equipotential contour distribution of the conventional PSOI ($N_{\rm d} = 1.8 \times 10^{15}$ cm^{-3}).

Figure 5 shows the effects of structure parameters on BV for the proposed CI PSOI. Figure 5(a) shows the effects of $N_{\rm n^+}$ on BV, $E_{\rm I,P}$ and the maximal hole concentration $N_{\rm h,m}$. It can be seen that when $N_{\rm n^+}$ is larger than 2×10^{18} cm^{-3}, BV is invariable, as are $E_{\rm I,P}$ and $N_{\rm h,m}$. When $N_{\rm n^+}$ is less than 2×10^{18} cm^{-3}, BV decreases as $N_{\rm n^+}$ decreases, which can be explained as follows: when $N_{\rm n^+}$ is larger than 2×10^{18} cm^{-3}, the n$^+$-regions under the drain are undepleted and the ionized donors are invariable, which is independent of $N_{\rm n^+}$, and therefore, inversion holes fixed by the force from the ionized donors as shown in Fig. 1(b) are invariable with $N_{\rm n^+}$, as is $E_{\rm P,I}$, which results in a changeless BV. However, when $N_{\rm n^+}$ is less than 2×10^{18} cm^{-3}, the n$^+$-regions under the drain are fully depleted, that is to say, the concentration of the ionized donors is equal to $N_{\rm n^+}$, and therefore, $N_{\rm h,m}$ and $E_{\rm I,P}$ decrease as $N_{\rm n^+}$ decreases, which leads to a diminishing BV as shown in Fig. 5(a). We define $N_{\rm n^+,c} = 2 \times 10^{18}$ cm^{-3} as the critical $N_{\rm n^+}$ for the highest BV, and in order to obtain a perfect BV, $N_{\rm n^+}$ should be adequately higher than $N_{\rm n^+,c}$. Figure 5(b) shows the effects of $t_{\rm C}$, $L_{\rm E}$, $L_{\rm H}$ and $L_{\rm d}$ on BV. It can be seen from Fig. 5(b) that there is a maximum BV=631 V with $t_{\rm C} = L_{\rm E}$=0.5 μm and $L_{\rm H} = 2$ μm, and BV is improved with the increase of $L_{\rm d}$ which breaks through the BV limitation of the conventional PSOI just as shown in Fig. 5(b). Moreover, when $t_{\rm C}$ or $L_{\rm E}$ is 0 μm, CI PSOI becomes a conventional PSOI whose BV is only 246 V. Figure 5(c) shows the effects of the p-top layer and the substrate concentrations ($N_{\rm sub}$). The maximal BVs are almost equal for different p-top layer thicknesses ($t_{\rm p}$) of 0.5, 1 and 1.5 μm. In addition, the maximal BVs appear when $N_{\rm p} \times t_{\rm p}$ is about 1.5×10^{12} cm^{-2} which satisfies the RESURF (REduced SURface Field) condition, and after that, BV sharply decreases because of premature breakdown at the n$^+$–p junction

on the drain side. N_{sub} has a faint influence on BV, and BV only decreases by 4.07% when N_{sub} increases from 1×10^{14} cm^{-3} to 1×10^{15} cm^{-3}. Figure 5(d) gives the effects of silicon window length L_W on voltages and hole concentrations under the drain. Although the voltage shared by the substrate layer V_{sub} slowly increases because the depletion layer extends into the substrate with a sustained V_S (voltage shared by the top silicon layer), BV decreases with the increase of L_W, resulting from the greater decrease of the voltage shared by the dielectric buried layer V_I due to the reduction of the maximal interface hole concentration $N_{h,m}$ under the drain and therefore, the decrease of $E_{I,P}$ given by Eq. (11).

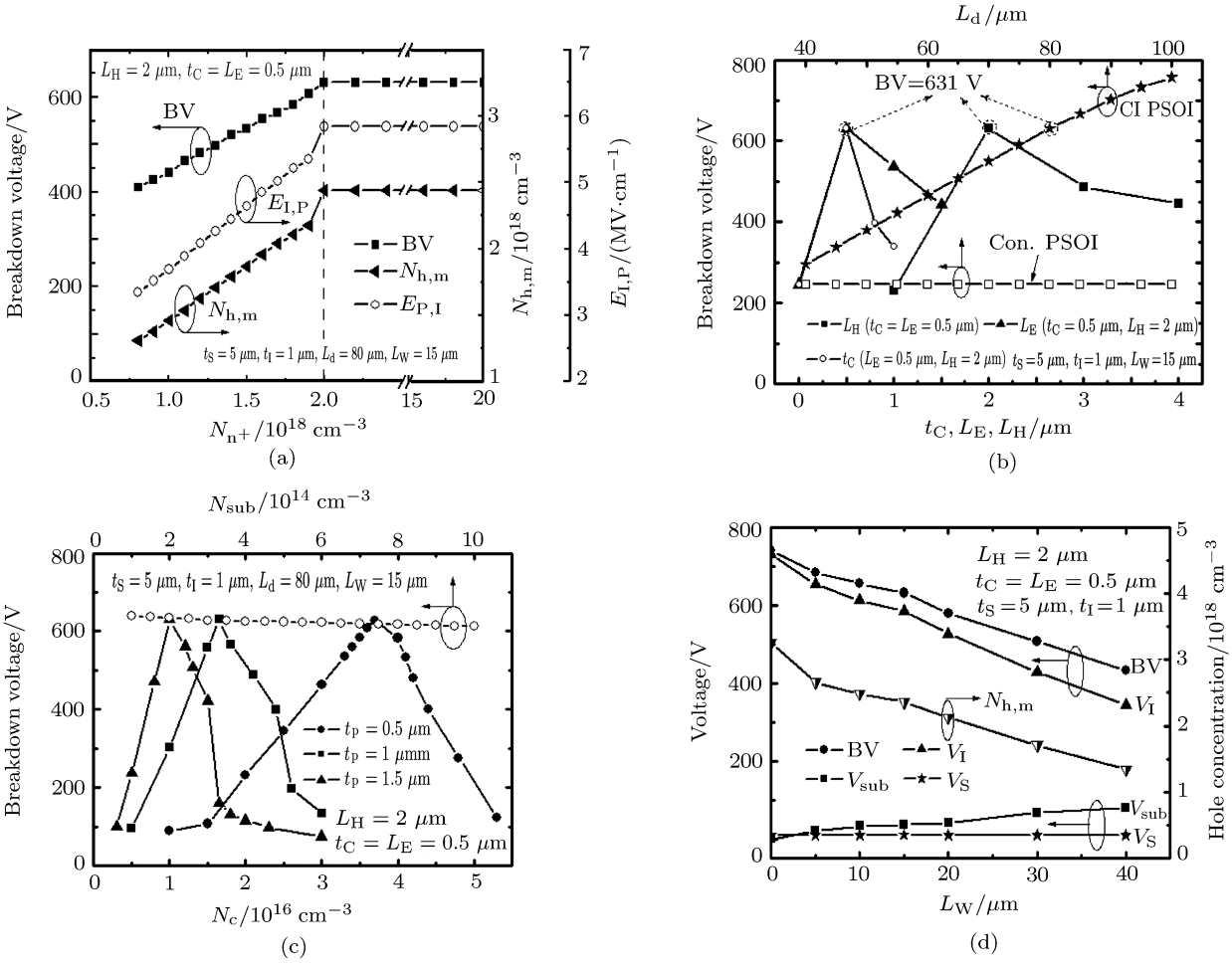


Fig. 5. Effects of device parameters on breakdown voltage. t_S = 5 μm, t_I = 1 μm, t_{sub} = 30 μm for all. Panel (a) shows N_{n+} on BV, $E_{I,P}$ and the maximal hole concentration $N_{h,m}$. Panel (b) exhibits t_C, L_E, L_H and L_d on breakdown voltage. L_d = 80 μm for t_C, L_E, and L_H. t_C = L_E = 0.5 μm and L_H = 2 μm for L_d. $N_{sub} = 3 \times 10^{14}$ cm^{-3} for all. Panel (c) displays N_p (with $N_{sub} = 3 \times 10^{14}$ cm^{-3}) and N_{sub} on breakdown voltage. t_C = L_E = 0.5 μm, L_H = 2 μm and L_d = 80 μm for all. Panel (d) gives silicon window length L_W on voltages and hole concentration under the drain. t_C = L_E = 0.5 μm, L_H = 2 μm,L_d = 80μm, and $N_{sub} = 3 \times 10^{14}$ cm^{-3} for all.

Figure 6 gives the thermal characteristics of the CI PSOI, the conventional PSOI and SOI. The bottom of the substrate is held at 300 K, and the gate voltage (V_g) is 15 V for all simulations. With a V_d of 30 V, it can be seen that the surface temperature of the CI PSOI is the lowest and its maximal temperature T_{max} is 303.39 K, but that of the conventional SOI is the highest and its T_{max} is 318.30 K. Moreover, the situations of T_{max} of the CI PSOI and the conventional PSOI are under the drain due to the existence of silicon windows under the source, whereas that of the conventional SOI is under the source, which can be seen more clearly from Figs. 6(b) and 6(c). It can be concluded that the proposed CI PSOI can enhance the breakdown voltage while maintaining a lower SHE.

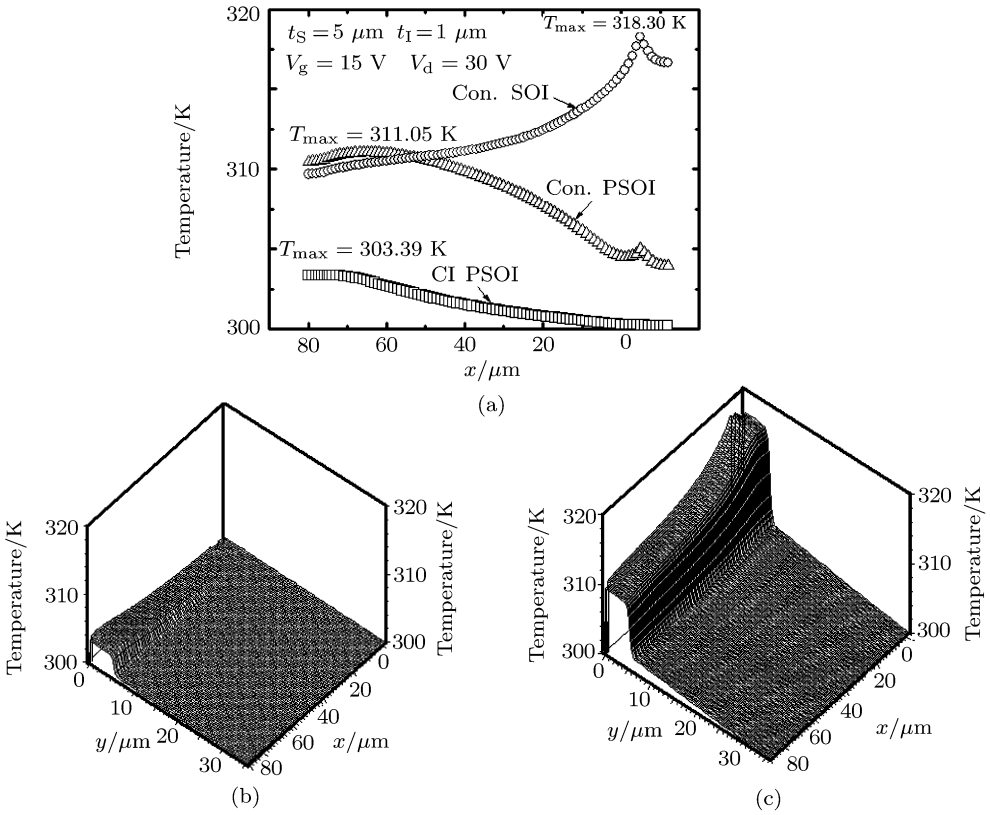


Fig. 6. Thermal characteristics with $V_d = 30$ V and $V_g = 15$ V. The device parameters are the same as those in Fig. 4. Panel (a) shows surface temperature profiles ($y = 0.001\ \mu m$) for the CI PSOI, the conventional PSOI and SOI. Panel (b) indicates three-dimensional temperature profiles of the CI PSOI. Panel (c) exhibits three-dimensional temperature profiles of the conventional SOI.

4. Conclusion

A novel interface charge island structure of a high voltage device on partial-SOI (CI PSOI) and its analytical model for the interface electric field are proposed in this paper. Utilized in the CI PSOI effectively is the enhancement effect of the interface charges on the electric field of the dielectric buried layer to increase breakdown voltage while alleviating the self-heating effect by a silicon window under the source. The BV for the CI PSOI increases by 156.5% and 223.6% while the maximal temperature at $V_g = 15$ V and $V_d = 30$ V reduces by 7.66 K and 14.91 K in comparison with those for the conventional PSOI and SOI devices, respectively. The proposed CI-structure is a brand-new concept for SOI/PSOI high voltage devices to accumulate and utilize the interface charges.

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