SiC epitaxial layers grown by chemical vapour deposition and the fabrication of Schottky barrier diodes*

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This paper presents the results of unintentionally doped 4H-SiC epilayers grown on n-type Si-faced 4H-SiC substrates with 8° off-axis toward the [11$\bar{2}$0] direction by low pressure horizontal hot-wall chemical vapour deposition. Growth temperature and pressure are 1580 °C and 10^4 Pa, respectively. Good surface morphology of the sample is observed using atomic force microscopy (AFM) and scanning electron microscopy (SEM). Fourier transform infrared spectroscopy (FTIR) and x-ray diffraction (XRD) are used to characterize epitaxial layer thickness and the structural quality of the films respectively. The carrier concentration in the unintentional 4H-SiC homoepitaxial layer is about 6.4×10^{14} cm^{-3} obtained by C–V measurements. Schottky barrier diodes (SBDs) are fabricated on the epitaxial wafer in order to verify the quality of the wafer and to obtain information about the correlation between background impurity and electrical properties of the devices. Ni and Ti/4H-SiC Schottky barrier diodes with very good performances were obtained and their ideality factors are 1.10 and 1.05 respectively.

Keywords: 4H-silicon carbide, low pressure horizontal hot-wall chemical vapour deposition, atomic force microscope, scanning electron microscopy

PACC: 6855, 8115H ,7360, 7870C

1. Introduction

In recent years there has been increasing interest and research on SiC, because it is a wide band gap semiconductor with excellent features such as high critical breakdown field and high thermal conductivity to have a great benefit on applications of high power and high frequency at high temperatures.[1−6] In power applications, such as PiN power devices, a lightly doped I-SiC layer can be used for achieving very high blocking voltages up to more than twenty thousand volts.[7−9] The growth of very low-doped epilayers is still an attractive issue, because the normal way to improve the blocking voltage is to increase the thickness of the buffer layer. Morever, for high frequency application of metal semiconductor field effect transistor (MESFET) devices a technological solution of a compensated semi-insulating epilayer, i.e., an I layer, is used,[10] or high purified substrates or semi-insulated substrates are adopted.[11]

It is obvious that the technique for unintentionally doped epilayers with low impurity concentration becomes very important. In order to achieve high quality SiC epilayers, there are various factors to be concerned with,[12] such as type of substrates, cleaning procedure, substrate susceptor, reactor dimensions, orientations, and so on. Regarding the graphite substrate susceptor, we must protect it by rigid metal carbide, i.e. TaC, to prevent carbon escape from the susceptor, otherwise the growth or quality may be out of control.

For high quality SiC devices, low defect levels and high crystal quality epilayers are basically required. Therefore, optimized conditions are necessary to decrease carrot type defects, pits, screw dislocations, and triangular shape defects with inclusion of 3C-SiC, which degrade the performance of the reverse bias.[13] The epitaxial growth on the SiC substrates has led not only to dissociation of micro-pipes into screw dislocations but also suppression of the defect level concentration towards the growth direction, as the thickness increases.[14]

2. Epitaxial growth and characterization

Homoepitaxial growth was carried out in the reactor by using the $SiH_4/C_3H_8/H_2$ system, which is a commercial low-pressure, hot-wall CVD (LP-HW-

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CVD) reactor (Epigress VP508 system). The SiC epitaxial layers were grown on the Si-faced (0001) 4H-SiC substrates with 8° off axis, inclined toward [11$\bar{2}$0], purchased from the SiCrystal.AG. After substrate surface etching at 1400 °C for 10 min in H_2 and C_3H_8 flow, high purity industrial grade H_2, the carrier gas with a flow rate of 90 l/min was used for the growth of epitaxial layers keeping the reactor pressure at 10^4 Pa, while the growth temperature and growth time were 1580 °C and 2 hours respectively. The flow rates of SiH_4 and C_3H_8 used as source gases were maintained to have a C/Si ratio of 1.5 in the gas phase. The growth rate was about 5 μm/h. The process flow chart is shown in Fig. 1.

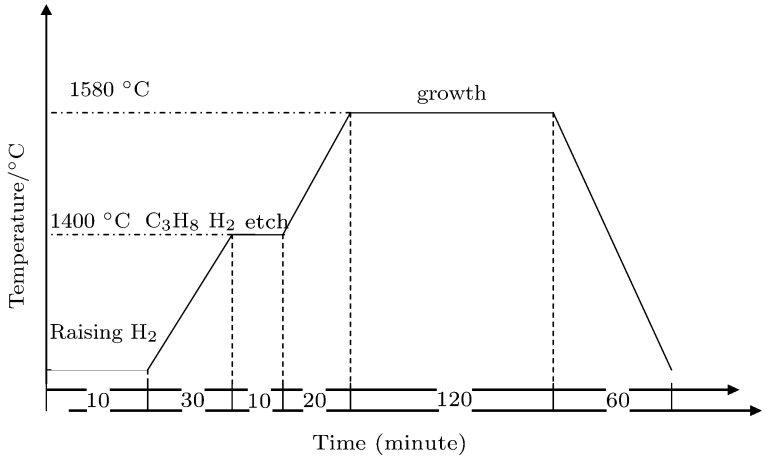


Fig. 1. The process flow chart.

The crystal of the 4H-SiC epilayer was evaluated by using XPert MPD PRO. Figure 2 shows a typical x-ray diffraction (XRD) width scan between 20°–60° for the epilayer sample. One strong peak diffraction from the (0004) planes of 4H-SiC is at 35.608 °C. No other peak is found beside 35.608 °C on the (0004) planes, which is in accordance with the standard map of Ref. [15].

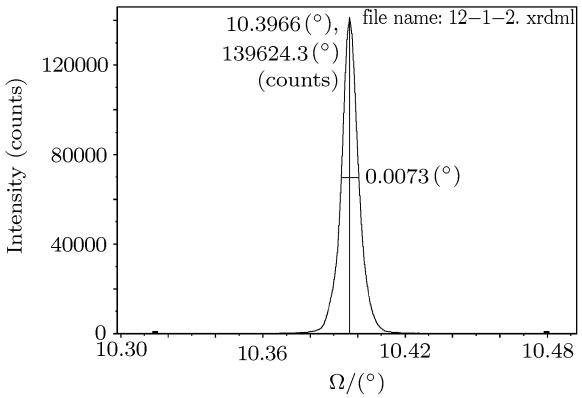


Fig. 2. The XRD pattern for a 10 μm thick 4H-SiC epilayer with FWHM 0.0073°.

As shown in this figure, one very sharp and symmetrical peak shows that the full width at half maximum (FWHM) is in 0.0073°, which is comparable to that in Ref. [16]. This indicates that the epilayer has good 4H-SiC crystalline structure.

Figures 3 and 4 show the surface morphology of 4H-SiC epilayers grown on 8° off-axis Si (0001), observed by scanning electron microscopy (SEM) and atomic force microscopy (AFM) respectively.[17] From Fig. 3, it is clear that the surface of the epilayers is very smooth without macro-steps. Figure 4 shows an AFM image of the 4H-SiC epilayer with a size of 10 μm×10 μm with the RMS 0.27 nm.

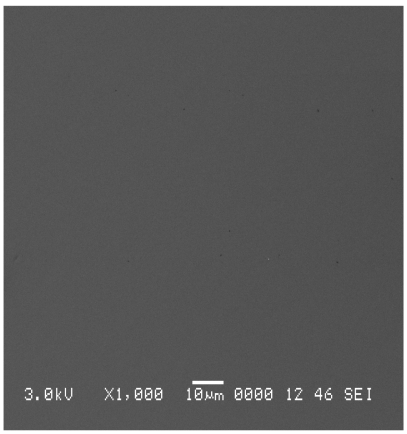


Fig. 3. SEM images of the 4H-SiC epilayer.

It is well known that the height of a single double-layer of Si and C atoms is 0.25 nm that is stacked in the

c-direction to form the various SiC polytypes. This result would lead us to conclude that an atomically flat and damage free SiC surface, ideal for epitaxial growth, has been obtained.

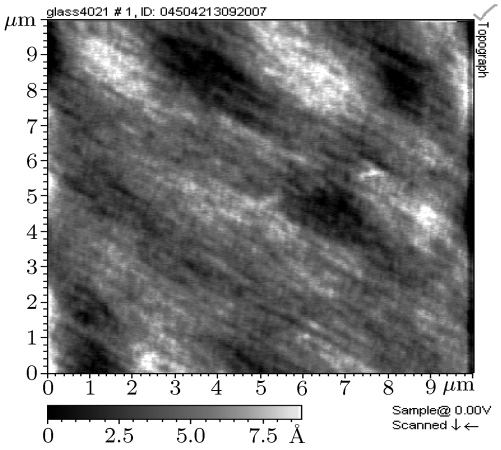


Fig. 4. AFM images of the 4H-SiC epilayer surfaces.

The infrared reflectance spectra were measured to evaluate the thickness of the epilayer at room temperature (RT) using Fourier transform infrared (FTIR) spectrometry, PerkinElmer Spectrum100 for the infrared spectral region (350–7800 cm^1). The measurements were performed in the infrared range from 400 cm^{-1} to 4500 cm^{-1} using a KBr beam splitter and a deuterated triglycine sulfate detector with KBr window, in which a high intensity ceramic light source, a beam splitter, and a mercury cadmium telluride detector were used. The reflectance data were collected at an angle of incidence of 16 degrees, and an aluminium mirror was used as a reference. The 9-point measure pattern is adopted as shown in Fig. 5.

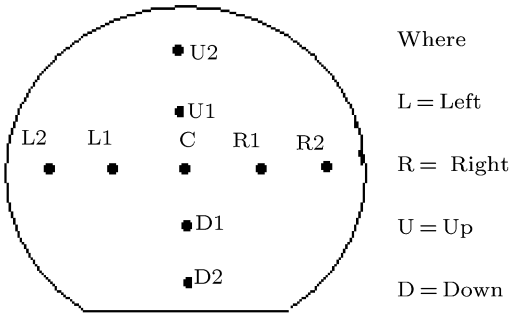


Fig. 5. The 9-point measure pattern, where C, L, R, U and D represent central, left, right, up and down respectively, indicating the measurement locations.

Table 1 shows the uniformity of the epitaxial layer. Selected 9-point pattern areas were used to test the depth. The FTIR data have confirmed a very uniform depth with a (max–min)/(max+min) uniformity of 1.74% by σ/mean. The mean depth of the epilayer is about 10.2 μm, and the different batches have shown repeatable results.

Table 1. Unintentional epitaxial layer thickness of a 9-point pattern measured by FTIR.[17]

sample	point	C	L1	L2	R1	R2	U1	U2	D1	D2	mean	σ/mean
No. 1	depth/μm	10.205	10.197	10.345	10.3	10.3	10.386	10.771	10.24	10.2	10.327	1.74%
No. 2	depth/μm	10.07	10.147	10.6	10.126	10.36	10.154	10.55	10.05	10.276	10.259	1.99%
No. 3	depth/μm	9.944	9.885	9.97	10.016	10.27	9.959	10.2	9.904	9.97	10.013	1.32%

3. Schottky barrier diode (SBD) fabrication and measurement

The samples were cleaned by a standard RCA cleaning process, followed by HF and acetone treatment. Electron beam evaporated Ni/Pt(450/50 nm) was implemented for full area backside and annealed at 1000 °C in N_2 for 2 min to form ohmic contacts, and then electron beam evaporated Cr/Au(50/200 nm) was processed on the top side. Circular Schottky contacts were formed by electron beam evaporating Ni/Cr/Au or Ti/Cr/Au (200/50/200 nm) and patterned by lift off with a diameter of 1.3 mm. The Ti and Ni were chosen in our studies because they are the most widely used metals for Schottky contacts in commercial SiC devices. The structure of an SBD investigated in this paper is shown in Fig. 6.

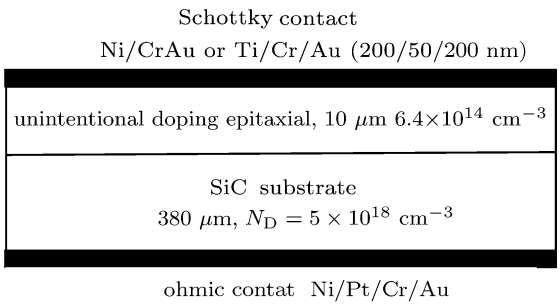


Fig. 6. Cross section of epitaxial 4H-SiC SBD.

C–V measurement

The capacitance–voltage (C–V) measurements of the Ni and Ti/4H-SiC SBD were conducted by using a Keithley 590 C–V analyser at frequencies of 1 MHz and a voltage sweep of −20–1 V. Based on the data of C–V mearuemnet, the ionized doping concentration, i.e., free carrier concentration, calculated with Eq. (1)[1)], is shown in Fig. 7, in which quasistatic and high-frequency capacitances are used to minimize errors caused by interface states.

$$N = \frac{(-2\times10^{-24})[(1-C_{\rm Q}/C_{\rm ox})/(1-C_{\rm H}/C_{\rm ox})]}{A^2 q\varepsilon_{\rm S}} \times \left[\frac{\rm d}{{\rm d}V_{\rm GS}}\left(\frac{1}{C_{\rm H^2}}\right)\right]^{-1}, \quad (1)$$

where N is the ionized doping concentration ($\rm cm^{-3}$), in other words, it stands for the free carrier concentration. $C_{\rm Q}$, $C_{\rm ox}$, $C_{\rm H}$ are quasistatic capacitance (pF), oxide capacitance (pF) and high-frequency capacitance (pF) respectively. A is the gate area ($\rm cm^{-2}$), q is the electron charge, $\varepsilon_{\rm s}$ is the dielectric constant of the substrate material, and $V_{\rm GS}$ is the gate substrate voltage.

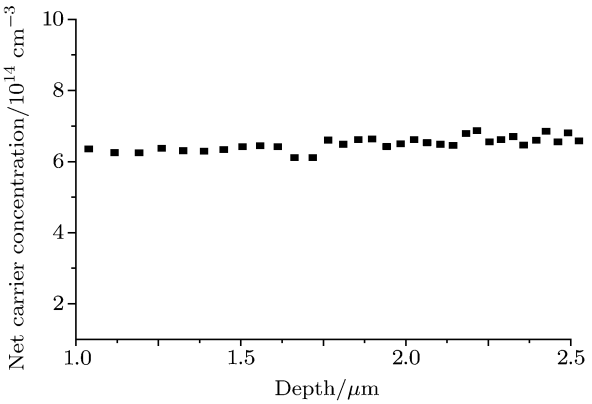


Fig. 7. Profile of free carrier concentration with depth.

As can be seen from this figure, the depth profile of free carrier concentration extracted from C–V measurements is quite uniform and the net carrier concentration is approximately 6.4×10^{14} $\rm cm^{-3}$.

I–V measurement

The current–voltage (I–V) measurement was performed by using a Keithley 4200 semiconductor parameter analyser and probing station. Figure 8 exhibits the forward and reverse I–V characteristic curves. The turn-on voltage of the Ni and Ti/SiC SBD is approximately 1.44 V and 0.50 V respectively, and the reverse current at −200 V is 1.0×10^{-12} A (7.5×10^{-11} A·$\rm cm^{-2}$) and 6.6×10^{-11} A (5.1×10^{-9} A·$\rm cm^{-2}$) respectively. The Ni and Ti/SiC SBDs also show a very low reverse current and excellent rectifying characteristic.

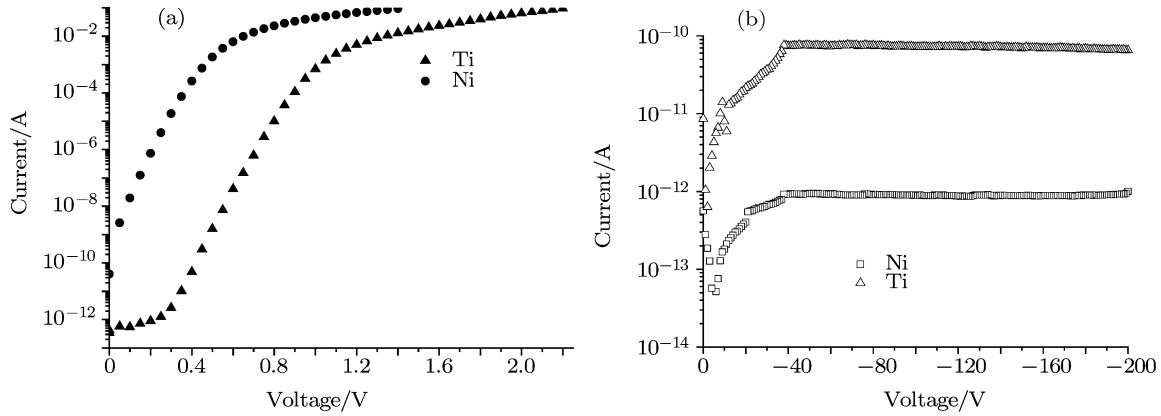


Fig. 8. Forward (a) and reverse (b) I–V characteristics of the Ni and Ti/4H-SiC SBD.

[1)] KEITHLEY Model 82-DOS Simultaneous C–V document

At a low forward voltage, using the thermionic emission theory, we can express the current running through the SiC Schottky diode as Eq. (2)

$$I = I_{\rm s} \exp\left(\frac{qV}{nkT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right], \qquad (2)$$

where $I_{\rm s}$ is the reverse saturation current obtained by the y-interception of the linear fitting curve of the linear area of the I–V curve in semilogarithmic plots, and they are 1×10^{-16} A and 8×10^{-9} A for Ni and Ti/SiC SBDs respectively. A^* is the effective Richardson's constant (150 A·cm^{-2}·K^{-2}), and n is the ideality factor. The ideality factor can be given by Eq. (3)

$$n = \frac{q}{kT}\frac{\partial V}{\partial {\rm In}I}. \qquad (3)$$

The Schottky barrier height $\phi_{\rm B}$ is obtained from Eq. (4)

$$I_{\rm s} = AA^*T^2 \exp\left(-\frac{q\phi_{\rm B}}{kT}\right). \qquad (4)$$

In Eq. (2), it should include the image force and tunnelling effects to lower the Schottky barrier, so the Schottky barrier height extracted from the I–V curve is underestimated.

If the forward voltage is larger than the threshold voltage, the forward current through the SiC Schottky diode can be expressed in Eq. (5) in which the effect of series resistance is included

$$I = AA^*T^2 \exp\left(-\frac{q\phi_{\rm B}}{kT}\right)\left\{\exp\left[\frac{q}{nkT}(V - IR_{\rm s})\right] - 1\right\}, \qquad (5)$$

where $R_{\rm s}$ is the series resistance and it is expressed by Eq. (6)

$$R_{\rm s} = \left(1 - \frac{\partial {\rm In}I}{\partial V}\frac{nkT}{q}\right)\Big/\left(\frac{\partial I}{\partial V}\right). \qquad (6)$$

Using the thermionic emission model mentioned above, we find that the ideality factor is $n = 1.10$ and 1.05, the Schottky barrier height $\phi_{\rm B}$ is 1.27 eV and 0.86 eV, and the series resistance $R_{\rm s}$ is 6.71 Ω and 5.79 Ω for Ni and Ti/SiC SBDs respectively.

4. Conclusion

A high quality unintentionally doped n type 4H-SiC homoepitaxial layer is obtained using by an LP-HW-CVD reactor, and a free carrier concentration as low as 6.4×10^{14} cm^{-3} is achieved. Excellent morphological and structural properties of 4H-SiC epitaxial layers have been observed. With the 4H-SiC epilayers, Ni and Ti/4H-SiC Schottky barrier diodes were fabricated to further verify the quality of epitaxial layers of 4H-SiC. Measurement results demonstrate that the Ni and Ti/4H-SiC SBDs have perfect characteristics with turn-on voltages of 1.44 V and 0.50 V, reverse current densities of 7.5×10^{-11} A/cm^2 and 5.1×10^{-9} A/cm^2 at −200 V, an ideality factor (n) of 1.10 and 1.05, and a Schottky barrier height ($\phi_{\rm B}$) of 1.27–1.44 eV and 0.86–0.92 eV, respectively.

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