Electrical characteristics of SiGe-on-insulator nMOSFET and SiGe-silicon-on-aluminum nitride nMOSFET*

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This paper investigates the electrical characteristics and temperature distribution of strained Si/SiGe n-type metal oxide semiconductor field effect transistor (nMOSFET) fabricated on silicon-on-aluminum nitride (SOAN) substrate. This novel structure is named SGSOAN nMOSFET. A comparative study of self-heating effect of nMOSFET fabricated on SGOI and SGSOAN is presented. Numerical results show that this novel SGSOAN structure can greatly eliminate excessive self-heating in devices, which gives a more promising application for silicon on insulator to work at high temperatures.

Keywords: electrical characteristics, self-heating effect, SiGe-on insulator, SiGe-silicon-on-aluminum nitride

PACC: 7340Q, 7300A, 7360H

1. Introduction

Device scaling is recognized globally to improve the performance of complementary metal–oxide semiconductor (CMOS) devices. In particular, as the feature size is reduced to nanoscale, enhancement of devices performance is no longer proportional to the gate length due to the short channel effect and the great leakage current.[1] The capacity of gate control over the channel shrinks with geometry scaling down. The schemes which increase doping concentration and vertical electric field are proposed to reduce the parasitic effect.[2] However these approaches degrade the carrier mobility because of impurity and high-field saturation. In recent years, innovative materials and device structures are investigated to solve these problems.

There are two methods available. One of them is to introduce the stress in channel region to enhance the carrier mobility.[3−5] Another method is silicon on insulator (SOI) technology which acts as a novel isolation technology. Especially the ultra-thin body SOI metal–oxide semiconductor field effect transistor (MOSFET) is giving a promising structure, which can diminish short channel effect without a heavily doping channel. In addition, combination of strained silicon material and SOI structure offers significant performance enhancement over the conventional bulk silicon MOSFETs and SOI MOSFETs, which includes faster switching time, reduced power consumption, lower voltage operation and reduced short channel effect.[6,7]

However, one of the major issues related to strained-Si SOI MOSFETs is the self-heating effect. The thermal conductivity of SiGe alloy (about 5–10 W/m·K) fabricated on the silicon substrate and SiO_2 (1.4 W/m·K) is much smaller than the bulk silicon thermal conductivity (145 W/m·K).[8,9] A comparative study of self-heating effect on electron mobility in nanoscale strained SOI and strained silicon grown on relaxed SiGe-on-insulator nMOSFET is presented by Seong Je Kim.[10] In the case of strained-Si SGOI nMOSFET, we consider the self-heating effect in the thickness range from 5 nm to 10 nm, the mobility degradation of strained-Si SGOI nMOSFET is slightly higher than that of strained-Si SOI nMOSFET. Because of excessive self-heating, it is difficult to expand the application of SGOI MOSFETs to high temperature operation.

A solution to the self-heating problem of SGOI MOSFETs is to introduce a new kind of insulator

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which has higher thermal conductivity as the buried layer. Aluminum nitride (AlN) has excellent advantages of high thermal conductivity (285 W/m·K), high resistance (over 10^{14} Ω·cm) and a coefficient of thermal expansion close to that of silicon (about 4.5×10^{-6} °C versus $3.5\sim4\times10^{-6}$ °C). Thus, using AlN as a buried insulator can greatly remove the heat generation during the devices work.

Based on successful formation of silicon on aluminum nitride (SOAN) structure by ion-cut process,[11] a strained Si/SiGe layer is fabricated on SOAN substrate in this paper, which is called SGSOAN nMOSFET. A detailed electrical model including self-heating is provided. The electrical characteristics and temperature distribution of SGSOAN nMOSFET and SGOI nMOSFET are compared.

2. Structure design and simulation

Based on successful formation of SOAN structure by ion-cut process, an SGSOAN nMOSFET is proposed. The cross-sectional views of SGOI nMOSFET and SGSOAN nMOSFET are shown in Figs. 1(a) and 1(b) respectively. In these two devices, the thickness of buried layer is equal. The thickness of silicon buffer layer is 10 nm. The detailed parameters for simulated devices are shown in Table 1.

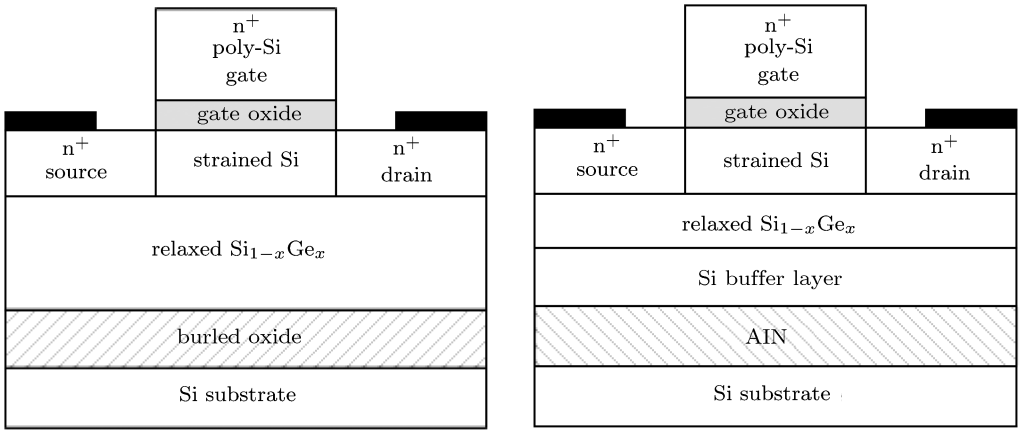


Fig. 1. Device structures simulated: (a) SGOI nMOSFET; (b) SGSOAN nMOSFET.

Table 1. The detailed structure parameters.

device parameters	SGOI (SiO_2)	SGSOAN (silicon/AlN)
n^+ source/drain doping	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
n^- source/drain extension doping	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
p^- silicon film doping	5×10^{17} cm^{-3}	5×10^{17} cm^{-3}
n^+ poly-Si doping	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
gate length	50 nm	50 nm
thickness of thin film	10 nm	10 nm
gate oxide thickness	4 nm	4 nm
channel thickness	10/60 nm	10/50/10 nm
insulator on the bulk silicon substrate	SiO_2 (100 nm)	AlN (100 nm)
p^- substrate doping	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Ge content in $Si_{1-x}Ge_x$	20%	20%

To obtain the electrostatic potential distribution, electron concentration and hole concentration, the following Possion's equation and electron and hole continuity equations must be solved:

$$\boldsymbol{\nabla}\cdot\varepsilon\boldsymbol{\nabla}\phi=-q(p-n+N_{\rm D}+N_{\rm A}), \tag{1}$$

$$\boldsymbol{\nabla}\cdot\boldsymbol{J}_n=qR_{+}q\frac{\partial n}{\partial t}, \tag{2}$$

where ε is the electrical permittivity, q is the electronic charge, n and p are the electron concentration and hole concentration respectively, $N_{\rm D}$ is the concentration of ionized donors, $N_{\rm A}$ is the concentration of ionized acceptors, R is the electron–hole recombination rate.

For nanometer SOI devices, the channel thickness becomes very thin and the channel width has reached the quantum scale, the quantization effect must be included. When we take the quantum effect into consideration, an extra potential-like parameter Λ is included into the classical concentration formula.

$$n = N_{\rm C} \exp\left(\frac{E_{{\rm F}_n} - E_{\rm C} - \Lambda}{kT}\right), \tag{3}$$

where k is Boltzmann constant, T is the carrier temperature, $N_{\rm C}$ is the conduction band density of state, $E_{\rm C}$ is the conduction band energy, and $E_{{\rm F}_n}$ is the electron Fermi energy. In the simulation, a density gradient model is adopted.

For the biaxial tension, the strain in silicon is caused by the lattice mismatch of silicon with relaxed SiGe, which leads to an energy splitting in the energy band by an upward shifting of four valleys and a lowering of two others.[8] Strain effects on the silicon band structure are given by[1]

$$(\Delta E_{\rm c})_{\rm s-Si} = 0.57x, \tag{4}$$

$$(\Delta E_{\rm g})_{\rm s-Si} = 0.4x, \tag{5}$$

where x is the Ge mole content in the $Si_{1-x}Ge_x$ layer, and it ranges from 0 to 1, $(\Delta E_{\rm c})_{\rm s-Si}$ is the reduction of electron affinity in silicon caused by the strain, $(\Delta E_{\rm g})_{\rm s-Si}$ is the reduction of bandgap in silicon caused by strain. The band structure parameters for $Si_{1-x}Ge_x$ layer are shown as follows:

$$N_{\rm v,SiGe} = (0.6x + 1.04(1-x) \times 10^{19}\ {\rm cm}^{-3}, \tag{6}$$

$$\varepsilon_{\rm SiGe} = 11.8 + 4.2x, \tag{7}$$

$$(\Delta E_{\rm g})_{\rm SiGe} = 0.467x, \tag{8}$$

where $(\Delta E_{\rm g})_{\rm SiGe}$ is the reduction of $Si_{1-x}Ge_x$ bandgap, $N_{\rm v,SiGe}$ is the valence band density of states of $Si_{1-x}Ge_x$, and $\varepsilon_{\rm SiGe}$ is the permittivity of $Si_{1-x}Ge_x$.

For nanoscale devices, the conventional drift-diffusion equation is not suitable to describe the carrier transport mechanism, which neglects the local effect such as the velocity overshoot and overestimates the impact ionization generation rate. A hydrodynamic model accounted for energy transport of carriers in transport equation must be adopted. To obtain the temperature distribution in the simulated device, a lattice heat flow equation must be solved for each material involved in the device,

$$C_{\rm L}\frac{\partial T_{\rm L}}{\partial t} = \nabla(\kappa_1 \nabla T_{\rm L}) + H, \tag{9}$$

where $T_{\rm L}$ is the local lattice temperature, $C_{\rm L}$ is the lattice heat capacity, κ_1 is the thermal conductivity, and H is the thermal generation coefficient, a simple form of H can be written as[8]

$$H = (\boldsymbol{J}_{\rm n} + \boldsymbol{J}_{\rm p}) \cdot \boldsymbol{E}, \tag{10}$$

where $\boldsymbol{J}_{\rm n}$ and $\boldsymbol{J}_{\rm p}$ are electron current density and hole current density respectively, $\boldsymbol{E}$ is the electric field.

Table 2 shows values of the heat capacity $C_{\rm L}$ and thermal conductivity κ for various materials in the simulated device at the room temperature 300 K.

Table 2. Values of the heat capacity $C_{\rm L}$ and thermal conductivity κ_1 for various materials in the simulated devices at the room temperature 300 K.[10]

material	$C_{\rm L}$(J/K·cm^3)	κ_1/(W/cm·K)
silicon	1.63	1.5
SiO_2	1.67	0.014
poly-Si	1.63	1.5
AlN	1.94	2.85
$Si_{1-x}Ge_x$	1.63 ∼ 1.67	0.6 ∼ 1.5

For the hydrodynamic model, electron current density and hole current density are given by

$$\begin{aligned}\boldsymbol{J}_{\rm n} = {} & q\mu_{\rm n}(n\nabla E_{\rm C} + kT_{\rm n}\nabla n + f_{\rm n}^{\rm td}kn\nabla T_{\rm n} \\ & - 1.5nkT\nabla \ln m_{\rm n}),\end{aligned} \tag{11}$$

$$\begin{aligned}\boldsymbol{J}_{\rm p} = {} & q\mu_{\rm p}(p\nabla E_V - kT_{\rm p}\nabla n - f_{\rm p}^{\rm td}kp\nabla T_{\rm p} \\ & -1.5pkT\nabla \ln m_{\rm p}),\end{aligned} \tag{12}$$

where $\mu_{\rm n}$ and $\mu_{\rm p}$ are electron mobility and hole mobility respectively. n and p are the electron concentration and hole concentration respectively, $T_{\rm n}$ and $T_{\rm p}$ are the electron temperature and hole temperature respectively. $m_{\rm n}$ and $m_{\rm p}$ are the electron effective mass and hole effective mass respectively. Both $f_{\rm n}^{\rm td}$ and $f_{\rm p}^{\rm td}$ are the fitting parameters. Among these four terms, the first term is the contribution of the spatial variation of the electrostatic potential, electron affinity and the bandgap. The second term considers the gradient of carrier concentration. The two remaining terms take into account the gradient of carrier temperature and the spatial variation of the effective masses $m_{\rm n}$ and $m_{\rm p}$. When we use the hydrodynamic model, the carrier temperature is assumed to be not equal to the

lattice temperature. In this simulation, the contribution of hole temperature to lattice temperature is very slight. In order to shorten the computational time, we assume that the hole temperature equals the lattice temperature. The hydrodynamic model is so complicated that its detailed form is not presented here. The full equations are provided in Ref. [12].

It is worth while noting that all these parameters depend on the temperature, and parameters set for $Si_{1-x}Ge_x$ depend on mole fraction. When x equals 0, C_L and κ are set to 1.63 J/K·cm^3 and 1.5 W/cm·K, respectively. When x equals 1, C_L and κ are set to 1.67 J/K· cm^3 and 0.6 W/cm·K, respectively.

3. Simulation results and discussion

To investigate the performance of SGSOAN structure, we compare the output characteristics, temperature distribution, subthreshold characteristics and the drain leakage current of SGSOAN nMOSFET with SGOI nMOSFET.

3.1. Output characteristics and temperature distribution

A comparison of I_d–V_{ds} characteristics for SGOI nMOSFET and SGSOAN nMOSFET is shown in Fig. 2. The gate bias is held at 1 V, 2 V, 3 V, 4 V, respectively. The drain bias is ramped up from 0 V to 5 V. When the gate bias is greater than 2 V, for SGOI nMOSFET, reduction of the drain current is caused by the self-heating effect occurs in the saturation region. Because the channel mobility reduces at high temperature. The higher the gate bias, the more serious the degradation becomes. On the contrary, for SGSOAN structure, it is difficult to observe the degradation of current output in saturation region, even for high gate bias of 4 V.

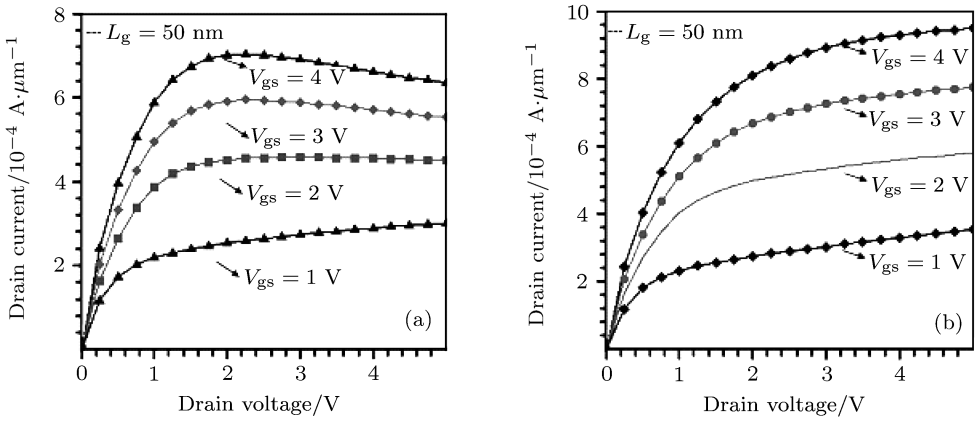


Fig. 2. Output characteristics: (a) regular structure SGOI nMOSFET; (b) novel structure SGSOAN nMOSFET.

In the case of the drain bias of 5 V and gate bias of 4 V, the temperature distribution in the device is extracted to test the impact of self-heating on performance of SGOI nMOSFET and SGSAON nMOSFET. The three-dimensional (3D) temperature distribution of the SGOI nMOSFET and SGSOAN nMOSFET are shown in Figs. 3(a) and 3(b) respectively. The horizontal and vertical profiles are presented by the x axis and y axis, respectively. The initial temperature of the device is assumed to be 300 K. In SGOI nMOSFET, the channel temperature rises to 540 K because of the excessive self-heating in the device, which is shown in Fig. 3(a). However, for SGSOAN nMOSFET, the temperature only increases to 330 K. It is clearly seen that the self-heating effect in SGSOAN nMOSFET is not so serious as that in SGOI nMOSFET. It is because the thermal conductivity of a buried oxide below a SiGe buffer layer has a low value of 1.4 W/m·K, which is two orders lower than that of silicon (145 W/m·K) and AlN (285 W/m·K) at room temperature. The majority of the heat generated in channel region is transferred into the silicon substrate through the buried AlN layer in the SGSOAN. Therefore, the slope for temperature distribution along y axis direction remains almost unchanged, as shown in Fig. 3(b).

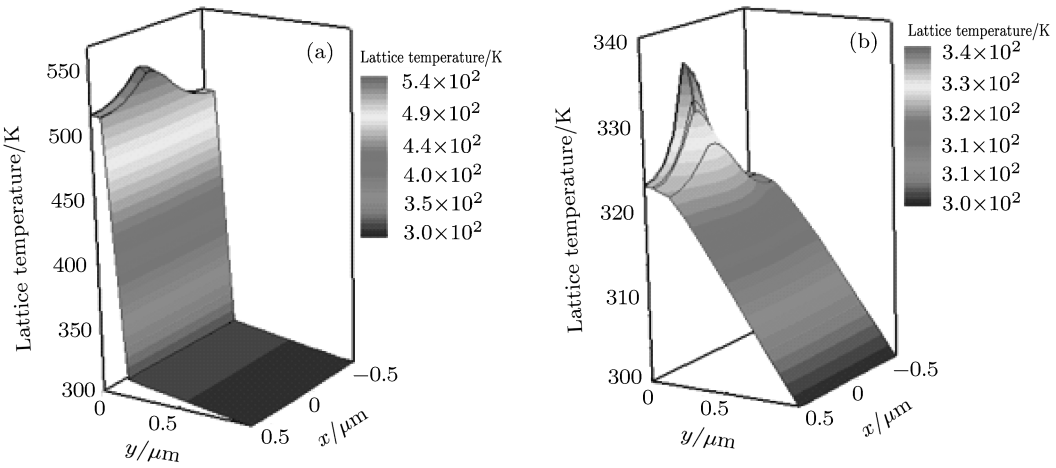


Fig. 3. Simulated 3D temperature distribution: (a) SGOI; (b) novel structure SGSOAN nMOSFETs.

3.2. Subthreshold characteristic

For the subthreshold characteristic simulation, the aim is to study how quickly the inversion layer is established. The drain bias is held at 0.05 V, and the gate bias is ramped up from 0 V to 1.2 V. The simulated threshold voltages in the SGOI nMOSFET and SGSOAN nMOSFET have the same values of 0.290 V using the maximum transconductance method. The subthreshold slopes of these two kinds of devices are 98.759 mV/dec and 98.791 mV/dec, respectively. The simulation results are shown in Fig. 4. From Fig. 4, we can find that there is almost no difference in the subthreshold characteristic between SGSOAN nMOSFET and SGOI nMOSFET. So it is feasible to replace the buried oxide layer with Si/AlN compound layers without changing the subthreshold characteristic of SGOI nMOSFET.

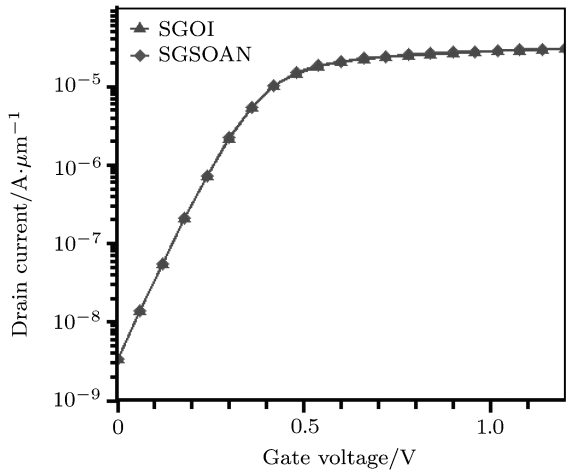


Fig. 4. Subthreshold characteristics of SGOI and SGSOAN nMOSFETs.

3.3. Drain leakage current

In this simulation, the gate bias is held at 0 V, and the drain bias is ramped in the range from 0 V to 3 V. The drain leakage current characteristics of SGOI nMOSFET and SGSOAN nMOSFET are shown in Fig. 5.

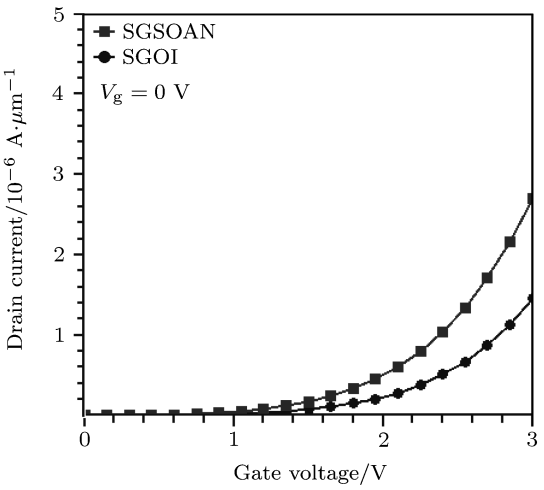


Fig. 5. Drain leakage current of SGOI and SGSOAN nMOSFETs.

For SGSOAN nMOSFET, the drain leakage current is slightly higher than that of SGOI nMOSFET. The result can be explained as follows. Before the inversion layer is established, the channel below the gate oxide and drain region can be equivalent to a p–n junction of reverse bias. Current through the p–n junction comes

from the electron–hole pair generation. Electron–hole pair generation depends on the electric field strength and the width of the space charge region. When the gate bias is held at 0 V, the drain and substrate can be seen as a parallel capacitance. The AlN and SiO_2 can be seen as dielectric materials in parallel capacitance, respectively. Due to higher permittivity 9.1 of AlN in comparison with 3.9 of SiO_2, a large great number of charges will be collected in drain if the identical drain bias is specified, which causes higher electrical field. The width of depletion charge region will be further increased, which induces more electron–hole pairs.

4. Conclusion

For the first time, a novel SGSOAN structure is proposed. The electrical characteristics of SGSOAN nMOSFET are analysed, which include the output characteristics, temperature distribution, subthreshold characteristics and drain leakage current. This paper presents a comparative study of electrical characteristics of nMOSFETs fabricated on SGOI nMOSFET and SGSOAN nMOSFET. The numerical simulation results show that the SGSOAN structure can greatly reduce the self-heating effect during the same working conditions. So this novel structure can expand the applications of SOI to high temperature.

References

[1] Venkataraman V, Nawal S and Kumar M J 2007 *IEEE Trans. Electron. Dev.* **54** 554

[2] Bufler F M and Fichtner W 2002 *Appl. Phys. Lett.* **81** 82

[3] Lin G J, Lai H K, Li C, Chen S Y and Yu J Z 2008 *Chin. Phys.* B **17** 34

[4] Tezuka T, Nakaharai S, Moriyama Y, Hirashita N, Sugiyama N, Tanabe A, Usuda K and Takagi S 2007 *IEEE Trans. Electron. Dev.* **54** 1247

[5] Lim S J, Shim T H, Choi K R and Park J G 2009 *Semicond. Sci. Technol.* **24** 305014

[6] Toshifumi I, Toshinori N and Tsutomu T 2006 *IEEE Trans. Electron. Dev.* **53** 2809

[7] Han R Q, Li D Y, Liu X Y, Sun L, Wang Y and Zhang S D 2007 *Chin. Phys.* **16** 240

[8] Yazdani K E, Yang Y Z and Asheghi M 2006 *IEEE Trans. Components and Packaging Tech.* **29** 254

[9] Zhang Z X, Lin Q, Zhu M and Lin C L 2004 *Ceramics International* **30** 1289

[10] Kim S J, Shim T H, Choi K R and Park J G 2009 *Semicond. Sci. Technol.* **24** 035014

[11] Zhu M, Chen P and Fu R K 2004 *IEEE Trans. Electron. Dev.* **51** 901

[12] Luan S Z and Liu H X 2008 *Chin. Phys.* B **17** 3077