An analytical threshold voltage model for dual-strained channel PMOSFET*

Qin Shan-Shan(秦珊珊)†, Zhang He-Ming(张鹤鸣), Hu Hui-Yong(胡辉勇), Dai Xian-Ying(戴显英), Xuan Rong-Xi(宣荣喜), and Shu Bin(舒 斌)

Key Laboratory of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an 710071, *China*

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Based on the analysis of vertical electric potential distribution across the dual-channel strained p-type Si/strained $Si_{1-x}Ge_x$/relaxd $Si_{1-y}Ge_y$(s-Si/s-SiGe/$Si_{1-y}Ge_y$) metal–oxide–semiconductor field-effect transistor (PMOSFET), analytical expressions of the threshold voltages for buried channel and surface channel are presented. And the maximum allowed thickness of s-Si is given, which can ensure that the strong inversion appears earlier in the buried channel (compressive strained SiGe) than in the surface channel (tensile strained Si), because the hole mobility in the buried channel is higher than that in the surface channel. Thus they offer a good accuracy as compared with the results of device simulator ISE. With this model, the variations of threshold voltage and maximum allowed thickness of s-Si with design parameters can be predicted, such as Ge fraction, layer thickness, and doping concentration. This model can serve as a useful tool for p-channel s-Si/s-SiGe/$Si_{1-y}Ge_y$ metal–oxide–semiconductor field-effect transistor (MOSFET) designs.

Keywords: strained Si, strained SiGe, dual-channel metal–oxide–semiconductor field-effect transistor (MOSFET), threshold voltage

PACC: 7340Q, 7360L

1. Introduction

With the improvement of the integration of integrated circuit (IC), and the devices being scaled down to nano scale, IC performance is approaching the physics limits. New technologies should be used to improve performances of the devices. Strain engineering has played an essential part of complementary metal-oxide semiconductor (CMOS) device design from the 90 nm technology node, for it offers device designers the ability to enhance carrier mobility and modify the band gap. Recently, researches about this strain engineering were reported in Refs. [1]–[8].

For metal–oxide–semiconductor field-effect transistor (MOSFET), threshold voltage is one of most important parameters. Its value directly affects the AC and the DC characteristics, subthreshold effect, and so on. In this paper, by analysing the distribution of electric potential across the device structure, the model of threshold voltage is established. And the maximum s-Si layer thickness is modeled for the buried channel inversion layer forming easier.

2. Device structure

While biaxially tensile strain significantly enhances electron mobility[5,6] and is used for advanced n-channel metal–oxide–emiconductor (NMOS) device, it does not offer a similar enhancement in hole mobility[7,8] for p-channel metal–oxide–semiconductor (PMOS) device. On the other hand, compressive strain in the channel enhances the hole mobility. As a result, a dual-channel CMOS device was proposed,[9−12] of which the schematic cross section of the structure shown in Fig. 1. A compressively strained $Si_{1-x}Ge_x$ (s-SiGe) layer and a tensile strained Si (s-Si) layer are subsequently grown on a relaxed $Si_{1-y}Ge_y$ ($x > y$) substrate. The energy band structure as shown in Fig. 1, has large valence band offsets at the s-Si/s-SiGe and s-SiGe/$Si_{1-y}Ge_y$ interfaces and a large conduction band offset at the s-Si/s-SiGe interface. This band structure can offer a higher hole mobility in buried PMOSFET and a higher electron mobility in n-channel metal–oxide–semiconductor field-effect transistor (NMOSFET) on a single substrate.

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†Corresponding author. E-mail: qinshan_003@163.com

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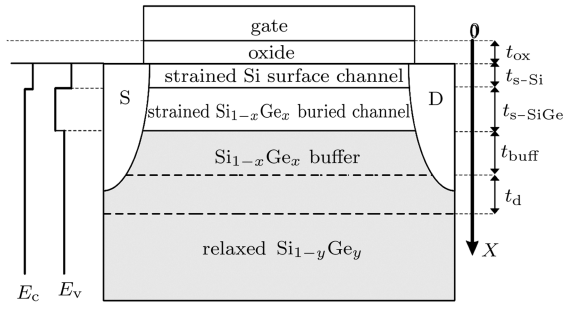


Fig. 1. Cross section of the dual-channel dual-strained PMOSFET.

The cross section of the MOSFET structure is shown in Fig. 1. In the analysis it is assumed that the tensile strained silicon layer, the compressively strained $Si_{1-x}Ge_x$ film and the relaxed $Si_{1-y}Ge_y$ buffer are undoped, and their thicknesses are $t_{s\text{-}Si}, t_{s\text{-}SiGe}, t_{buff}$ respectively. The doping concentration N_B in the n-type substrate is uniform. Ge fraction in the SiGe layer is constant.

3. Vertical electric potential distribution

The threshold voltage is related to the electric potential distribution on each layer in the vertical direction to the channel, which can be derived from Poisson's equation.

3.1. Relaxed $Si_{1-y}Ge_y$ depletion region

In the depletion region in the relaxed $Si_{1-y}Ge_y$ substrate, the Poisson's equation becomes:

$$\frac{d^2\Phi_1(x)}{dx^2} = -\frac{qN_B}{\varepsilon_y}, \quad (t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} \le x < t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} + t_d), \tag{1}$$

where $\Phi_1(x)$ is the electric potential, and ε_y is the permittivity of the relaxed $Si_{1-y}Ge_y$ substrate. The boundary condition is expressed as

$$E_1(t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} + t_d) = -\frac{d\Phi_1(x)}{dx}\Big|_{x=t_{ox}+t_{s\text{-}Si}+t_{s\text{-}SiGe}+t_{buff}+t_d} = 0, \tag{2}$$

where $E_1(x)$ is the electric field.

Performing the integration of Eq. (1), the electric field in this layer can be expressed as

$$\begin{aligned} E_1(x) = {} & \frac{qN_B}{\varepsilon_y}(x - t_{ox} - t_{s\text{-}Si} - t_{s\text{-}SiGe} - t_{buff} - t_d), \\ & (t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} \le x < t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} + t_d). \end{aligned} \tag{3}$$

Usually, potential is set to be zero at the substrate, thus $\Phi_1(t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} + t_d) = \Phi_{sub} = 0$. So, $\Phi_1(x)$ can be expressed as

$$\begin{aligned} \Phi_1(x) = {} & -\frac{qN_B}{2\varepsilon_y}(x - t_{ox} - t_{s\text{-}Si} - t_{s\text{-}SiGe} - t_{buff} - t_d)^2 + \Phi_1(t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} + t_d) \\ = {} & -\frac{qN_B}{2\varepsilon_y}(x - t_{ox} - t_{s\text{-}Si} - t_{s\text{-}SiGe} - t_{buff} - t_d)^2, \\ & (t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} \le x < t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff} + t_d). \end{aligned} \tag{4}$$

3.2. Relaxed $Si_{1-y}Ge_y$ buffer

It is also assumed that this layer is fully depleted. Under the depletion approximation condition, Poisson's equation can be expressed as

$$\frac{d^2\Phi_2(x)}{dx^2} = 0, \quad (t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} \le x < t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff}), \tag{5}$$

where $\Phi_2(x)$ is the electric potential in this relaxed $Si_{1-y}Ge_y$ buffer layer. According to the continuity of electric displacement, there is $E_2(t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff}) = E_1(t_{ox} + t_{s\text{-}Si} + t_{s\text{-}SiGe} + t_{buff})$. Using this boundary

condition, the electric field $E_2(x)$ is obtained as

$$E_2(x) = -\frac{\mathrm{d}\Phi_2(x)}{\mathrm{d}x} = -\frac{qN_\mathrm{B}}{\varepsilon_y}t_\mathrm{d}. \tag{6}$$

Base on electric potential continuity shown in the following equation:

$$\Phi_2(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}+t_\mathrm{buff}) = \Phi_1(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}+t_\mathrm{buff}) = -\frac{qN_\mathrm{B}}{2\varepsilon_y}t_\mathrm{d}^2, \tag{7}$$

the integration of Eq. (5) can be calculated, leading to the following equation:

$$\begin{aligned}\Phi_2(x) = &-\frac{qN_\mathrm{B}}{2\varepsilon_y}t_\mathrm{d}^2 + \frac{qN_\mathrm{B}t_\mathrm{d}}{\varepsilon_y}(x - t_\mathrm{ox} - t_\mathrm{s\text{-}Si} - t_\mathrm{s\text{-}SiGe} - t_\mathrm{buff}),\\ &(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe} \le x < t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}+t_\mathrm{buff}).\end{aligned} \tag{8}$$

3.3. Strained $Si_{1-x}Ge_x$ layer

Poisson's equation in this region can be written as

$$\frac{\mathrm{d}^2\Phi_3(x)}{\mathrm{d}x^2} = -\frac{\rho_x(x)}{\varepsilon_x}, \qquad (t_\mathrm{ox}+t_\mathrm{s\text{-}Si} \le x < t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}), \tag{9}$$

where $\Phi_3(x)$ is the electric potential, ε_x is the permittivity, and $\rho_x(x)$ is the charge density.

Supposing that $\rho_x(x) = 0$ when $|\Phi_3(x)| \le |\Phi_\mathrm{TH}|$, and $\rho_x(x) = qN_\mathrm{B}\exp\{-q[\Phi_\mathrm{TH} - \Phi_3(x)]/kT\}$ when $|\Phi_3(x)| > |\Phi_\mathrm{TH}|$, where Φ_TH is the electric potential when the inversion layer just emerges in the buried channel. According to the continuity conditions of displacement and electric potential along the interface, there exist $\varepsilon_x E_3(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}) = \varepsilon_y E_2(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe})$, and $\Phi_3(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}) = \Phi_2(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe})$, hence

$$E_3(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}) = E_{3,0} = -\frac{qN_\mathrm{B}}{\varepsilon_x}t_\mathrm{d}, \tag{10}$$

$$\Phi_3(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}) = \Phi_{3,0} = -\frac{qN_\mathrm{B}t_\mathrm{d}}{2\varepsilon_y}(t_\mathrm{d}+2t_\mathrm{buff}). \tag{11}$$

When $|\Phi_3(x)| \le |\Phi_\mathrm{TH}|$, using these boundary conditions to calculate the integration of equation (9) yields

$$E_{3,\mathrm{H}}(x) = -\frac{qN_\mathrm{B}}{\varepsilon_x}t_\mathrm{d}, \tag{12}$$

$$\Phi_{3,\mathrm{H}}(x) = \Phi_{3,0} + \frac{qN_\mathrm{B}t_\mathrm{d}}{\varepsilon_x}(x - t_\mathrm{ox} - t_\mathrm{s\text{-}Si} - t_\mathrm{s\text{-}SiGe}), \qquad (t_\mathrm{ox}+t_\mathrm{s\text{-}Si} \le x < t_\mathrm{ox}+t_\mathrm{s\text{-}Si}+t_\mathrm{s\text{-}SiGe}), \tag{13}$$

where $\Phi_{3,\mathrm{H}}(x)$ is the electric potential, and $E_{3,\mathrm{H}}(x)$ is the electric field.

When $|\Phi_3(x)| > |\Phi_\mathrm{TH}|$, using the boundary conditions (10) and (11) to calculate the integration of equation (9) gives

$$E_{3,\mathrm{S}}^2(x) - E_{3,0}^2 = \frac{2N_\mathrm{B}kT}{\varepsilon_x}\left[\exp\left(\frac{\Phi_\mathrm{TH} - \Phi_{3,\mathrm{S}}(x)}{kT/q}\right) - \exp\left(\frac{\Phi_\mathrm{TH} - \Phi_{3,0}}{kT/q}\right)\right]. \tag{14}$$

Solving Eqs. (14), Eq. (15) can be obtained as

$$E_{3,\mathrm{S}}(x) = -\frac{qN_\mathrm{B}t_\mathrm{d}}{\varepsilon_x}\sqrt{1+H(\Phi_3)}. \tag{15}$$

Here

$$H(\Phi_3) = \frac{2\varepsilon_x N_\mathrm{B}kT}{(qN_\mathrm{B}t_\mathrm{d})^2}\left[\exp\left(\frac{\Phi_\mathrm{TH} - \Phi_{3,\mathrm{S}}(x)}{kT/q}\right) - \exp\left(\frac{\Phi_\mathrm{TH} - \Phi_{3,0}}{kT/q}\right)\right], \tag{16}$$

$\Phi_{3,\mathrm{S}}(x)$ is the electric potential, and $E_{3,\mathrm{S}}(x)$ is the electric field.

At the interface between strained $Si_{1-x}Ge_x$ and strained Si, there exists

$$E_\mathrm{B} = E_{3,\mathrm{S}}(t_\mathrm{ox}+t_\mathrm{s\text{-}Si}) = -\frac{qN_\mathrm{B}t_\mathrm{d}}{\varepsilon_x}\sqrt{1+H(\Phi_\mathrm{B})}, \tag{17}$$

where $\Phi_\mathrm{B} = \Phi_{3,\mathrm{S}}(t_\mathrm{ox}+t_\mathrm{s\text{-}Si})$.

3.4. Strained Si layer

Poisson's equation in this region can be written as

$$\frac{\mathrm{d}^2\Phi_4(x)}{\mathrm{d}x^2} = 0, \quad (t_{\mathrm{ox}} \le x < t_{\mathrm{ox}} + t_{\text{s-Si}}). \tag{18}$$

This equation is solved in the following two cases.

1) When $|\Phi_3(x)| \le |\Phi_{\mathrm{TH}}|$, according to the continuity conditions of displacement and electric potential along the interface, there exist $\varepsilon_{\text{s-Si}}E_{4,H}(t_{\mathrm{ox}} + t_{\text{s-Si}}) = \varepsilon_x E_{3,\mathrm{H}}(t_{\mathrm{ox}} + t_{\text{s-Si}}+)$ and $\Phi_{4,\mathrm{H}}(t_{\mathrm{ox}} + t_{\text{s-Si}}) = \Phi_{3,\mathrm{H}}(t_{\mathrm{ox}} + t_{\text{s-Si}})$. Calculate the integration of Eq. (18), then we will obtain

$$E_{4,\mathrm{H}}(x) = -\frac{qN_{\mathrm{B}}}{\varepsilon_{\text{s-Si}}}t_{\mathrm{d}}, \tag{19}$$

$$\Phi_{4,\mathrm{H}}(x) = \Phi_{3,\mathrm{H}}(t_{\mathrm{ox}} + t_{\text{s-Si}}) + \frac{qN_{\mathrm{B}}t_{\mathrm{d}}}{\varepsilon_{\text{s-Si}}}(x - t_{\mathrm{ox}} - t_{\text{s-Si}}). \tag{20}$$

2) When $|\Phi_3(x)| > |\Phi_{\mathrm{TH}}|$, the boundary conditions are $\Phi_{4,\mathrm{S}}(t_{\mathrm{ox}} + t_{\text{s-Si}}) = \Phi_{\mathrm{B}}$ and $E_{4,\mathrm{S}}(t_{\mathrm{ox}} + t_{\text{s-Si}}) = (\varepsilon_x/\varepsilon_{\text{s-Si}})E_{\mathrm{B}} = -(qN_{\mathrm{B}}t_{\mathrm{d}}/\varepsilon_{\text{s-Si}})\sqrt{1 + H(\Phi_{\mathrm{B}})}$. Using the method above, Eqs. (21) and (22) can be obtained as

$$E_{4,\mathrm{S}}(x) = -\frac{\mathrm{d}\Phi_4(x)}{\mathrm{d}x} = -\frac{qN_{\mathrm{B}}t_{\mathrm{d}}}{\varepsilon_{\text{s-Si}}}\sqrt{1 + H(\Phi_{\mathrm{B}})}, \tag{21}$$

$$\Phi_{4,\mathrm{S}}(x) = \Phi_{\mathrm{B}} + \frac{qN_{\mathrm{B}}t_{\mathrm{d}}}{\varepsilon_{\text{s-Si}}}(x - t_{\mathrm{ox}} - t_{\text{s-Si}})\sqrt{1 + H(\Phi_{\mathrm{B}})}. \tag{22}$$

3.5. Gate oxide layer

In the ideal case, the fixed change destiny is zero. Thus Poisson equation can be written as

$$\frac{\mathrm{d}^2\Phi_5(x)}{\mathrm{d}x^2} = 0, \quad (0 \le x < t_{\mathrm{ox}}). \tag{23}$$

When $|\Phi_3(x)| \le |\Phi_{\mathrm{TH}}|$, using the method mention above, the electric field and electric potential can be obtained as

$$E_{5,\mathrm{H}}(x) = -\frac{qN_{\mathrm{B}}}{\varepsilon_{\mathrm{ox}}}t_{\mathrm{d}}, \tag{24}$$

$$\Phi_{5,\mathrm{H}}(x) = \Phi_{3,\mathrm{H}}(t_{\text{s-Si}} + t_{\mathrm{ox}}) - \frac{qN_{\mathrm{B}}t_{\mathrm{d}}}{\varepsilon_{\text{s-Si}}}t_{\text{s-Si}} + \frac{qN_{\mathrm{B}}t_{\mathrm{d}}}{\varepsilon_{\mathrm{ox}}}(x - t_{\mathrm{ox}}). \tag{25}$$

In the case of $|\Phi_3(x)| > |\Phi_{\mathrm{TH}}|$, the boundary condition is $E_{5,\mathrm{S}}(t_{\mathrm{ox}}) = (\varepsilon_{\text{s-Si}}/\varepsilon_{\mathrm{ox}})E_{4,\mathrm{S}}(t_{\mathrm{ox}}) = -(qN_{\mathrm{B}}t_{\mathrm{d}}/\varepsilon_{\mathrm{ox}}) \times\sqrt{1 + H(\Phi_{\mathrm{B}})}$, as a result, we obtain

$$E_{5,\mathrm{S}}(x) = -\frac{qN_{\mathrm{B}}t_{\mathrm{d}}}{\varepsilon_{\mathrm{ox}}}\sqrt{1 + H(\Phi_{\mathrm{B}})}, \tag{26}$$

$$\Phi_{5,\mathrm{S}}(x) = \Phi_{\mathrm{B}} - \frac{qN_{\mathrm{B}}t_{\mathrm{d}}}{\varepsilon_{\text{s-Si}}}(t_{\text{s-Si}})\sqrt{1 + H(\Phi_{\mathrm{B}})} + \frac{qN_{\mathrm{B}}t_{\mathrm{d}}}{\varepsilon_{\mathrm{ox}}}\sqrt{1 + H(\Phi_{\mathrm{B}})}(x - t_{\mathrm{ox}}). \tag{27}$$

4. Threshold voltage model

From Eqs. (25) and (27), the electric potential at the interface between s-Si/SiO_2: $\Phi_{5,\mathrm{H}}(0)$ and $\Phi_{5,\mathrm{S}}(0)$ can be figured out respectively. Hence, the gate voltage can be expressed as

$$V_{\mathrm{G}} = V_{\mathrm{FB}} + \Phi_{5,\mathrm{H}}(0)$$

and

$$V_{\mathrm{G}} = V_{\mathrm{FB}} + \Phi_{5,\mathrm{S}}(0), \tag{28}$$

where $V_{\rm FB} = (1/q)\left[\Phi_{\rm m} - (\chi_{\text{s-Si}} + E_{\text{g,s-Si}}/2)\right] - (kT/q)\ln(N_{\rm B}/n_{i,y}) - Q_{\rm ox}/C_{\rm ox}$ is the flat band voltage, with $\Phi_{\rm m}$ being the work function of the metal gate, $\chi_{\text{s-Si}}$ the electron affinity of s-Si, $n_{i,y}$ the intrinsic carrier concentration of the $Si_{1-y}Ge_y$ substrate, $Q_{\rm ox}$ and $C_{\rm ox}$ the oxide charges and capacitance respectively.

Let $V_{\rm TH}$ represent the gate voltage when the s-SiGe buried channel just enters into the inversion region, and let $V_{\rm TS}$ denote the gate voltage when the s-Si surface channel just enters into the inversion region. Considering the fact that the hole mobility in the buried channel is higher than that in the surface channel, we should design $V_{\rm TH}$ and $V_{\rm TS}$ such that they satisfy $|V_{\rm TH}| < |V_{\rm TS}|$.

When strong inversion occurs in the s-SiGe buried channel first, the electric potential should satisfy the following equation:

$$\begin{aligned} &\Phi_{3,\rm H}(t_{\rm OX}+t_{\text{s-Si}}) \\ &= \Phi_{\rm TH} \\ &= -\frac{2kT}{q}\ln\frac{N_{\rm B}}{n_{i,y}} + \frac{\Delta E_{\rm v1}}{q}, \end{aligned} \tag{29}$$

where $\Delta E_{\rm v1}$ is the valence offset between the s-SiGe buried channel and the $Si_{1-y}Ge_y$ substrate. Substituting Eq. (29) into Eq. (13) yields

$$\begin{aligned} &t_{\rm d,max} \\ &= -t_{\rm buff} - \frac{\varepsilon_y}{\varepsilon_x}t_{\text{s-SiGe}} \\ &\quad + \sqrt{\left(t_{\rm buff} + \frac{\varepsilon_y}{\varepsilon_x}t_{\text{s-SiGe}}\right)^2 - \frac{2\varepsilon_y}{qN_{\rm B}}\Phi_{\rm TH}}. \end{aligned} \tag{30}$$

It is known that the thickness of depletion layer will stop increasing once it enters into the strong inversion. Thus the threshold voltage of the buried channel can be expressed as

$$\begin{aligned} &V_{\rm TH} \\ &= V_{\rm FB} + \Phi_{5,\rm B}(0) \\ &= V_{\rm FB} + \Phi_{\rm TH} - \frac{qN_{\rm B}t_{\rm d}}{\varepsilon_{\text{s-Si}}}t_{\text{s-Si}} - \frac{qN_{\rm B}t_{\rm d}}{\varepsilon_{\rm ox}}t_{\rm ox}. \end{aligned} \tag{31}$$

When the s-Si surface channel enters into the inversion region, there exists $\Phi_{4,\rm S}(t_{\rm ox}) = \Phi_{\rm TS}$:

$$\Phi_{\rm TS} = -\frac{2kT}{q}\ln\frac{N_{\rm B}}{n_{i,y}} + \frac{\Delta E_{\rm v2}}{q}, \tag{32}$$

where $\Delta E_{\rm v2}$ is the valence offset between the s-Si surface channel and the $Si_{1-y}Ge_y$ substrate. Thus the threshold voltage of the surface channel can be expressed as:

$$\begin{aligned} V_{\rm G} &= V_{\rm TS} \\ &= V_{\rm FB} + \Phi_{5,\rm S}(0) \\ &= V_{\rm FB} + \Phi_{\rm TS} - \frac{qN_{\rm B}t_{\rm d}t_{\rm ox}}{\varepsilon_{\rm ox}}\sqrt{1+H(\Phi_{\rm B})}. \end{aligned} \tag{33}$$

In order to ensure that the strong inversion in the surface channel occurs later than that in the s-SiGe channel, in which the holes have higher mobilities, the electric potential of the s-Si/s-SiGe hetero-interface should satisfy the following inequality:

$$|\Phi_{4,\rm H}(t_{\rm ox})| < |V_{\rm TS}|. \tag{34}$$

Substituting Eq. (32) and inequality (34) into Eq. (20), the maximum allowed thickness of s-Si can be obtained as

$$t_{\text{s-Si max}} \leq \frac{\varepsilon_{\text{s-Si}}\left(\Delta E_{\rm v1} - \Delta E_{\rm v2}\right)}{q^2 N_{\rm B} t_{\rm d}}. \tag{35}$$

5. Results and discussion

With the models derived above and the parameters of strained Si and strained SiGe,[13−15] the variations of threshold voltage with design parameter can be predicted, such as Ge fraction, layer thickness, and doping concentration. The derived analytical model is consistent with the results of device simulation with using the ISE. The relationships of the maximum allowed thickness of s-Si and the threshold voltages with the device structure parameters will be discussed. The threshold voltage is defined as the gate voltage when the minority carrier concentration in the channel is equal to the doping concentration in substrate. According to the curves of the hole concentrations at the surface and the s-Si/s-SiGe hetero-interface which change with the gate voltage, which are obtained from the device simulator ISE,$V_{\rm TH}$ and $V_{\rm TS}$ can be extracted. The maximum allowed thickness of s-Si refers to the thickness when $V_{\rm TH}$ equals $V_{\rm TS}$.

In Fig. 2, it is shown that both $V_{\rm TH}$ and $V_{\rm TS}$ vary with the Ge fraction (y) in $Si_{1-y}Ge_y$, when the Ge fraction (x) is constant in s-SiGe. The strain rate of the s-SiGe layer will reduce when y increases and x keeps constant, leading to a reduction in valence band offset between s-SiGe layer and relaxed $Si_{1-y}Ge_y$ substrate. Consequently, as the intrinsic carrier concentration decreases, a larger $|V_{\rm TH}|$ is needed for the s-Si/s-SiGe hetero-interface to form an inversion layer.

Additionally, the strain rate in the s-Si layer is determined by the Ge content in the relaxed $Si_{1-y}Ge_y$ substrate, and $|V_{TS}|$ will reduce when fewer holes are confined in the buried channel.

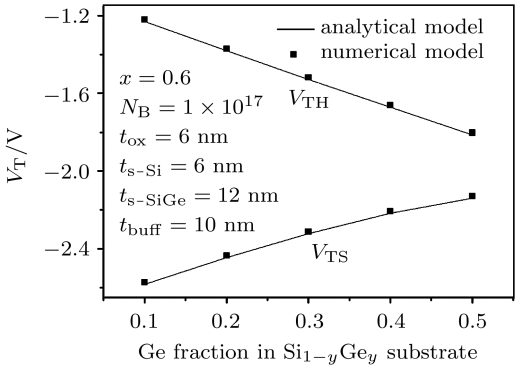


Fig. 2. Variations of buried channel and surface channel threshold voltages with y when x is 0.6.

Figure 3 indicates that V_{TH} decreases when the Ge content increases in the s-SiGe layer and the Ge content is fixed in the relaxed $Si_{1-y}Ge_y$. This is attributed to the enhancement of valance band offset between s-SiGe layer and $Si_{1-y}Ge_y$ substrate, which will lead the intrinsic carrier concentration and hole-sheet density to increase. So, a less negative gate bias is needed for the strong inversion in the buried channel. $|V_{TS}|$ increases with the the increase of Ge fraction (x) in s-SiGe layer on $Si_{1-y}Ge_y$ substrate, which is shown in Fig. 3, owing to the deeper quantum well that will confine more holes in the buried channel.

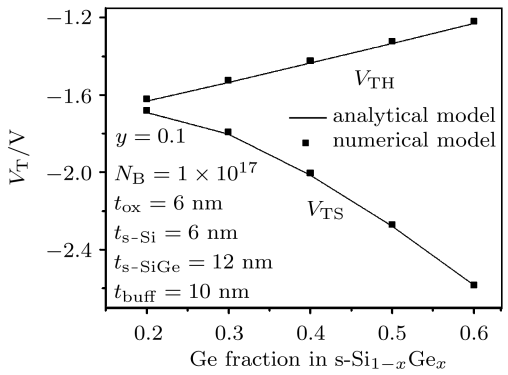


Fig. 3. Variations of buried channel and surface channel threshold voltages with x when y is 0.1.

The dependences of the threshold voltage on substrate doping concentration N_B are shown in Fig. 4. It can be observed that $|V_{TH}|$ and $|V_{TS}|$ increase as doping concentration N_B increases, because the increasing ionized charges cause reverse carrier density to decrease. The difference between V_{TH} and V_{TS} decreases as the Ge fraction increases in the substrate, and $|V_{TH}|$ decreases with the Ge fraction in the substrate reducing, which are shown in Fig. 4. Since the enhancement of the valence band offset between s-SiGe and relaxed $Si_{1-y}Ge_y$ will cause the intrinsic carrier concentration to increase. $|V_{TS}|$ can be explained in turn.

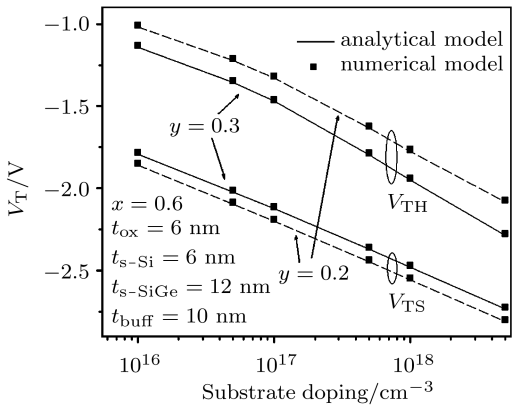


Fig. 4. Variations of buried channel and surface channel threshold voltages with N_B.

Figure 5 shows the variations of V_{TH} and V_{TS} with the thickness of s-Si, $t_{s\text{-}si}$. This increase in $|V_{TH}|$ is due to the fact that the buried channel in the s-SiGe layer is shifted away from the oxide layer by increasing $t_{s\text{-}Si}$. As a result, a more negative gate bias is needed to create a strong inversion in the buried channel. The thicker the s-Si layer is, the higher will the voltage dropping across the s-Si layer be. It causes strong inversion to appear more easily in the surface channel and $|V_{TS}|$ to decrease.

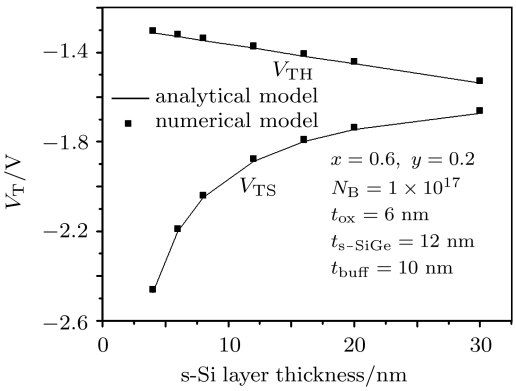


Fig. 5. Variations of buried channel and surface channel threshold voltage with $t_{s\text{-}Si}$.

The maximum allowed s-Si thickness decreases when the substrate doping concentration increases, which results from the increase of ionized charges in the substrate, which is shown in Fig. 6. It can be found that the thickness decreases with a higher Ge fraction in the substrate, which is due to the smaller valance band offset between s-Si layer and s-SiGe. The

smaller valance band offset will also result in smaller threshold voltage difference between the buried and the surface channels as shown in Fig. 6.

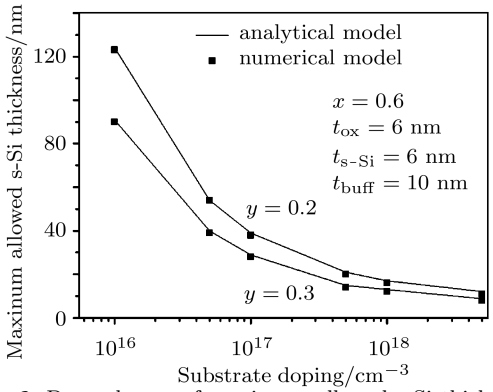


Fig. 6. Dependences of maximum allowed s-Si thickness on N_B and y.

6. Conclusion

Analytical model for the threshold voltage is derived from the analysis of vertical electric potential distribution across the dual-channel PMOSFET. And the maximum allowed thickness of s-Si is given too, which can ensure that the strong inversion happens earlier in the buried channel (compressive strained SiGe) than in the surface channel, because of the higher hole mobility in the buried channel. The analytical model is verified by simulations using ISE. The relationships of the maximum allowed thickness of s-Si and the threshold voltage to device structure parameters are discussed, such as Ge fraction, layer thickness, and doping concentration. This model can serve as a useful reference for p-channel strained Si/strained $Si_{1-x}Ge_x$/relaxd $Si_{1-y}Ge_y$ MOSFET design.

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