Impact of the displacement damage in channel and source/drain regions on the DC characteristics degradation in deep-submicron MOSFETs after heavy ion irradiation*

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This paper mainly reports the permanent impact of displacement damage induced by heavy-ion strikes on the deep-submicron MOSFETs. Upon the heavy ion track through the device, it can lead to displacement damage, including the vacancies and the interstitials. As the featured size of device scales down, the damage can change the dopant distribution in the channel and source/drain regions through the generation of radiation-induced defects and thus have significant impacts on their electrical characteristics. The measured results show that the radiation-induced damage can cause DC characteristics degradations including the threshold voltage, subthreshold swing, saturation drain current, transconductance, etc. The radiation-induced displacement damage may become the dominant issue while it was the secondary concern for the traditional devices after the heavy ion irradiation. The samples are also irradiated by Co-60 gamma ray for comparison with the heavy ion irradiation results. Corresponding explanations and analysis are discussed.

Keywords: CMOS devices, displacement damage, heavy ion irradiation, gamma ray irradiation

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1. Introduction

With the featured size of metal oxide semiconductor field effect transister (MOSFET) scaling down to deep submicron region, short channel effects, punch-through effect and hot carrier effect have become the main issues to the progress of CMOS (Complementary Metal–Oxide–Semiconductor) integrated circuits.[1−4] To suppress their impacts, special device designs are needed, such as lightly doped drain (LDD) structure, retrograde channel doping, halo structure, etc. In the recent years, more attention has been paid to the response of the deep-submicron devices after heavy ion irradiation, including radiation-induced leakage current and soft breakdown.[5,6] For the single device, researchers mainly devoted to studying the radiation-induced charge trapping in the gate oxide, buried oxide and shallow trench isolation (STI) of the devices,[7−17] while little attention has been paid to the displacement damage in the channel and source/drain (S/D) regions of the devices with static impacts. As CMOS technology scales down, the interaction region radius of displacement damage induced by the heavy-ion strike is comparable to the featured size of device. The damage can result in the stochastic variation in the number of dopant atoms located in the channel due to the heavy ion irradiation and thus threshold voltage fluctuation, showing more distinct impact as the highly scaled devices have less than several hundreds of dopant atoms in the channel region. However, so far few reports have reported the impact of displacement damage on the advanced channel engineering in the deep-submicron devices under heavy ion irradiation environment as well as S/D regions. In this paper, the degraded characteristics in the deep-submicron devices due to the displacement damage is investigated and analysed.

2. Experimental details

The devices used in this paper were n-channel and p-channel metal–oxide–semiconductor (MOS) transistors with the SMIC (Semiconductor Manufacturing International Corp. of China) 0.18 μm technology.

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The channel width of the devices was from 0.22 μm to 5 μm, and the channel length of the devices ranges from 0.18 μm to 0.5 μm, respectively. In this experiment, the 60 MeV Br ion (LET = 31.8 MeV $\cdot$ cm^2/mg) was performed to be perpendicular to the surface of the devices for fluences of 5×10^7 ions/cm^2 and 2.2×10^8 ions/cm^2 using electrostatic tandem accelerator. All the devices were not encapsulated in order to be directly irradiated by the heavy ions. Furthermore, the bonding procedure needed to bias the device under irradiation is hard to accomplish as it may introduce substantial damage. During the irradiation, all the terminals were kept floating, which is typical case of many practical situations but not the worst case bias condition. Moreover, to compare with the heavy ion results, some fresh devices were also irradiated by Co-60 gamma source at a dose rate of 50 rad (Si)/s with different doses. Before and after irradiation, the transfer (I_{ds}–V_{gs}) and output (I_{ds}–V_{ds}) characteristics were measured by using a semiconductor parameter analyser (HP-4156) with the source and substrate terminals grounded. In this experiment, there are about 600 samples under radiation (200 samples for gamma ray radiation and 400 for heavy ion radiation, respectively).

3. Results and discussion

After heavy ion irradiation, we found that most devices are degraded for the higher fluence while a small part of the devices are degraded for the lower fluence. This is due to the more probability or multiple strikes on the same device for the higher fluence. However, for the minimum-size MOSFETs in this work, even only one strike can have a very important impact on the characteristics degradation.

First, we discuss some mechanism on the formation of the displacement damage in silicon after heavy ion irradiation. Energetic particles incident on a solid lose their energy, leading to ionizing and nonionizing process as they travel through a given material. The result of this energy loss is the generation of electron–hole pairs (ionization) and displaced atoms (displacement damage). The latter is mainly focused here. The primary lattice defects are vacancies and intersitials. They are highly mobile at room temperature and therefore can migrate a long distance to form a locally disordered region (defect cluster or displacement damage region). Displacement lattice damage in semiconductor materials can have a significant impact on their electrical properties such as decrease of carrier mobility, change of majority carrier density, increase of resistivity, etc. Thus the drain current, threshold voltage and subthreshold swing will be changed accordingly.

The impacts can be divided into three types (Type-A, Type-B, Type-C) and will be analysed in the following. For the degraded devices, Type-A and Type-C account for 10%, respectively. The others belong to Type-B. Table 1 lists the comparison of DC characteristics before and after heavy ion irradiation.

Table 1. Comparison of the characteristics degradation in this work. The impacts can be divided into three types, Type-A, Type-B, Type-C.

degradation	post/pre						
	Type-A		Type-B			Type-C	
	PMOS	NMOS	PMOS	NMOS		PMOS	NMOS
decrease of g_m	19 %	5%	27 %	16.7%	17%	–14.8 %	–9%
degradation of I_g	No	No	No	No	No	No	No
change of SS	No	No	No	No	No	decrease	decrease
shift in V_{th}	80 mV	48 mV	No	No	No	100 mV	72 mV
increase of I_{off}	No	one order	No	No	No	No	No
reduction of I_{on}	21.2 %	5%	slightly	slightly	25%	–26.8 %	–20 %

Figure 1 shows the I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (2.2×10^8 ions/cm^2) for p-type MOSFETs (PMOSFETs) with $W/L = 5$ μm/0.35 μm. The off-state drain current is not degraded. After heavy ion irradiation, although a large number of charges are trapped in the STI region, the threshold voltage of the parasitic transistors induced by irradiation is larger than that of main transistors for PMOSFETs. Therefore, these trapped charges in the STI regions have little

impact on the DC characteristics degradation for the PMOSFETs. The $V_{\rm th}$ shift is negative with its absolute value larger than 80 mV, and a large decline in saturation drain current is observed up to about 20%. This degradation phenomenon is also found in n-type MOSFETs as illustrated in the Fig. 2. The $V_{\rm th}$ increases 48 mV, and the saturation drain current is degraded. We also found that there is about one order of magnitude increase in the off-state drain current after irradiation in the NMOSFETs, which is related to the build-up of positive charge in the STI. This is because there is a parasitic lateral transistor in this irradiated NMOSFETs and the threshold voltage of parasitic lateral transistors is smaller than that of the main transistor. Concerning the Type-A for the NMOSFETs and PMOSFETs, this mainly results from transient enhanced diffusion of dopant atom in the substrate. The induced charges trapped in the gate oxide can be neglected due to the ultra-thin gate oxide for easy tunneling. However, the channel and the S/D regions can also be damaged after heavy ion irradiation. When the heavy ions strike the devices, the crystal structure of the target material is destroyed and lattice damage is generated. The irradiated material consists of a distribution of vacancies and a similar distribution of interstitials. The radiation-induced defects are highly mobile at room temperature, and can migrate a long distance in the Si substrate to form stable extended defects such as clusters or dislocations. After the heavy ion strike, the lattice must be thermally annealed to recover the original crystal lattice. Due to oversaturation of point defects from ion strikes, transient enhanced diffusion of dopant caused by point defects can be observed during post annealing and the diffusion coefficient increases temporarily (i.e. until damage is annealed out) up to 10 times. Therefore, this induces the dopant redistribution in the substrate, increasing the channel surface doping concentration near the source/drain junction. The impact of the dopant distribution is more and more important as the featured size scales down because there are only several hundred dopant atoms in the channel region. The result is also observed as reverse short channel effect.[18] But here is radiation-induced dopant redistribution which causes the increase of threshold voltage and thus the reduction of the drain current is observed.

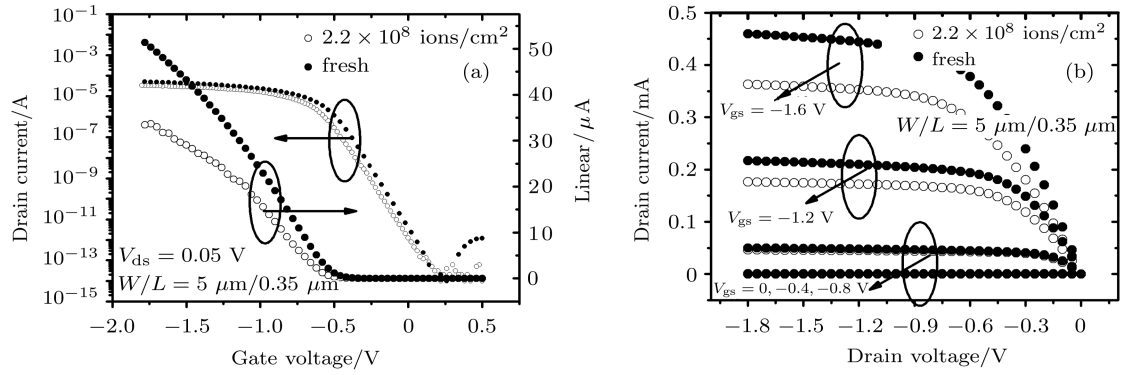


Fig. 1. The $I_{\rm ds}$–$V_{\rm gs}$ and $I_{\rm ds}$–$V_{\rm ds}$ characteristics before and after heavy ions exposure (2.2×10^8 ions/cm^2) for PMOSFETs with $W/L = 5$ μm/0.35 μm (Type-A).

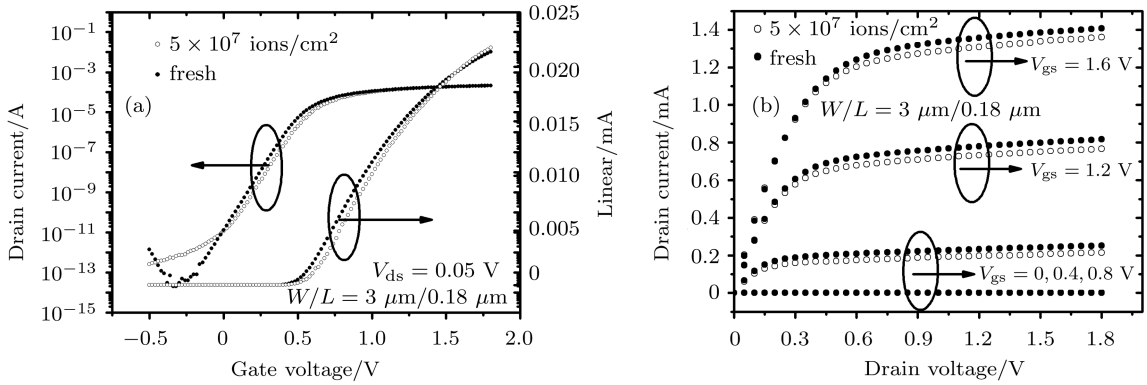


Fig. 2. The $I_{\rm ds}$–$V_{\rm gs}$ and $I_{\rm ds}$–$V_{\rm ds}$ characteristics before and after heavy ions exposure (5×10^7 ions/cm^2) for NMOSFETs with $W/L = 3$ μm/0.18 μm (Type-A).

Figure 3 shows the I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (2.2×10^8 ions/cm^2) for PMOSFETs with W/L = 5 μm/0.18 μm. The V_{th} of PMOSFETs does not shift after irradiation and the drain current in the linear region decreases significantly larger than 50%. Figure 4 shows the I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure for NMOSFET with W/L = 5 μm/0.18 μm. The results in NMOSFETs are similar to the results in PMOSFETs as shown in Fig. 4. The V_{th} shows neglectable shift and the degradation of the drain current in the linear region is up to 30%. The off-state drain current is not increased, revealing that the parasitic transistors are not formed in this irradiated NMOS device probably because the trapped charge in the STI region may not make the surface inverted. Figure 5 shows the I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure for another NMOSFETs with W/L = 5 μm/0.5 μm. The V_{th} has no change while the saturation drain current reduces up to 25%. For Type-B in NMOSFETs and PMOSFETs, this is mainly ascribed to the displacement in the LDD region of the drain region. As we know, the symmetric lightly doped drain structure has been widely used to reduce the leakage current and enhance device reliability for short channel devices. If the displacement damage is in the drain region but away from LDD region, the irradiation has little impact on the DC degradation due to no evident increase of resistance. Therefore, little changes can occur for the traditional device. However, if the radius of the displacement damage region covers the whole or partial LDD region, the displacement damage can increase the resistivity of the LDD region, and thus increase the series resistance in the drain region and lead to the visible decrease of the drain current in the linear region as illustrated in Figs. 3 and 4. If the displacement damage region is near the LDD region of source terminal, the increased series resistance induced by the heavy ion irradiation can also show more distinct degradation of the DC characteristics as shown in the Fig. 5.

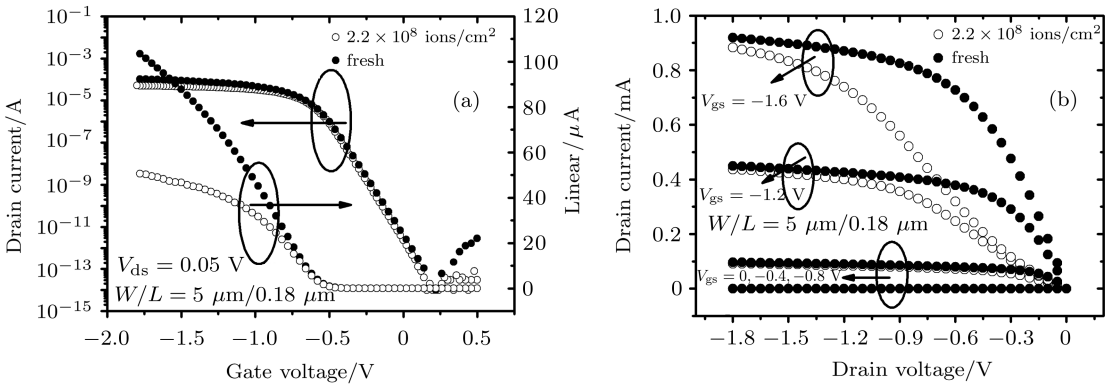


Fig. 3. The I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (2.2×10^8 ions/cm^2) for PMOSFETs with W/L = 5 μm/0.18 μm (Type-B).

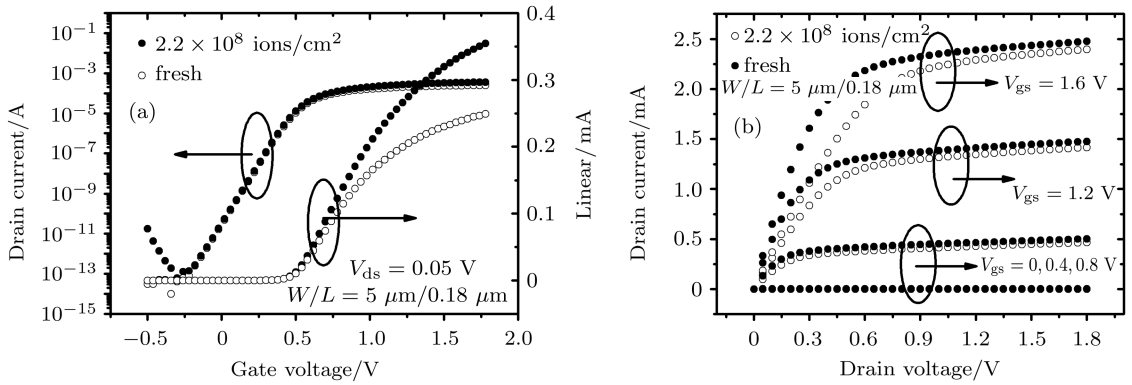


Fig. 4. The I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (2.2×10^8 ions/cm^2) for NMOSFETs with W/L = 5 μm/0.18 μm (Type-B).

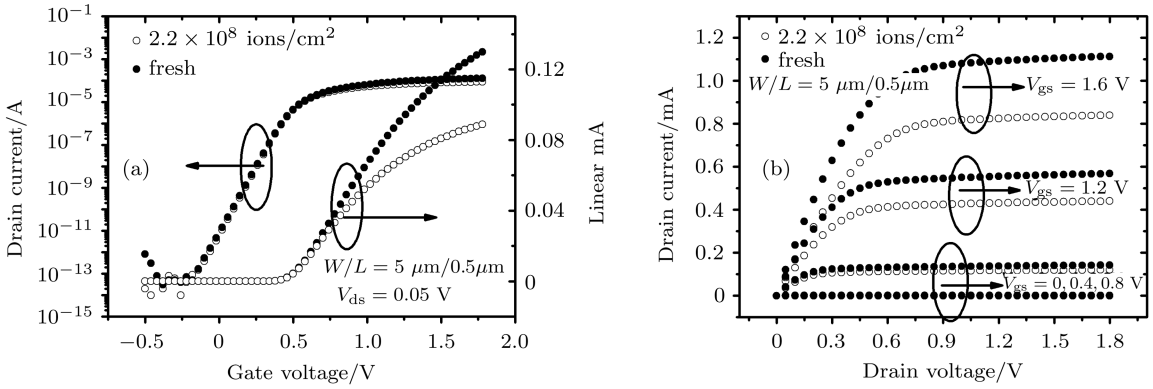


Fig. 5. The I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (2.2×10^8 ions/cm^2) for NMOSFETs with $W/L = 5$ μm/0.5 μm (Type-B).

Figure 6 presents the I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (5×10^7 ions/cm^2) for PMOSFETs with $W/L = 3$ μm/0.18 μm. The V_{th} shift is positive with its absolute value larger than 100 mV. The subthreshold swing becomes smaller, and the saturation drain currents are increased. Besides in the irradiated PMOSFETs, the similarly degraded characteristic is also found in the irradiated NMOS devices. Figure 7 presents the I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (5×10^7 ions/cm^2) for NMOSFETs with $W/L = 0.22$ μm/0.18 μm. The V_{th} decreases about 72 mV. The subthreshold characteristic becomes better and the drain current increases up to about 20%. The breakdown voltage becomes lower as shown in Figs. 6 and 7. To our surprise, great differences appear in the transfer characteristics for type-C in comparison with the above mentioned cases. This may be related to the decrease of active doping density in channel region. In a traditional device, the channel length is much larger than the size of the displacement damage region. Thus the induced local dopant density change is negligible. Nevertheless, for the ultra-deep-submicron device, the radius of the displacement damage region is comparable to the size of the device. The radiation-induced defects (damage) can make the decrease of channel average doping density. This will lead to the V_{th} reduction and the depletion capacitance C_D decrease with gate capacitance C_{ox} unchanged. Therefore, the subthreshold swing decreases. However, the device may punch through at higher drain voltage, which causes much larger drain current compared to the fresh device, as shown in Figs. 6 and 7.

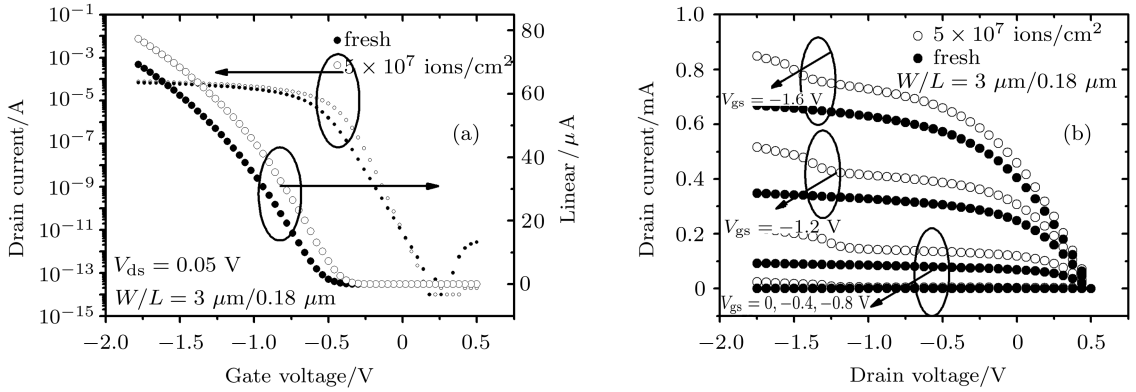


Fig. 6. The I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (5×10^7 ions/cm^2) for PMOSFETs with $W/L = 3$ μm/0.18 μm (Type-C).

Moreover, in order to compare with the heavy ion results, some fresh devices are also irradiated by Co-60 gamma source at a dose rate of 50 rad (Si) /sec with different doses. Figure 8 shows the I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after Co-60 gamma ray exposure for NMOSFETs with W/L of 5 μm/0.18 μm. The

evident change is the increase of off-state drain current as the dose increases, which is related to the build-up of positive charge in the STI. This is because the threshold voltage of parasitic lateral transistors is smaller than that of the main transistors and the number of trapped charges in the STI regions become more large as the dose increases. For the output curves, the saturation drain current is slightly increased due to the parasitic current of the parasitic transistors. For PMOSFETs after the gamma ray radiation, no changes are observed (not shown here). Even though a large number of charges are trapped in the STI regions, these trapped charges have little impact on the off-state drain current. This is because the threshold voltage of the parasitic transistors is larger than that of the main transistors, and thus the parasitic transistors can not be turned on under normal operating voltage. All the irradiated NMOSFETs and PMOSFETs by gamma ray radiation show the same results. In general, only ionization damage is taken into account when energetic photons (gamma ray and x-ray) interact with solid-state material. However, for high-energy heavy ions, displacement damage should also be considered in the irradiated material. The energy transferred during an elastic and inelastic nuclear collision may be large enough to knock an atom from its lattice site. This creates a vacancy and an atom in an interstitial position. The probability of such displacement is higher for higher energy and larger atomic number of the heavy ion. The experimental results show that the characteristics of the irradiated NMOSFETs and PMOSFETs after heavy ion irradiation is different from that of gamma ray radiation. This reveals that the displacement damage induced by heavy ion strikes is more important for the DC degradation under heavy ion irradiation.

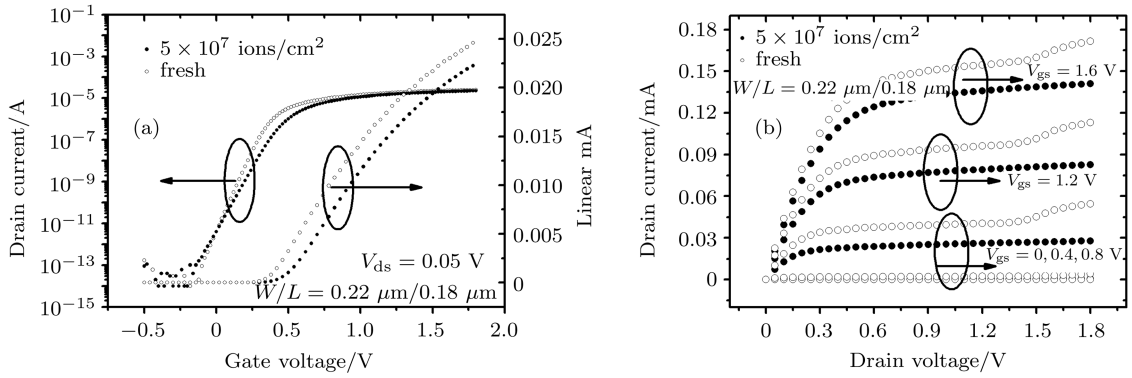


Fig. 7. The I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after heavy ions exposure (5×10^7 ions/cm^2) for NMOSFETs with $W/L = 0.22$ μm/0.18 μm (Type-C).

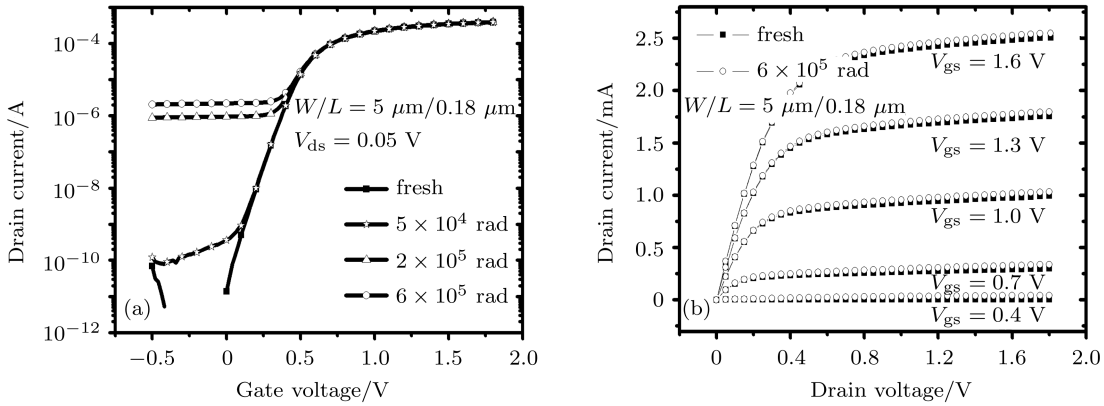


Fig. 8. The I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics before and after Co-60 gamma ray exposure for NMOSFETs with $W/L = 5$ μm/0.18 μm.

4. Conclusion

This paper mainly presents the impacts of permanent damage induced by heavy-ion strikes on the deep-submicron MOSFETs. The results of this work show the measured DC characteristics degradations due to the transient enhanced diffusion of dopant atom in the substrate, the increase of the series resistance in the

D/S region, the decrease of active doping density in channel region. As CMOS technology scales into the ultra-deep-submicron region, the displacement damage can cause the devices permanent damaged and becomes a very important factor for radiation hardness. Moreover, the radiation-induced device behaviour can lead to profound changes in the circuits' performance, some of which may be very difficult to predict. Therefore, to design radiation-hardened circuits, more attention should be paid to the impact induced by the displacement damage after heavy ion irradiation. The channel engineering as well as S/D engineering such as retrograde doping structure, LDD structure, halo structure etc., which is necessary for scaled CMOS technology, should be reconsidered and trade-off for the radiation-hardened design.

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