Statistical Elmore delay of RC interconnect tree*

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As feature size keeps scaling down, process variations can dramatically reduce the accuracy in the estimation of interconnect performance. This paper proposes a statistical Elmore delay model for RC interconnect tree in the presence of process variations. The suggested method translates the process variations into parasitic parameter extraction and statistical Elmore delay evaluation. Analytical expressions of mean and standard deviation of interconnect delay can be obtained in a given fluctuation range of interconnect geometric parameters. Experimental results demonstrate that the approach matches well with Monte Carlo simulations. The errors of proposed mean and standard deviation are less than 1% and 7%, respectively. Simulations prove that our model is efficient and accurate.

Keywords: statistical delay, parasitic extraction, RC interconnect, process variations

PACC: 0250, 7220, 7850G

1. Introduction

With technologies shrinking to the deep submicrometer (DSM) regime, the impact of process variations on very large scale integration (VLSI) circuits has become extremely critical.[1−3] Technology scaling beyond (shorter or lower) 90 nm is causing high levels of parameter variations, which are changing the design problem from a deterministic problem to a probabilistic problem.[4] Process variations affect not only the yield, but also the performance and reliability.[5]

As we know, the impact of interconnects is more important than that of gates.[6,7] The RC delay of interconnects is 2.75 times larger than the gate delay at 90 nm; 4.29 times larger at 65 nm, and 7.56 times larger at 45 nm.[8] Interconnect process variation has a direct impact on the delay of interconnect tree. The performance of interconnect is becoming less predictable as device dimensions shrink below the sub-100 nanometer scale. The reduced predictability stems from poor control of the physical features of interconnects in the manufacturing process. All of these make it increasingly difficult to analyse the delay of RC interconnect tree in the presence of process variations. Thus, it is very crucial to develop an efficient and accurate strategy for delay analysis during early design.

Although some circuit computer-aided design (CAD) tools, such as HSPICE,[9] are able to analyse the delay of interconnect with variations, they are all based on the Monte Carlo approach. With this technique, random samples of each input variable are taken. The outputs are computed for each set of inputs over several trials and distribution results. The Monte Carlo simulation[10,11] obtains a realistic distribution, but it increases the simulation time considerably. Considering that the interconnect delay distribution with process variation is Gaussian distribution, a new approach to converting process variations into delay variation is presented so as to resolve the above mentioned problem.

In this paper, we first briefly review the characteristics of process variations. We then introduce an effective resistance and capacitance model in the presence of process variations. Next, statistical Elmore delay of RC tree is obtained using the proposed new parasitic parameter model. Finally, we verify and summarize our work.

2. Characteristics of process variations

Process variations depend on structural variation in the chip that is based on the circuit layout, neighbouring environment, and process conditions. Process variations impact the geometry of a structure and can lead to undesirable effects which may be functional or parametric, causing a malfunctioning circuit or degradation in performance.[12]

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As shown in Fig. 1, the interconnect structural variation is composed of three components, metal thickness, inter-layer dielectric (ILD) thickness, and line width. Additional geometric effects such as sidewall slope or surface and edge roughness may also be of concern, but are not considered in this work. Note that line space is not an independent parameter since a variation in line width automatically causes a change in the line space.

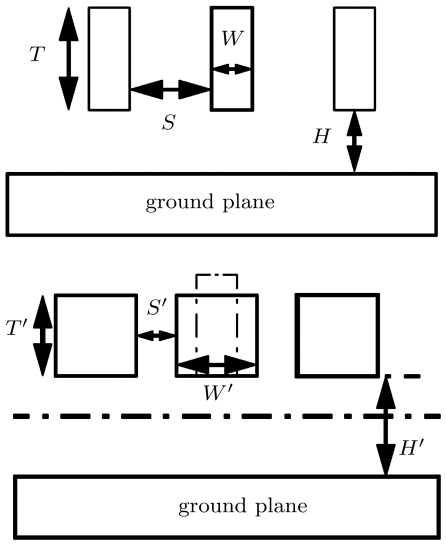


Fig. 1. Cross-section of parallel interconnect lines.

In Fig. 1, the figure on the top shows the ideal case, and the figure on the bottom shows some different types of variations in the interconnect lines. The variations caused by manufacturing will alter the geometry of interconnect. This in turn leads to variations in electrical parameter such as line resistance and capacitance.

3. Resistance and capacitance with process variations

The importance of interconnect parasitic parameter has been in an ever increasing trend. The clock trees often contain long wires, therefore a good description of the interconnect geometry variation is needed for accurate circuit simulation. With any change in the physical dimension of interconnect, its resistance and capacitance also change, causing interconnect delay to fluctuate.[13] In order to model the influence of variation on interconnect delay, we need to capture the effect of geometric variation on the electrical parameters. Therefore, it is necessary to handle process variations as accurately as possible in layout parasitic extraction.

For the simple structure shown in Fig. 1, the geometric parameters of interest are line width W, line space S, ILD thickness H and metal thickness T. For the middle line surrounded by two lines, its resistance R, self capacitance $C_{\rm gnd}$, and coupling capacitance $C_{\rm coup}$ per unit length can be expressed using the following equations as[14]

$$R = \rho l/WT, \tag{1}$$

$$\frac{C_{\rm gnd}}{\varepsilon} = 1.11\frac{W}{H} + \left[0.79\left(\frac{W}{H}\right)^{0.10} + 0.59\left(\frac{T}{H}\right)^{0.53}\right] + \left[0.52\left(\frac{W}{H}\right)^{0.01} + 0.46\left(\frac{T}{H}\right)^{0.17}\right]\left(1 - 0.87\,\mathrm{e}^{-\frac{S}{H}}\right), \tag{2}$$

$$\frac{C_{\rm coup}}{\varepsilon} = \frac{T}{S} + 1.21\left(\frac{T}{H}\right)^{0.10}\left(\frac{S}{H} + 1.15\right)^{-2.22} + 0.25\ln\left(1 + 7.17\frac{W}{S}\right)\left(\frac{S}{H} + 0.54\right)^{-0.64}. \tag{3}$$

Then, the total interconnect capacitance is expressed as

$$C = C_{\rm gnd} + 2C_{\rm coup}. \tag{4}$$

The analysis of the interconnect sensitivity to process variation can reflect the variation of parasitic parameters with interconnect physical dimension. To simplify the analysis, we use Z to represent the geometric parameters such as line width, line space, ILD thickness, and metal thickness. The changes in the resistance and the capacitance due to these geometric variations can be written as

$$\Delta R = \frac{\partial R}{\partial Z}\Delta Z, \tag{5}$$

$$\Delta C = \frac{\partial C}{\partial Z}\Delta Z. \tag{6}$$

In order to capture the relationship between changes in electrical parameters and those in geometric parameters, the variations of resistance and capacitance versus interconnect width under 65 nm process technology are illustrated in Fig. 2.

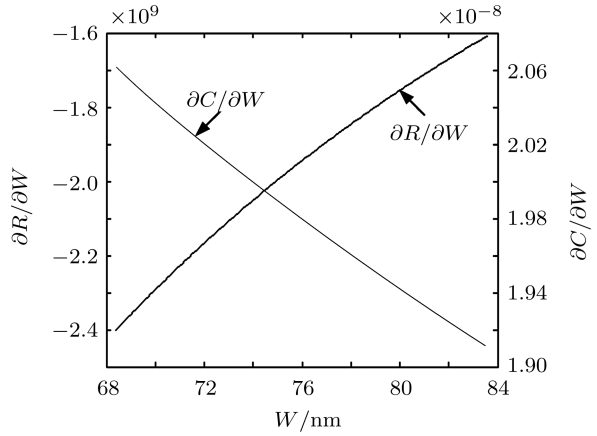


Fig. 2. Variations of resistance and capacitance versus interconnect width.

It shows that linear approximation[15] can be used to describe these changes, leading to the following equation:

$$\frac{\partial R}{\partial Z} = a_{\mathrm{ZR}} Z_{\mathrm{practical}} + b_{\mathrm{ZR}}. \tag{7}$$

Here, $Z_{\mathrm{practical}}$ represents nominal geometric parameter. The modeling coefficients a_{ZR} and b_{ZR} can be calculated using

$$\left.\frac{\partial R}{\partial Z}\right|_{1.1Z} = 1.1 a_{\mathrm{ZR}} Z + b_{\mathrm{ZR}}, \tag{8}$$

$$\left.\frac{\partial R}{\partial Z}\right|_{0.9Z} = 0.9 a_{\mathrm{ZR}} Z + b_{\mathrm{ZR}}. \tag{9}$$

After solving the above equations, the constants a_{ZR} and b_{ZR} are as follows:

$$a_{\mathrm{ZR}} = \frac{1}{0.2Z}\left(\left.\frac{\partial R}{\partial Z}\right|_{1.1Z} - \left.\frac{\partial R}{\partial Z}\right|_{0.9Z}\right), \tag{10}$$

$$b_{\mathrm{ZR}} = \left.\frac{\partial R}{\partial Z}\right|_{1.1Z} - 1.1 a_{\mathrm{ZR}} Z. \tag{11}$$

Hence, Eq. (5) can be rewritten as

$$\begin{aligned}\Delta R &= \left[a_{\mathrm{ZR}}\left(Z+\Delta Z\right)+b_{\mathrm{ZR}}\right]\Delta Z \\ &= a_{\mathrm{ZR}}\left(\Delta Z\right)^2 + \left(a_{\mathrm{ZR}} Z + b_{\mathrm{ZR}}\right)\Delta Z.\end{aligned} \tag{12}$$

Assuming that the geometric parameters which obey distribution $N(0,\sigma_Z^2)$ are independent random variables, the expressions of mean and standard deviation of interconnect resistance with process variation considered are given by

$$E\left(R\right) = R + E\left(\Delta R\right) = R + \sum_Z a_{\mathrm{ZR}}\sigma_Z^2, \tag{13}$$

$$\begin{aligned}D\left(R\right) &= D\left(\Delta R\right) \\ &= \sum_Z 2a_{\mathrm{ZR}}^2\sigma_Z^4 + \sum_Z \left(a_{\mathrm{ZR}} Z + b_{\mathrm{ZR}}\right)^2\sigma_Z^2.\end{aligned} \tag{14}$$

By performing similar calculations for the interconnect capacitance, its mean and standard deviation can be expressed as

$$E\left(C\right) = C + E\left(\Delta C\right) = C + \sum_Z a_{\mathrm{ZC}}\sigma_Z^2, \tag{15}$$

$$\begin{aligned}&D\left(C\right) \\ &= D\left(\Delta C\right) \\ &= \sum_Z 2a_{\mathrm{ZC}}^2\sigma_Z^4 + \sum_Z \left(a_{\mathrm{ZC}} Z + b_{\mathrm{ZC}}\right)^2\sigma_Z^2.\end{aligned} \tag{16}$$

In conclusion, the changes in electrical parameter due to variation in geometric dimensions can be captured by Eqs. (13)–(16).

4. Statistical Elmore delay model

In this section, we discuss a new approach to modeling the interconnect delay while considering variations in physical dimension.

The interconnect delay is defined as the time difference between the input and the output waveforms crossing 50% of their full-swing value.

Elmore delay model is widely used due to the existence of a simple tractable formula for the delay that has recursive properties, making the calculation of circuits highly efficient.

For an RC tree, Elmore delay at node i is defined as[16−18]

$$\tau_i = \sum_{j\in P_i} R_j \cdot C_{\mathrm{d}j}. \tag{17}$$

Here P_i means the only path from the root to the given node i, and $C_{\mathrm{d}j}$ is the total downstream capacitance at j.

In fact, although the Elmore delay is the upper bound for the interconnect delay, it is very close to the actual delay. Hence, Elmore delay model is adopted to analyse the RC delay in the presence of geometric parameter variations.

According to the definition of Elmore delay shown in Eq. (17), the fluctuation of delay in the presence of the process variations can be expressed as

$$\begin{aligned}&\Delta\tau_i \\ &= \sum_{j\in P_i}\frac{\partial\tau}{\partial R_j}\Delta R_j + \sum_{j=1}^{n}\frac{\partial\tau}{\partial C_j}\Delta C_j \\ &= \sum_{j\in P_i} C_{\mathrm{d}j}\Delta R_j + \sum_{j=1}^{n} R_{ij}\Delta C_j \\ &= \sum_{j\in P_i} C_{\mathrm{d}j}\Delta R_j + \sum_{j\in P_i} R_{ij}\Delta C_j + \sum_{j\notin P_i} R_{ij}\Delta C_j\end{aligned}$$

$$= \sum_{j\in P_i} \left(C_{\mathrm{d}j}\Delta R_j + R_{ij}\Delta C_j\right) + \sum_{j\notin P_i} R_{ij}\Delta C_j. \quad (18)$$

In Eq. (18), R_{ij} is the common resistance from the input to nodes i and j. n is the number of all nodes.

It is easy to obtain the mean of interconnect delay with process variations by using the above mentioned method, i.e.,

$$\begin{aligned} & E(\tau_i) \\ &= \tau_i + E(\Delta\tau_i) \\ &= \tau_i + \sum_{j\in P_i} C_{\mathrm{d}j} E(\Delta R_j) + \sum_{j=1}^{n} R_{ij} E(\Delta C_j). \end{aligned} \quad (19)$$

When the geometric parameters are fluctuating, ΔR_j and ΔC_j are correlative. According to the equation $\mathrm{cov}(X,Y) = E(XY) - E(X)E(Y)$, the covariance of ΔR_j and ΔC_j can now be written as

$$\begin{aligned} & \mathrm{cov}_j(Z) \\ &= \mathrm{cov}\left(C_{\mathrm{d}j}\Delta R_{jZ}, R_{ij}\Delta C_{jZ}\right) \\ &= 2C_{\mathrm{d}j} a_{\mathrm{ZR}j} R_{ij} a_{\mathrm{ZC}j} \cdot \sigma_Z^4 \\ &\quad + C_{\mathrm{d}j} R_{ij} \left(a_{\mathrm{ZR}j} Z + b_{\mathrm{ZR}j}\right)\left(a_{\mathrm{ZC}j} Z + b_{\mathrm{ZC}j}\right)\sigma_Z^2. \end{aligned} \quad (20)$$

Using the Eq. $D(X+Y) = D(X) + D(Y) + 2\mathrm{cov}(X,Y)$, covariance of delay can be expressed, using the following equation, as

$$\begin{aligned} D(\tau_i) &= D(\Delta\tau_i) \\ &= \sum_{j\notin P_i} R_{ij}^2 D(\Delta C_j) + \sum_{j\in P_i} \Big[C_{\mathrm{d}j}^2 D(\Delta R_j) \\ &\quad + R_{ij}^2 D(\Delta C_j) + 2\mathrm{cov}_j(W) + 2\mathrm{cov}_j(T)\Big]. \end{aligned} \quad (21)$$

We can also use the standard deviation that is given in Eq. (22) to further simplify the application.

$$\sigma_i = \sqrt{D(\tau_i)}. \quad (22)$$

5. Simulation and discussion

In this section, we use the RC interconnect tree shown in Fig. 3 to verify the efficiency and accuracy of the proposed model.

There are made two assumptions for the RC tree. The first one is that nodes 4, 6, 7, 8, 9, and 10 connect the substrate through vias. The second one is that the changes in geometric parameter Z obey the normal distribution and $3\sigma_Z$ is equal to 10 % of the nominal value.

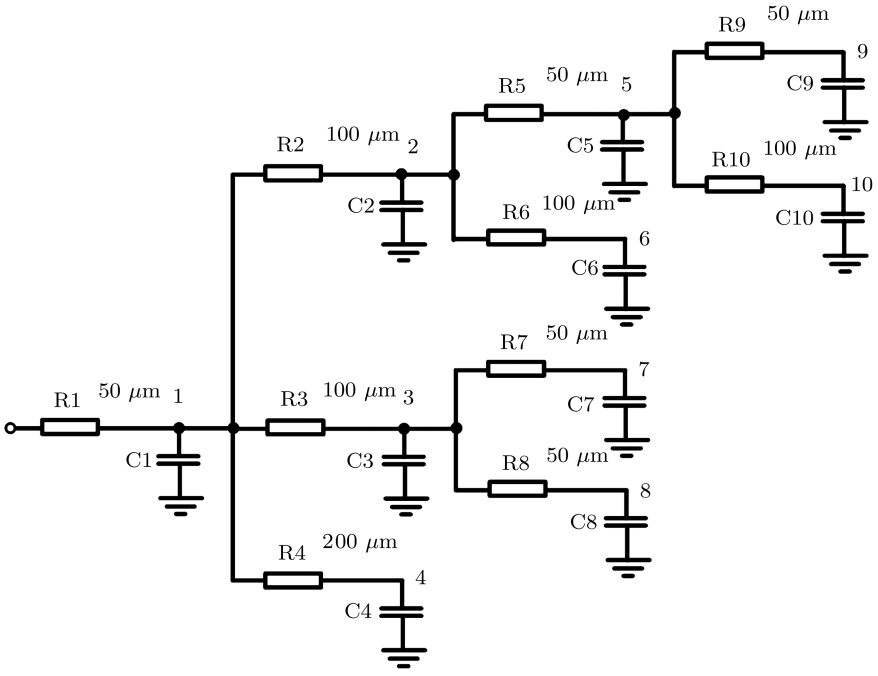


Fig. 3. RC interconnect tree.

In order to verify the proposed model, we compare the analytical model with the HSPICE-based Monte Carlo simulation.[9] The probability plots for delay of node 9 are shown in Fig. 4. For this test case, the values for W, T and H were chosen from 90 nm process technology,[8] and their 3-σ variabilities are all selected to be 10%. The figure compares the histogram obtained by Monte Carlo simulation with the Gaussian distribution given by analytical model proposed in the previous section. The mean and the standard deviation of delay, computed using the analytical mode, match well with the values found using Monte Carlo simulation.

To further verify the proposed model, we compare the delays obtained from HSPICE-based Monte Carlo simulation via 1000 sampling points with those achieved by our method. We compute the mean and the standard deviation of delay at various nodes in the RC tree shown in Fig. 3. Table 1 compares the mean and the standard deviation obtained using Monte Carlo simulation with those achieved using the proposed model under process node 90 nm, 65 nm and 45 nm.[8] The table shows that the model works well across all nodes. The error ranges of mean and standard deviation are −0.81%–1% and −1.45%–6.34%, respectively. We also find that node 4 shows a relatively large error in the simulations of mean and standard deviation. This large error is primarily due to its longer path from the root node. At the same time, with the feature size decreasing, the sensitivity of process variation increases dramatically, which causes the higher errors under 45 nm process technology.

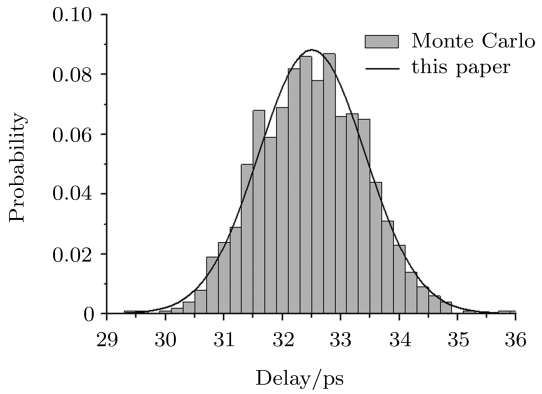


Fig. 4. Comparison between delay probability distributions obtained by Monte Carlo simulation and proposed method.

Table 1. Mean and standard deviation of RC interconnect delay.

node	process/nm	mean/ps			σ/ps		
		Monte Carlo[9]	this paper	error/(%)	Monte Carlo[9]	this paper	error/(%)
9	90	32.505	32.771	0.82	0.9094	0.9251	1.73
	65	56.963	56.933	–0.053	1.5827	1.6081	1.60
	45	102.402	102.17	–0.227	2.8019	2.8890	3.11
10	90	35.095	35.358	0.75	0.9006	0.9224	2.43
	65	61.424	61.428	0.0063	1.5629	1.6036	2.60
	45	110.277	110.24	–0.034	2.7738	2.8814	3.88
6	90	31.658	31.908	0.79	0.8997	0.9146	1.66
	65	55.502	55.435	–0.12	1.5673	1.5898	1.44
	45	99.821	99.481	–0.34	2.7718	2.8560	3.04
7	90	22.201	22.423	1.00	0.7412	0.7403	–0.12
	65	39.031	38.955	–0.19	1.3057	1.2868	–1.45
	45	70.479	69.905	–0.81	2.3124	2.3113	–0.05
8	90	22.201	22.423	1.00	0.7412	0.7403	–0.12
	65	39.031	38.955	–0.19	1.3057	1.2868	–1.45
	45	70.479	69.905	–0.81	2.3124	2.3113	–0.05
4	90	28.225	28.460	0.83	0.7733	0.8106	4.83
	65	49.532	49.442	–0.18	1.3520	1.4092	4.23
	45	89.148	88.727	–0.47	2.3812	2.5321	6.34

The proposed model can present the closed-form expressions of mean and standard deviation of interconnect delay for the given variations in relevant process parameters, such as line width, metal thickness, line space, and ILD thickness. Hence, it takes less running time than Monte Carlo Simulation.

6. Conclusion

Based on the Elmore delay model, a novel statistical model of RC interconnect delay in the presence of process variations is presented. Analytical expressions of mean and standard deviation of interconnect delay can be obtained in a given fluctuation range of interconnect parameters. The calculation efficiency is improved by the proposed novel statistical model compared with that by the HSPICE-based Monte Carlo method. In sum, the proposed model can be used for simulating and optimizing VLSI interconnect delay.

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