Preparation of size controllable copper nanocrystals for nonvolatile memory applications

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A method of fabricating Cu nanocrystals embedded in SiO_2 dielectric film for nonvolatile memory applications by magnetron sputtering is introduced in this paper. The average size and distribution density of Cu nanocrystal grains are controlled by adjusting experimental parameters. The relationship between nanocrystal floating gate micro-structure and its charge storage capability is also discussed theoretically.

Keywords: nanocrystal grain, nonvolatile memory, Coulomb blockade effect, magnetron sputtering

PACC: 8116D, 9365, 2110S, 8115C

1. Introduction

Nowadays, portable digital devices, such as cellular phones, digital cameras, and laptops, are playing more and more important roles in people's daily lives. In these devices, nonvolatile memory is one of the key components. It is responsive for date storage and can significantly affect the overall performance. Higher storage density, faster write/erase speed and lower operating voltage are required in the future memory. However, because of its structure limitation, traditional memory, in which the polysilicon floating gate is used, struggles to meet these requirements. Under this background, a new memory structure in which a nanocrystal floating gate was used, was introduced by Tawari *et al.*[1] Because nanocrystal floating gate memory has many advantages such as a low operating voltage, high endurance, fast write/erase speed and better immunity to soft error,[2] more and more research groups now focus on this field. A variety of nanocrystal floating gates, such as Au, Pt, Ag, Si, Ge, have been fabricated and their electrical properties have also been investigated.[3−7] However, though the methods of fabricating nanocrystal grains are rapidly developed, the size and distribution density control of the nanocrystal grains has been studied very little. The relationship between nanocrystal floating gate micro-structure and its charge storage capability is seldom discussed either.

In this work, a method of fabricating monolayer Cu nanocrystal grains embedded in SiO_2 dielectric films by magnetron sputtering is developed. The average size and distribution density of the Cu nanocrystal grains are well controlled in a certain range by adjusting the sputtering parameters. The relationship among average size, distribution density and charge storage capability of metal nanocrystal grains are discussed theoretically.

2. Experiment and discussion

The experimental parameters of magnetron sputtering, such as sputtering voltage, sputtering current, pressure, substrate temperature and deposition time are all controllable during the deposition process. This advantage makes the magnetron sputtering chosen for fabricating nanocrystal grains in this work. The fabrication process of dielectric layer/Cu nanocrystal floating gate/dielectric layer, which has a sandwich structure, can be illuminated in Fig. 1. First, a 3-nm SiO_2 dielectric film grew on a well-cleaned Si substrate (p-type, (100) orientation) as tunnel oxide layer. Then, a thin Cu film was deposited on it. Because usually there exists considerable interface energy between metal film and amorphous film, the growth of the deposited Cu film will follow the Volmer–Weber mode,[8]

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That means that not only continuous film but also discrete nanodots will form on the tunnel oxide layer in the beginning. In this step, the growth rate and time were controlled accurately to ensure that the theoretical thickness of Cu film does not exceed a critical thickness at which the Cu nanodots begin to be connected with each other. After these two steps, a SiO_2 film of 25 nm in thickness was deposited onto the monolayer of Cu nanocrystal grains as a control oxide layer.

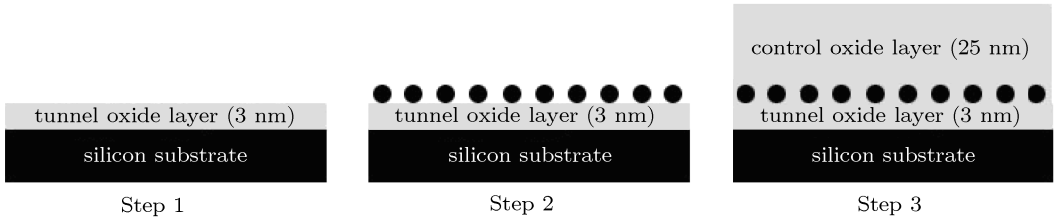


Fig. 1. Illustration of the Cu nanocrystal fabrication process.

The critical thickness was investigated in a series of pre-experiments and the transmission electron microscope (TEM) results verified that the value was about 2 nm.[9] Then, in the Cu nanocrystal fabrication process, the growth rate and the deposition time were controlled carefully to ensure that the theoretical thickness of the deposited Cu film does not exceed 2 nm. The growth rates of Cu film under different sputtering parameters were obtained through a series of preliminary experiments. Table 1 shows the growth rates under different sputtering powers.

Table 1. Growth rates of Cu film under different sputtering powers.

sputtering power/W	69	110	130	170
Cu growth rate/nm·s^{-1}	0.9	1.7	2.1	3.3

Appropriate sputtering parameters were selected by a series of pre-experiments. The sputtering powers were chosen to be 48, 55 and 69 W by adjusting sputtering voltage and current, and the deposition times for Cu films were all fixed to be 2 s. The temperature of the substrates temperatures were all kept at 400 °C during the deposition process. Heating of the substrates provides extra energy for the adsorbed Cu atoms and helps them transfer easily on the amorphous SiO_2 layer, which plays an important role in the growth of Cu nanocrystal grains.[9] The plane view appearance of the composited films was observed by TEM JEM-2011. The appearance of the Cu nanocrystal grains and the statistical results are shown in Fig. 2.

Figure 2 shows that the prepared Cu nanocrystal grains are homogeneous in size and uniform in distribution. As the sputtering power increases to 48, 55 and 69 W, the average diameter of the obtained Cu nanocrystal grains increases to 3.7, 4.3 and 5.8 nm respectively. Meanwhile, the nanocrystal grain distribution density decreases from 1.7×10^{12}/cm^2 to 8.8×10^{11}/cm^2. These values are consistent with those given by other groups' work.[3,10,11] The experimental results verify that the average size and the distribution density of Cu nanocrystal grains are controllable in a certain range by adjusting the sputtering parameters.

It is believed that the Coulomb blockade effect is significant in the nanocrystal floating gate write/erase process. So the discussion on the relationship between nanocrystal floating gate micro-structure and its charge storage capability is necessary and helpful for designing devices. The Coulomb blockade energy of nanocrystal grain can be expressed as $e^2/2C$, where e is the magnitude of electronic charge, C is the capacitance of a single nanocrystal grain. Because most of the nanocrystal grains are spherical, the Coulomb blockade energy expression can be converted into $e^2/4\pi\varepsilon_0\varepsilon_r d$, where d is the diameter of spherical nanocrystal grain, ε_r is the permittivity of silicon dioxide film. It shows that the Coulomb blockade energy is inversely proportional to the nanocrystal grain diameter. From this point of view, if fast write/erase speed and low operating voltage are required in a nanocrystal floating gate memory, nanocrystals with larger average diameter should be chosen preferably.

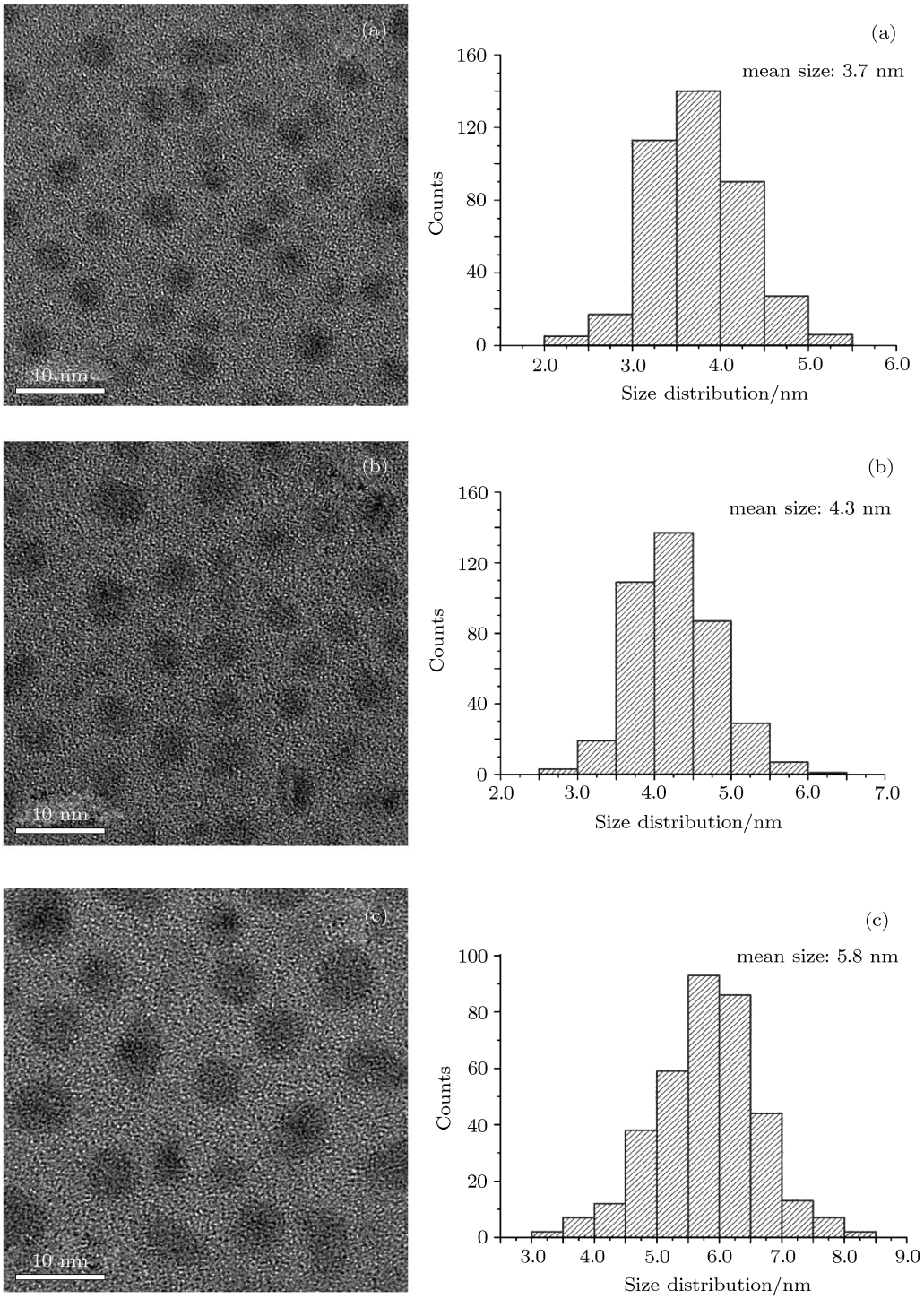


Fig. 2. Appearance and statistical results of prepared Cu nanocrystal grains at sputtering powers of 48 W (a), 55 W (b), and 69 W (c).

The distribution density of the nanocrystal grains can also affect the device performance. Tiwari *et al.*[1] have given the relationship between memory threshold voltage shift and nanocrystal floating gate micro-structure as follows:

$$\Delta V_{\mathrm{FB}} = \frac{qN_{\mathrm{nc}}}{\varepsilon_{\mathrm{ox}}}\left(t_{\mathrm{cox}} + \frac{\varepsilon_{\mathrm{ox}} t_{\mathrm{nc}}}{2\varepsilon_{\mathrm{nc}}}\right), \tag{1}$$

where N_{nc} is the distribution density of nanocrystals, $\varepsilon_{\mathrm{ox}}$ and $\varepsilon_{\mathrm{nc}}$ are the permittivities of the dielectric layer and the nanocrystal grain respectively, t_{cox} is the thickness of the dielectric layer, and t_{nc} is the linear dimension

of nanocrystals. Because the permittivity of metallic materials is infinite under electrostatic field, equation (1) can be simplified into

$$\Delta V_{\mathrm{FB}} = \frac{qN_{\mathrm{nc}}}{\varepsilon_{\mathrm{ox}}} t_{\mathrm{cox}}. \tag{2}$$

Equation (2) shows that ΔV_{FB} is proportional to nanocrystal grain distribution density. That means that the increasing of the distribution density can enlarge the flash memory flat-band voltage shift. From this point of view, if a wide memory window is needed, floating gate with a large nanocrystal grain distribution density is preferred.

3. Conclusion

In this paper, a method of fabricating the Cu nanocrystal floating gate by magnetron sputtering is introduced. By adjusting magnetron sputtering parameters, the average size of the Cu nanocrystal grains can be controlled from 3.7 nm to 5.8 nm, and the distribution density can also be controlled at $1.7\times10^{12}/\mathrm{cm}^2$ to $8.8\times10^{11}/\mathrm{cm}^2$. The theoretical analysis indicates that large-diameter nanocrystal grains in the floating gate are favourable for increasing device write/erase speed and lowering device operating voltage. The increasing of the distribution density of the nanocrystal grains is helpful for enlarging the memory window.

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