Study on two-dimensional analytical models for symmetrical gate stack dual gate strained silicon MOSFETs*

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Based on the exact resultant solution of two-dimensional Poisson's equation, the novel two-dimensional models, which include surface potential, threshold voltage, subthreshold current and subthreshold swing, have been developed for gate stack symmetrical double-gate strained-Si MOSFETs. The models are verified by numerical simulation. Besides offering the physical insight into device physics, the model provides the basic designing guidance of further immunity of short channel effect of complementary metal-oxide-semiconductor (CMOS)-based device in a nanoscale regime.

Keywords: strained-Si, gate stack double-gate MOSFETs, short channel effect, the drain-induced barrier-lowering

PACC: 7330, 7340R, 7215N

1. Introduction

As complementary metal oxide semiconductor (CMOS) scaling is approaching the limit imposed by gate oxide tunneling, double-gate (DG) MOSFET is becoming a subject of intense very large scaled integrated circuit (VLSI) research because, in theory, it can be scaled to the shortest channel length possible for a given gate oxide thickness. The advantage advocate for DG MOSFETs includes: 1) 60-mV/decade subthreshold slope; volume inversion; 2) setting of threshold voltage by the gate work function, thus avoiding dopants and associated number fluctuation effects. To improve the device speed, to minimize short channel effects (SCEs), and to maintain full depletion and improved drain current, a new design by improving the conventional DG MOSFETs becomes important. In this paper, a new design of DG MOSFET called symmetrical gate stack double-gate (GS DG) strained-Si MOSFETs, in which the gate leakage and SCE will be greatly improved, is proposed, for the future ULSI circuits. In the proposed design, the average electric field under the gate further increases and the high density of interface trap states can be reduced using a gate stack structure.[1−3] Also, the strained-Si can improve the device speed.[4,5] To precisely analyse the GS DG strained-Si MOSFET, the exact two-dimensional expressions comprising channel potential, threshold voltage, subthreshold current, and subthreshold swing are needed, especially for the device applied to the integrated circuits. In this paper, based on the exact resultant solution of two-dimensional Poisson's equation, the physics models of channel potential, subthreshold swing, and threshold voltage for symmetrical GS DG strained-Si MOSFET's are developed. And the validity of the analytical model is verified by using the numerical simulation.

2. Strained-Si MOSFET

2.1. Effect of strain on band gap

In the presence of strain, the silicon thin film experiences biaxial tension and changes its band structure.[6−8] The strain causes the electron affinity of silicon to increase, it also causes the band gap and the effective mass of carriers to decrease. The above strain-related effects on the silicon band structure are

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modeled as follows:[9,10]

$$(\Delta E_{\rm C})_{\rm s-Si} = 0.57x, \tag{1}$$

$$(\Delta E_{\rm g})_{\rm s-Si} = 0.4x, \tag{2}$$

$$V_{\rm T}\ln\left(\frac{N_{\rm V,Si}}{N_{\rm V,s-Si}}\right) = V_{\rm T}\ln\left(\frac{m^*_{\rm h,Si}}{m^*_{\rm h,s-Si}}\right)^{3/2} = 0.075x, \tag{3}$$

where x is the strain in equivalent Ge mole fraction in the relaxed SiGe butter layer, $(\Delta E_{\rm C})_{\rm s-Si}$ is the increase in electron affinity of silicon due to strain, $(\Delta E_{\rm g})_{\rm s-Si}$ is the decrease in the bandgap of silicon due to strain, $V_{\rm T}$ is the thermal voltage. $N_{\rm V,Si}$ and $N_{\rm V,s-Si}$ are the density of states (DOS) in the valence band in normal and strained-silicon, respectively; $m^*_{\rm h,Si}$ and $m^*_{\rm h,s-Si}$ are effective masses of hole DOS in normal and strained-silicon, respectively.

2.2. Effect of strain on flatband voltage

Since the structure is symmetrical, the effect of strain on the front-channel flatband and back-channel flatband voltage of MOSFET with this structure can be modeled as follows:[9,10]

$$(V_{\rm FB,f})_{\rm s-Si} = (V_{\rm FB,f})_{\rm Si} + \Delta V_{\rm FB,f}, \tag{4}$$

where

$$(V_{\rm FB,f})_{\rm Si} = \phi_{\rm M} - \phi_{\rm Si},$$

$$\Delta V_{\rm FB,f} = \frac{-(\Delta E_{\rm C})_{\rm s-Si}}{q} + \frac{(\Delta E_{\rm g})_{\rm s-Si}}{q} - V_{\rm T}\ln\left(\frac{N_{\rm V,Si}}{N_{\rm V,s-Si}}\right),$$

$$\phi_{\rm Si} = \chi_{\rm Si}/q + E_{\rm g,Si}/2q + \phi_{\rm f-Si},$$

$$\phi_{\rm f-Si} = V_{\rm T}\ln(N_{\rm A}/n_{\rm i,Si}).$$

In the above relations, $\phi_{\rm M}$ is the gate work function, $\phi_{\rm Si}$ is the work function of unstrained-Si, $\phi_{\rm f-Si}$ is the Fermi potential of unstrained-Si, $E_{\rm g,Si}$ is the band gap of unstrained-Si, q is the electronic charge, $N_{\rm A}$ is the body doping concentration, $n_{\rm i,Si}$ is the intrinsic carrier concentration in unstrained-Si.

It is also important to consider the effect of strain on the built-in voltage across the source-body and drain-body junctions in strained-Si thin film, which can be written as

$$V_{\rm bi,s-Si} = V_{\rm bi,Si} + (\Delta V_{\rm bi})_{\rm s-Si}, \tag{5}$$

where

$$V_{\rm bi,Si} = \frac{E_{\rm g,Si}}{2q} + \phi_{\rm F,Si},$$

$$(\Delta V_{\rm bi})_{\rm s-Si} = \frac{-(\Delta E_{\rm g})_{\rm s-Si}}{q} - V_T\ln\left(\frac{N_{\rm V,Si}}{N_{\rm V,s-Si}}\right).$$

3. Model formulation

3.1. Two-dimensional model for surface potential

The schematic structure of a novel DG strained-Si MOSFET is shown in Fig. 1. The structure is symmetric. Referring to Fig. 1, the Poisson's equation of the potential distribution in the strained silicon film zone before the onset of strong inversion can be written as[11,12]

$$\frac{\partial^2\phi(x,y)}{\partial x^2} + \frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{qN_{\rm A}}{\varepsilon_{\rm Si}}, \quad (0 \le x \le L, \quad 0 \le y \le t_{\rm s-Si}), \tag{6}$$

where $N_{\rm A}$ is the doping concentration of the strained-Si film, $\varepsilon_{\rm Si}$ is the dielectric constant of strained-Si film, $t_{\rm s-Si}$ is the thickness of strained-Si film, the x axis is parallel to the channel, and the y axis is perpendicular to the channel. The potential profile in the vertical direction in the strained-Si film can be approximated by a parabolic function

$$\phi_1(x,y) = \phi_{\rm s}(x) + c_1(x)y + c_2(x)y^2, \quad (0 \le x \le L, \quad 0 \le y \le t_{\rm s-Si}), \tag{7}$$

where $\phi_{\rm s}(x)$ represents the surface potential at the gate-oxide/strained-Si interface. The coefficients $c_1(x)$ and $c_2(x)$ are functions of x. The Poisson's equation can be solved using the following boundary conditions.

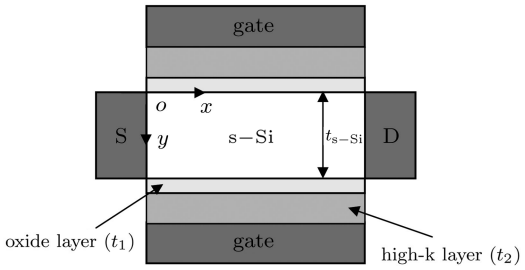


Fig. 1. Schematic structure of DG MOSFET.

(i) Electric flux (displacement) at the gate-oxide/strained-Si film interface of front gate is continuous, i.e.,

$$\left.\frac{{\rm d}\phi(x,y)}{{\rm d}y}\right|_{y=0} = \frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm Si}}\frac{\phi(x,0) - V'_{\rm GS,f}}{t_{\rm f}}, \tag{8}$$

where $\varepsilon_{\rm ox}$ is the dielectric constant of the gate oxide, $t_{\rm f}$ is the effective gate oxide thickness, $t_{\rm f}$ =

$t_1+(\varepsilon_{SiO_2}/k)t_2$. V_{GS} is the gate-to-source bias voltage, $V'_{GS,f} = V_{GS} - (V_{FB,f})_{s-Si}$.

(ii) Electric flux (displacement) at the gate-oxide/strained-Si film interface of bottom gate is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi(x,y)}{\mathrm{d}y}\right|_{y=t_{S-Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V'_{GS,b} - \phi(x,t_{s-Si})}{t_f}, \quad (9)$$

where $V'_{GS,b} = V_{GS} - (V_{FB,f})_{s-Si} = V'_{GS,f} = V'_{GS}$.

(iii) The surface potential at the source end is

$$\phi(0,y) = V_{bi,s-Si}. \quad (10)$$

(iv) The surface potential at the drain end is

$$\phi(L,y) = V_{bi,s-Si} + V_{DS}, \quad (11)$$

where V_{DS} is the drain-to-source bias voltage.

Using the boundary conditions (8), (9), (10), (11) and $\mathrm{d}\phi(x,y)/\mathrm{d}y\,|_{y=(1/2)t_{s-Si}} = 0$, under the symmetry condition of structure, one can obtain the following expression for two-dimensional (2D) channel potential

$$\phi(x,y) = \phi_s(x) + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_s(x) - V'_{GS}}{t_f}y - \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\phi_s(x) - V'_{GS}}{t_f t_{Si}}y^2. \quad (12)$$

Substituting Eq. (12) into Eq. (6), one obtains the differential equation that deals only with the surface potential in the channel strained-Si film

$$\frac{\mathrm{d}^2\phi_s(x)}{\mathrm{d}x^2} - \frac{1}{\lambda^2}\phi_s(x) = D, \quad (13)$$

where

$$\lambda = \sqrt{\varepsilon_{Si}t_f t_{s-Si}/2\varepsilon_{SiO_2}},$$
$$D = \frac{qN_A}{\varepsilon_{Si}} - \frac{1}{\lambda^2}V'_{GS}.$$

The solutions for Eq. (13) are simple second-order non-homogenous differential equations with constant coefficients, which can be written as

$$\phi_{S1}(x) = A\exp(x/\lambda) + B\exp(-x/\lambda) - \lambda^2 D. \quad (14)$$

In the channel strained-Si thin film, the boundary conditions of the surface potential are given as

$$\phi_s(0) = V_{bi,s-Si},$$
$$\phi_s(L) = V_{bi,s-Si} + V_{DS}.$$

Using the boundary conditions, the surface potential can be expressed as

$$A = \frac{\phi_2\,\mathrm{e}^{L/\lambda} - \phi_1}{\mathrm{e}^{2L/\lambda} - 1}, \quad (15)$$

$$B = \frac{\phi_2\,\mathrm{e}^{-L/\lambda} - \phi_1}{\mathrm{e}^{-2L/\lambda} - 1}, \quad (16)$$

where $\phi_2 = V_{bi,s-Si} + V_{DS} + \lambda^2 D$, $\phi_1 = V_{bi,s-Si} + \lambda^2 D$.

The minimum potential can be calculated from Eq. (14)

$$\phi_{s,min} = -\lambda^2 D + 2\sqrt{AB}. \quad (17)$$

The minimum occurs at

$$x_{min} = \frac{1}{2}\lambda\ln\left(\frac{B}{A}\right). \quad (18)$$

The electric field pattern along the channel determines the electron transport velocity through the channel. The electric field horizontal components under the metal gate is given by

$$E(x) = \frac{A}{\lambda}\exp(x/\lambda) - \frac{B}{\lambda}\exp(-x/\lambda). \quad (19)$$

3.2. Two-dimensional model for threshold voltage

The threshold voltage V_{TH} is the value of the gate voltage V_{GS} at which a conducting channel of MOSFET is induced. In a fully depleted thin film symmetric DG MOSFET, it is desirable that the front channel turns on with the back channel. Therefore, the threshold voltage is taken to be that value of gate source voltage for which $\phi_{s,min} = 2\phi_{F,Si}$, where $\phi_{F,Si}$ is the difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. For the strained-Si DG MOSFET, the threshold condition under the front gate is modified as[11,12]

$$\phi_{s,min} = 2\phi_{F,Si} + \Delta\phi_{s-Si} = \phi_{th}, \quad (20)$$

where $\Delta\phi_{s-Si} = -(\Delta E_g)_{s-Si}/q + V_T\ln(N_{V,Si}/N_{V,s-Si})$, ϕ_{th} is the value of surface potential at which the volumetric inversion electron charge density in the strained-Si device is the same as that in the unstrained-Si at threshold, i.e., equal to the body doping. In the case of symmetric DG structure, the threshold voltage is defined as the value of V_{GS} at which the minimum surface potential $\phi_{s,min}$ equals ϕ_{th}. Hence, one can determine the value of threshold voltage as the value of V_{GS} by solving Eq. (17). The threshold voltage can be expressed as follows:

$$V_{TH} = \frac{\lambda^2 qN_A}{\varepsilon_{Si}} + (V_{FB,f})_{s-Si} - \frac{-b + \sqrt{b^2 - 4ac}}{2a}, \quad (21)$$

where

$$a = 2\cosh\left(\frac{2L}{\lambda}\right) - 2\cosh\left(\frac{L}{\lambda}\right),$$

$$b = 4V_{\mathrm{bi,s-Si}} + 2V_{\mathrm{DS}} - 2V_{\mathrm{bi,s-Si}}\cosh\left(\frac{L}{\lambda}\right) - 2(V_{\mathrm{bi,s-Si}} + V_{\mathrm{DS}})\cosh\left(\frac{L}{\lambda}\right) + V_{\mathrm{bi,s-Si}}^2 - \phi_{\mathrm{th}}^2\left(2 - 2\cosh\left(\frac{2L}{\lambda}\right)\right),$$

$$c = (V_{\mathrm{bi,s-Si}} + V_{\mathrm{DS}})^2 - V_{\mathrm{bi,s-Si}}(V_{\mathrm{bi,s-Si}} + V_{\mathrm{DS}})\cosh\left(\frac{L}{\lambda}\right) + V_{\mathrm{bi,s-Si}}^2 - \phi_{\mathrm{th}}^2\left(2 - 2\cosh\left(\frac{2L}{\lambda}\right)\right).$$

3.3. Subthreshold current model

The current flows primarily from the drain to the source and consists of both drift current and diffusion current. The developed 2D potential model can be used to drive an explicit analytical current equation in the subthreshold regime. In the weak inversion region, the current is principally diffusion-dominated and proportional to the electron concentration at the virtual cathode. Therefore, the subthreshold current derived for this DG MOSFET can be expressed as[3]

$$J_n(y) = qD_n\frac{n_{\min}(y)}{L}(1 - \mathrm{e}^{-V_{\mathrm{DS}}/V_{\mathrm{T}}}), \qquad (22)$$

where D_n represents the diffusion constant and V_{T} the thermal voltage. To evaluate the subthreshold current, we need to find the carrier concentration, $n_{\min}(y)$, at the point along the channel where the potential is minimum. Since the minimum potential $\phi_{\min}(y)$ varies with distance from the two gates, we can obtain the value of the minimum potential by replacing $x_{\min}$ in Eq. (18).

Using Botzmann distribution function, the electron density at virtual cathode can be written as

$$n_{\min}(y) = (n_{\mathrm{i}}^2/N_{\mathrm{A}})\,\mathrm{e}^{\phi_{\min}(y)/V_{\mathrm{T}}}, \qquad (23)$$

where n_{i} is the intrinsic free-carrier density. We also have $x = 0$, $n_{\mathrm{i}} = 1.25\times10^{10}$ cm^{-3}; $x = 0.2$, $n_{\mathrm{i}} = 4.02\times10^{10}$ cm^{-3}; $x = 0.4$, $n_{\mathrm{i}} = 45.25\times10^{10}$ cm^{-3}.[13,14]

So the subthreshold current in Fig. 1 can be given as

$$I_{\mathrm{sub}} = 2\frac{KV_{\mathrm{T}}}{E_{\mathrm{S}}}(\mathrm{e}^{\phi_{\min}/V_{\mathrm{T}}} - \mathrm{e}^{\phi_{\mathrm{S\,min}}/V_{\mathrm{T}}}), \qquad (24)$$

where E_{S} represents the constant electric field, $E_{\mathrm{S}} = 2(\phi_{\min} - \phi_{\mathrm{S\,min}})/t_{\mathrm{s-Si}}$; $\phi_{\mathrm{S\,min}}$ is the minimum potential at (strained-Si/SiO_2) interface given by $\phi_{\mathrm{S\,min}} = \phi_{\min}(x_{\min}, 0)$. $\phi_{\min}$ represents the minimum potential $\phi_{\min} = \phi_{\min}(x_{\min}, (1/2)t_{\mathrm{s-Si}})$ and K is a constant defined as $K = (q\mu_n W V_{\mathrm{T}} n_{\mathrm{i}}^2/LN_{\mathrm{A}})(1 - \mathrm{e}^{-V_{\mathrm{DS}}/V_{\mathrm{T}}})$, with W being the width of the DG MOSFET, and the μ_n is the mobility of electron[13,14]

$$\mu_n = \begin{cases} \mu_{0n}\times(1 + 7.969x - 10.90x^2), & (0 \le x \le 0.15); \\ \mu_{0n}\times(1.789 + 1.708x - 2.663x^2), & (0.15 \le x \le 0.4); \end{cases} \qquad (25)$$

$$\mu_{0n} = \mu_{n,\min} + \frac{\mu_{n,\max} - \mu_{n,\min}}{1 + (N_{\mathrm{A}}/N_{r,n})^{\alpha}}, \qquad (26)$$

where $\mu_{n,\max} = 1430$ cm^2/V·s, $\mu_{n,\min} = 55.3$ cm^2/V·s, $N_{r,n} = 1.072\times10^{17}$ cm^{-3}, $\alpha = 0.73$, x is the value of effective Ge mole fraction in relaxed SiGe buffer.

3.4. Subthreshold swing model

Assuming that the drain current, I_{DS}, is proportional to the total amount of the free carriers at the virtual cathode, a general subthreshold swing (S) model can be expressed as

$$S = \frac{\partial V_{\mathrm{GS}}}{\partial \log I_{\mathrm{DS}}} = \left[\frac{\int_0^{t_{\mathrm{s-Si}}/2}\exp(\phi_{\min}/V_{\mathrm{T}})(\partial\phi_{\min}/\partial V_{\mathrm{GS}})\,\mathrm{d}y}{\int_0^{t_{\mathrm{s-Si}}/2}\exp(\phi_{\min}/V_{\mathrm{T}})\,\mathrm{d}y}\right]^{-1} V_{\mathrm{T}}\ln(10). \qquad (27)$$

An approximate solution of the integral (27) is given by[3]

$$S = \frac{KT}{q}\ln(10)\left[\frac{\partial\phi_{\mathrm{s,min}}}{\partial V_{\mathrm{GS}}}\right]^{-1}. \qquad (28)$$

So, for short-channel strained-Si DG MOSFET the subthreshold swing model can be written as

$$S = \frac{KT}{q}\ln(10)\left[1 + \frac{\sinh((x_{\min} - L)/\lambda) - \sinh(x_{\min}/\lambda)}{\sinh(L/\lambda)}\right]^{-1}. \qquad (29)$$

The developed compact subthreshold swing has been used to plot a graphical abacus to study the scaling capability of the proposed DG MSFET structure.

4. Results and discussion

To verify the proposed analytical model, a fully depleted (FD) n-channel gate stack DG strained-Si MOSFET shown in Fig. 1 was used.

Figure 2 shows the curve of surface potential against the horizontal distance in the channel for $L = 20$ nm. It can be seen that the incorporation of GS DG strained-Si design introduces a decrease of the potential barrier with increasing value of effective Ge mole fraction in the relaxed SiGe buffer at the source and drain end.

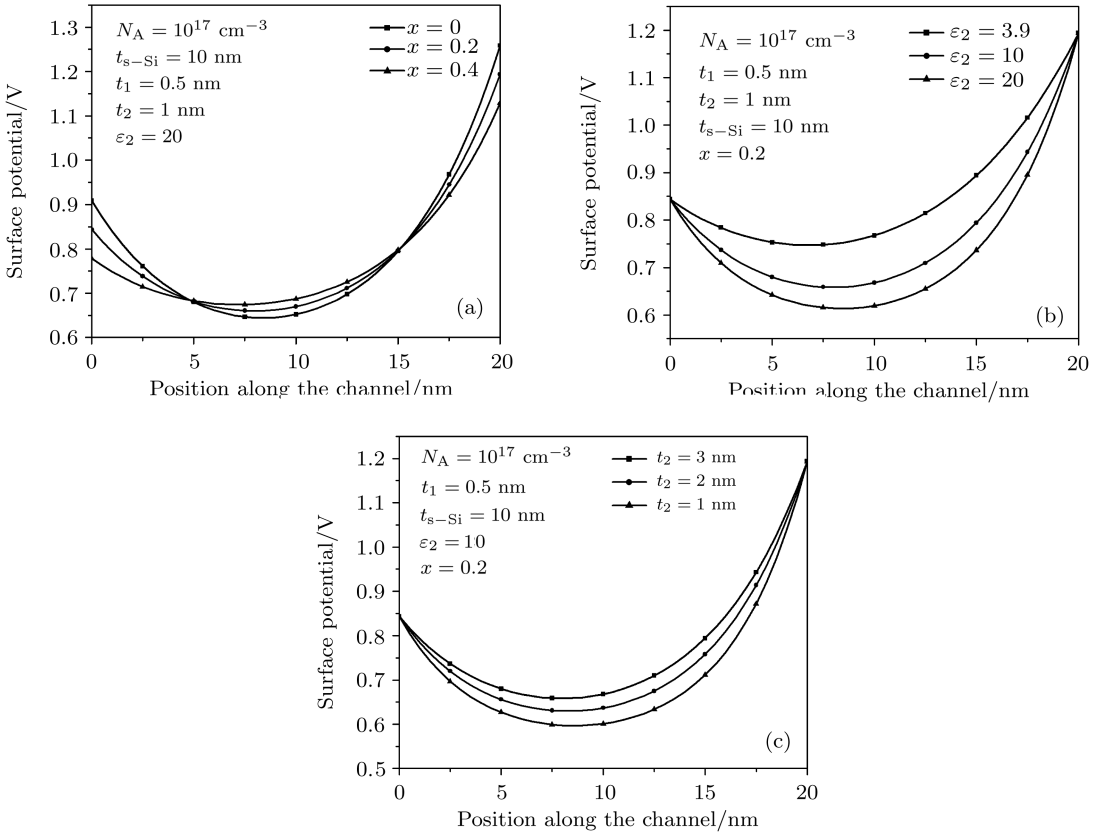


Fig. 2. Variation of surface potential along the channel for a 20-nm GSFD DG strained-Si MOSFET with the position along the channel: (a) for different Ge mole fractions in relaxed SiGe buffer; (b) for different ε_2 ($x = 0.2$); (c) for different t_2 ($x = 0.2$).

However, in the middle of the channel there is an increase of the potential barrier with the increase of the values of effective Ge mole fraction in the relaxed SiGe buffer, as shown in Fig. 2(a). Figure 2(b) shows that the incorporation of GS DG strained-Si design introduces a decrease of the potential barrier with the increase of the permittivity ε_2 for $x = 0.2$. However, this potential barrier is decreased when the high-k thickness t_2 is increased, as shown in Fig. 2(c). The shift in the potential profile screens the region near the source end from the variations in drain voltage and thus ensures reduction in threshold voltage roll-off in comparison with conventional strained-Si DG MOSFETs. Here, the gate stack oxide acts as controlling gate oxide.

Figure 3(a) shows the variation of threshold voltage with the channel length for different values of effective Ge mole fraction in the relaxed SiGe buffer and for a strained-Si thickness of 10 nm. It is observed that short channel effect becomes apparent when the channel length is below 10–15 nm and is marked by the sharp decrease in the V_{TH} value. The gate-

source/drain charge sharing and source-body/drain-body built-in potential barrier lowering due to overlap of the lateral source-body and drain-body depletion regions becomes significant for such short-channel lengths. It is also observed that the threshold voltage is lower for higher strain in the silicon film at a given channel length. It is evident that there is a significant fall in the threshold voltage with increasing strain, and the reduction in $V_{\rm TH}$ is almost linear. The reduction in $V_{\rm TH}$ with increasing Ge content x is due to the decrease in the faltband voltage, the decrease in the source-body/drain-body built-in potential barrier, and an earlier onset of inversion caused by the decrease in $\phi_{\rm th}$. Figure 3(b) compares the threshold voltage roll-off at drain-source bias ($V_{\rm DS} = 0.3$ V) and $x = 0.2$, for different lengths of conventional strained-Si DG MOSFETs. It is shown that the threshold voltage roll-off effect is considerably reduced in the case of GS DG strained-Si MOSFET even at channel lengths down to 10 nm. Moreover, due to the improved gate controllability, GS DG strained-Si MOSFET has a lower threshold voltage than the conventional DG MOSFET which makes it suitable for nanoelectronics digital application.

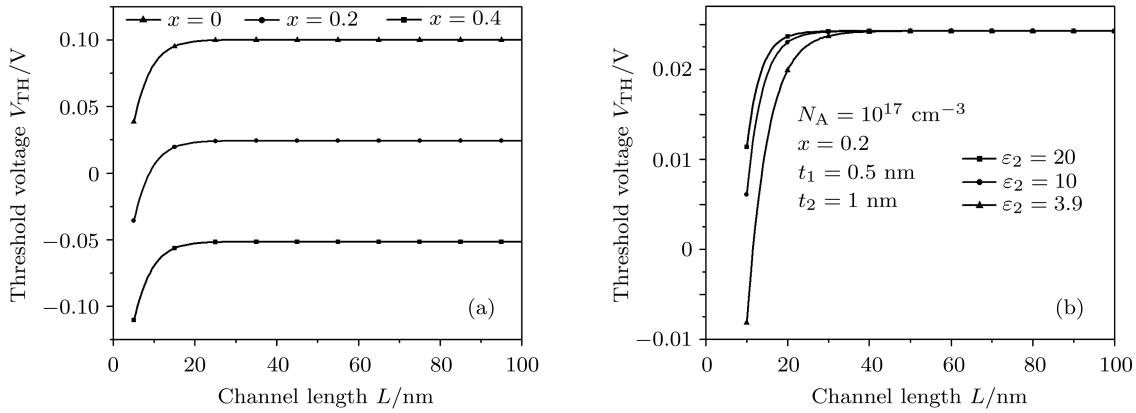


Fig. 3. Calculated threshold voltage of GS DG strained-Si MOSFET as a function of channel length for (a) different Ge mole fraction; (b) different dielectric permittivity ε_2.

Figure 4 shows the variation of DIBL with channel length for different high-k dielectric constant for GS DG MOSFET. The DIBL is obtained from the difference between the threshold voltage at high drain–drain source voltage ($V_{\rm DS} = 0.3$ V) and the threshold voltage value at low drain-drain source voltage ($V_{\rm DS} = 0.1$ V). From Fig. 4, it can be seen that DIBL is lower for GS DG strained-Si MOSFET than for DG strained-Si MOSFET. This indicates the fact that the incorporation of GS DG and high-k designs lead to an improvement of short channel effect.

Figure 5 shows the variation of threshold current with gate voltage for different high-k dielectric constants. It is clearly shown that the subthreshold current reduces as the dielectric constant ε_2 increases. It is noticed that the device with low leakage current and high ratio of $I_{\rm on}/I_{\rm off}$, can provide the circuit with high quality commutation OFF-state to ON-state when it is in digital operation for ULSI application. Therefore, the proposed GS DG strained-Si MOSFET design can be considered as a potential candidate for the nanoscale CMOS-based digital circuits.

Figure 6 shows the evolution of the subthreshold swing for different dielectric constants ε_2 for this novel structure, where the effect of the GS design on the law of scaling capability of the DG MOSFET is presented. Clearly, for equal electrical and geometrical parameters, the GS DG strained-Si MOSFET provides a better subthreshold swing and a small OFF-current with respect to conventional strained-Si MOSFETs.

In addition, it has been found that the scaling capability is improved and the minimal channel length is reduced for $s = 60$ mV/dec. Therefore, this novel structure provides excellent immunity against the short channel effect and enhancement in subthreshold swing compared to the conventional strained-Si DG MOSFET.

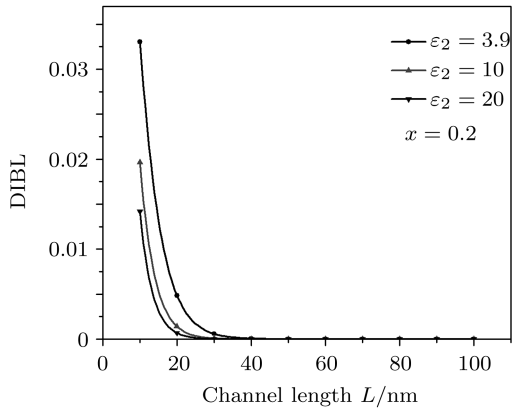


Fig. 4. Drain induced barrier lowing, DIBL, coefficient as a function of the channel length for different dielectric constants ε_2 at $x = 0.2$.

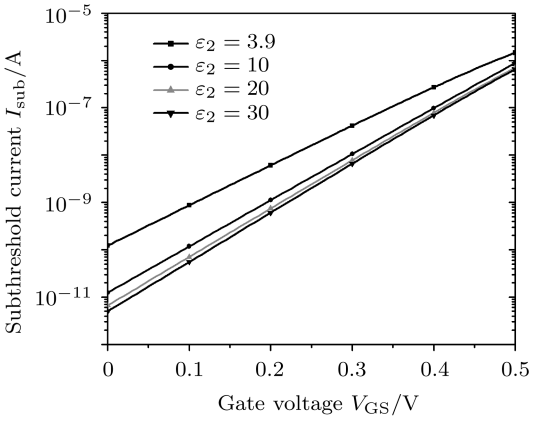


Fig. 5. Subthreshold current variation with gate voltage for different dielectric constant ε_2, ($L = 100$ nm, $t_1 = 0.5$ nm, $t_2 = 1$ nm, $t_{\rm s-Si} = 10$ nm).

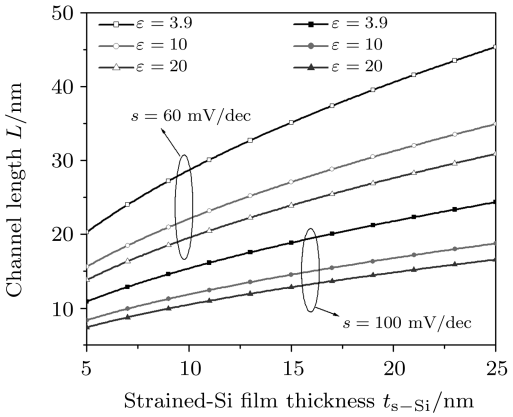


Fig. 6. Graphical abacus which allows studying the scaling capability of the proposed GS DG strained-Si MOSFET.

5. Conclusion

In this paper, the 2D analytical model of surface potential, threshold voltage, subthreshold current and subthreshold swing has been developed for GS DG strained-Si MOSFET. It has been shown that the high-k region on the oxide layer exhibits reduced SCE. The law of scaling capability of the proposed structure was compared with the conventional DG strained-Si MOSFET case, which illustrates the improved subthreshold behaviour of the GS DG strained-Si MOSFET over DG unstrained-Si MOSFET. The obtained results are in good agreement with the simulated results.

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