The study on two-dimensional analytical model for gate stack fully depleted strained Si on silicon-germanium-on-insulator MOSFETs*

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Based on the exact resultant solution of two-dimensional Poisson's equation in strained Si and $Si_{1-X}Ge_X$ layer, a simple and accurate two-dimensional analytical model including surface channel potential, surface channel electric field, threshold voltage and subthreshold swing for fully depleted gate stack strained Si on silicon-germanium-on-insulator (SGOI) MOSFETs has been developed. The results show that this novel structure can suppress the short channel effects (SCE), the drain-induced barrier-lowering (DIBL) and improve the subthreshold performance in nanoelectronics application. The model is verified by numerical simulation. The model provides the basic designing guidance of gate stack strained Si on SGOI MOSFETs.

Keywords: silicon-germanium-on-insulator MOSFETs, strained Si, short channel effects, the drain-induced barrier-lowering

PACC: 7330, 7340Q, 7215N

1. Introduction

As bulk and siliton-on insulator (SOI) MOSFETs scale down into sub-100-nm technology node, the gate oxide thickness is projected to reduce to 1.5 nm or below, such an ultra-thin gate oxide will induce high direct tunneling gate leakage currents,[1,2] which can increase the static power and affect the circuit operation. To solve the problem, the new dielectric materials with high dielectric constant (k) materials such as $HfSiO_4$ ($k = 10$), HfO_2 ($k = 20$) have been recommended to replace SiO_2 for solving the gate leakage problem. However, the interface trap states increase greatly on using the new dielectric materials to replace the gate oxide. So, the best method to solve this problem is using a stack gate structure.[3] Also, the strained Si can improve the device speed.[4,5] To precisely analyse the gate stack strained Si on silicon-germanium-on-insulator (SGOI) MOSFETs, the exact two-dimensional expression comprising channel potential, channel electric field, threshold voltage, and subthreshold swing is needed, especially for the device applied to the integrated circuits. In this paper, based on the exact resultant solution of two-dimensional Poisson's equation, the physics model of channel potential, subthreshold swing and threshold voltage for gate stack (GS) strained Si SGOI MOSFET's are developed. And the validity of the analytical model is verified by using the numerical simulation.

2. Strained-Si-on-insulator MOSFET

2.1. Effect of strain on band-gap

In the presence of strain, the silicon thin film experiences biaxial tension and changes its band structure.[6–8] The strain causes the electron affinity of silicon to increase, it also causes the band-gap and the effective mass of carriers to decrease. The above strain-related effects on the silicon band structure are modeled as follows:[9,10]

$$(\Delta E_{\mathrm{C}})_{\mathrm{s-Si}} = 0.57X, \tag{1}$$

$$(\Delta E_{\mathrm{g}})_{\mathrm{s-Si}} = 0.4X, \tag{2}$$

$$V_{\mathrm{T}} \ln\left(\frac{N_{\mathrm{V,Si}}}{N_{\mathrm{V,s-Si}}}\right) = V_{\mathrm{T}} \ln\left(\frac{m^*_{\mathrm{h,Si}}}{m^*_{\mathrm{h,s-Si}}}\right)^{3/2}$$

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$$= 0.075X, \tag{3}$$

where X is the strain in equivalent Ge mole fraction in the relaxed $Si_{1-X}Ge_X$ butter layer; $(\Delta E_C)_{s-Si}$ is the increase in electron affinity of silicon due to strain, $(\Delta E_g)_{s-Si}$ is the decrease in the band-gap of silicon due to strain, V_T is the thermal voltage. $N_{V,Si}$ and $N_{V,s-Si}$ are the density of states (DOS) in the valence band in normal and strained Si, respectively; $m^*_{h,Si}$ and $m^*_{h,s-Si}$ are effective masses of hole DOS in normal and strained Si, respectively.

The band-gap for the $Si_{1-X}Ge_X$ layer can also be estimated as follows:[9,10]

$$(\Delta E_g)_{SiGe} = 0.467X, \tag{4}$$

$$N_{V,SiGe} = (0.6X + 1.04(1-X)) \times 10^{19}\ \text{cm}^{-3}, \tag{5}$$

$$\varepsilon_{SiGe} = 11.8 + 4.2X, \tag{6}$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,SiGe}}\right) = V_T \ln\left(\frac{1}{1-0.44X}\right), \tag{7}$$

where $(\Delta E_g)_{SiGe}$ is the difference between the band-gap of $Si_{1-X}Ge_X$ and that of Si, $N_{V,SiGe}$ is the DOS in the valence band in the $Si_{1-X}Ge_X$ layer, and ε_{SiGe} is the permittivity of $Si_{1-X}Ge_X$.

2.2. Effect of strain on flatband voltage

The effect of strain on the front-channel flatband voltage of FD SGOI MOSFET can be modeled as follows:[9,10]

$$(V_{FB,f})_{s-Si} = (V_{FB,f})_{Si} + \Delta V_{FB,f}, \tag{8}$$

where $(V_{FB,f})_{Si} = \phi_M - \phi_{Si}$, $\Delta V_{FB,f} = -(\Delta E_C)_{s-Si}/q + (\Delta E_g)_{s-Si}/q - V_T \ln(N_{V,Si}/N_{V,s-Si})$, $\phi_{Si} = \chi_{Si}/q + E_{g,Si}/2q + \phi_{f-Si}$, $\phi_{f-Si} = V_T \ln(N_A/n_{i,Si})$.

In the above relations, ϕ_M is the gate work function, ϕ_{Si} is the work function of unstrained Si, ϕ_{f-Si} is the Fermi potential of unstrained Si, $E_{g,Si}$ is the band-gap of unstrained Si, q is the electronic charge, N_A is the body doping concentration, $n_{i,Si}$ is the intrinsic carrier concentration in unstrained Si. In the same way, the effect of strain on the back-channel flatband voltage of FD SGOI MOSFET is modeled as[9,10]

$$(V_{FB,b})_{SiGe} = (V_{FB,b})_{Si} + \Delta V_{FB,b}, \tag{9}$$

where $(V_{FB,b})_{Si} = \phi_{sub} - \phi_{Si}$, $\Delta V_{FB,b} = (\Delta E_g)_{SiGe}/q - V_T \ln(N_{V,Si}/N_{V,SiGe})$, $\phi_{sub} = \chi_{Si}/q + E_{g,Si}/2q + \phi_{f-sub}$, $\phi_{f-sub} = V_T \ln(N_{sub}/n_{i,Si})$.

Here ϕ_{sub} is the work function of the silicon back-substrate under the buried oxide, ϕ_{f-sub} is the Fermi potential in the silicon back-substrate, and N_{sub} is the doping concentration in the back-substrate.

It is also important to consider the effect of strain on the built-in voltage across the source-body and drain-body junctions in strained Si layer, which can be written as

$$V_{bi,s-Si} = V_{bi,Si} + (\Delta V_{bi})_{s-Si}, \tag{10}$$

where $V_{bi,Si} = E_{g,Si}/2q + \phi_{F,Si}$, $(\Delta V_{bi})_{s-Si} = -(\Delta E_g)_{s-Si}/q - V_T \ln(N_{V,Si}/N_{V,s-Si})$.

3. Model formulation

3.1. Two-dimensional model for surface potential

The schematic structure of novel FD SGOI MOSFET is shown in Fig. 1. Neglecting the effect of the fixed oxide charges on the electrostatics of the channel, the Poisson's equation of the potential distribution in the strained Si layer and $Si_{1-X}Ge_X$ layer before the onset of strong inversion can be written as[11–16]

$$\frac{\partial^2\phi_1(x,y)}{\partial x^2} + \frac{\partial^2\phi_1(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \tag{11}$$

$$\text{for } 0 \le x \le L,\ 0 \le y \le t_{s-Si};$$

$$\frac{\partial^2\phi_2(x,y')}{\partial x^2} + \frac{\partial^2\phi_2(x,y')}{\partial y'^2} = \frac{qN_A}{\varepsilon_{SiGe}} \tag{12}$$

$$\text{for } 0 \le x \le L,\ 0 \le y' \le t_{SiGe};$$

where N_A is the doping concentration of the strained Si layer and $Si_{1-X}Ge_X$ layer, ε_{si} is the dielectric constant of strained Si layer, ε_{siGe} is the dielectric constant of $Si_{1-X}Ge_X$ layer, t_{s-Si} is the thickness of strained Si layer, t_{SiGe} is the thickness of $Si_{1-X}Ge_X$ layer, the X axis is perpendicular to the channel, and the Y, Y' axes are parallel to the channel. The potential profile in the vertical direction in the strained Si layer and the $Si_{1-X}Ge_X$ layer can be approximated by a parabolic function.

$$\phi_1(x,y) = \phi_s(x) + c_{11}(x)y + c_{12}(x)y^2 \tag{13}$$

$$\text{for } 0 \le x \le L,\ 0 \le y \le t_{s-Si};$$

$$\phi_2(x,y') = \phi_b(x) + c_{21}(x)y' + c_{22}(x)y'^2 \tag{14}$$

$$\text{for } 0 \le x \le L,\ 0 \le y' \le t_{SiGe};$$

where $\phi_s(x)$ is the front channel surface potential at the gate-oxide/strained Si interface, $\phi_b(x)$ is the back channel surface potential at the $Si_{1-X}Ge_X$/buried oxide interface. The coefficients $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$, and $c_{22}(x)$ are functions of x only. The Poisson's equation can be solved using the following boundary conditions.

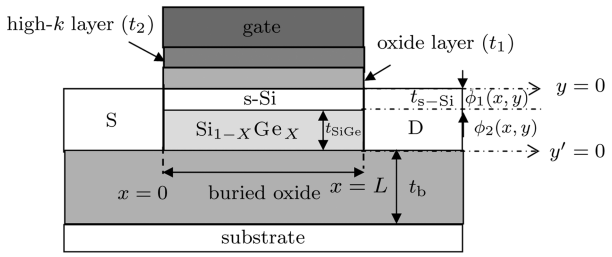


Fig. 1. Schematic structure of SGOI MOSFET.

(i) Electric flux (displacement) at the gate-oxide/strained Si film interface is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y}\right|_{y=0} = \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}}\frac{\phi_{\mathrm{S}}(x)-V'_{\mathrm{GS1}}}{t_{\mathrm{f}}}, \tag{15}$$

where $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the gate oxide, t_{f} is the effective gate oxide thickness $t_{\mathrm{f}} = t_1 + (\varepsilon_{\mathrm{sio_2}}/k)t_2$, V_{GS} is the gate-to-source bias voltage, $V'_{\mathrm{GS1}} = V_{\mathrm{GS}} - (V_{\mathrm{FB,f}})_{\mathrm{s-Si}}$.

(ii) Electric flux at the interface of buried oxide and the $Si_{1-X}Ge_X$ back channel is continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_2(x,y')}{\mathrm{d}y'}\right|_{y'=0} = \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{SiGe}}}\frac{\phi_{\mathrm{b}}(x)-V'_{\mathrm{SUB}}}{t_{\mathrm{b}}}, \tag{16}$$

where t_{b} is the buried-oxide thickness, $V'_{\mathrm{SUB}} = V_{\mathrm{SUB}} - (V_{\mathrm{FB.b}})_{\mathrm{SiGe}}$, V_{SUB} is the substrate bias.

(iii) Electric flux (displacement) and the electric potential at the interface of strained Si layer and $Si_{1-X}Ge_X$ layer are continuous, i.e.,

$$\left.\frac{\mathrm{d}\phi_1(x,y)}{\mathrm{d}y}\right|_{y=t_{\mathrm{s-Si}}} = -\frac{\varepsilon_{\mathrm{SiGe}}}{\varepsilon_{\mathrm{Si}}}\left.\frac{\mathrm{d}\phi_2(x,y')}{\mathrm{d}y}\right|_{y'=t_{\mathrm{SiGe}}}, \tag{17}$$

$$\phi_1(x,t_{\mathrm{s-Si}}) = \phi_2(x,t_{\mathrm{SiGe}}). \tag{18}$$

(iv) The surface potential at the source end is

$$\phi_1(0,0) = \phi_{\mathrm{S1}}(0) = V_{\mathrm{bi,s-Si}}. \tag{19}$$

(v) The surface potential at the drain end is

$$\phi_2(L_1+L_2,0) = \phi_{\mathrm{S2}}(L_1+L_2) = V_{\mathrm{bi,s-Si}} + V_{\mathrm{DS}}, \tag{20}$$

where V_{DS} is the drain-to-source bias voltage.

Using the boundary conditions (15), (16), (17) and (18), one can obtain the coefficients $c_{11}(x)$, $c_{12}(x)$, $c_{21}(x)$, $c_{22}(x)$ in Eqs. (13) and (14), and obtain the expressions for $\phi_1(x,y)$ and $\phi_2(x,y')$. Substituting $\phi_1(x,y)$ and $\phi_2(x,y)$ into Eqs. (11) and (12) respectively and substituting $y=0$, $y'=0$, one can obtain

$$\frac{\mathrm{d}^2\phi_{\mathrm{s}}(x)}{\mathrm{d}x^2} - 2\beta_1\phi_{\mathrm{s}}(x) + 2\alpha_1\phi_{\mathrm{b}}(x) = \delta_1, \tag{21}$$

$$\frac{\mathrm{d}^2\phi_{\mathrm{b}}(x)}{\mathrm{d}x^2} - 2\alpha_2\phi_{\mathrm{b}}(x) + 2b_2\phi_{\mathrm{s}}(x) = \delta_2, \tag{22}$$

where

$$\alpha_1 = \frac{(C_{\mathrm{b}}+2C_{\mathrm{SiGe}})}{2t^2_{\mathrm{s-Si}}(C_{\mathrm{SiGe}}+C_{\mathrm{s-Si}})},\quad \beta_1 = \frac{C_{\mathrm{SiGe}}+C_{\mathrm{f}}(C_{\mathrm{SiGe}}/C_{\mathrm{s-Si}})+(C_{\mathrm{f}}/2)}{t^2_{\mathrm{s-Si}}(C_{\mathrm{s-Si}}+C_{\mathrm{SiGe}})},$$

$$\delta_1 = \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{Si}}} - \left(\frac{C_{\mathrm{f}}(2C_{\mathrm{SiGe}}/C_{\mathrm{s-Si}}+1)V'_{\mathrm{GS}} - C_{\mathrm{b}}V'_{\mathrm{SUB}}}{t^2_{\mathrm{s-Si}}(C_{\mathrm{s-Si}}+C_{\mathrm{SiGe}})}\right),\quad \alpha_2 = \frac{C_{\mathrm{s-Si}}+C_{\mathrm{b}}(C_{\mathrm{Si}}/C_{\mathrm{SiGe}})+(C_{\mathrm{b}}/2)}{2t^2_{\mathrm{SiGe}}(C_{\mathrm{SiGe}}+C_{\mathrm{s-Si}})},$$

$$\beta_2 = \frac{C_{\mathrm{f}}+2C_{\mathrm{s-Si}})}{2t^2_{\mathrm{SiGe}}(C_{\mathrm{s-Si}}+C_{\mathrm{SiGe}})},\quad \delta_2 = \frac{qN_{\mathrm{A}}}{\varepsilon_{\mathrm{SiGe}}} - \left(\frac{C_{\mathrm{b}}(2C_{\mathrm{SiGe}}/C_{\mathrm{s-Si}}+1)V'_{\mathrm{SUB}} - C_{\mathrm{f}}V'_{\mathrm{GS}}}{t^2_{\mathrm{SiGe}}(C_{\mathrm{s-Si}}+C_{\mathrm{SiGe}})}\right).$$

Here, $C_{\mathrm{s-Si}} = \varepsilon_{\mathrm{Si}}/t_{\mathrm{s-Si}}$, $C_{\mathrm{f}} = \varepsilon_{\mathrm{f}}/t_{\mathrm{f}}$, $C_{\mathrm{b}} = \varepsilon_{\mathrm{ox}}/t_{\mathrm{b}}$, $C_{\mathrm{SiGe}} = \varepsilon_{\mathrm{SiGe}}/t_{\mathrm{SiGe}}$.

By eliminating $\phi_{\mathrm{b}}(x)$ from Eqs. (21) and (22), one can obtain

$$\frac{\mathrm{d}^4\phi_{\mathrm{s}}(x)}{\mathrm{d}x^4} - (2\alpha_2+2\beta_1)\frac{\mathrm{d}^2\phi_{\mathrm{s}}(x)}{\mathrm{d}x^2} + 4(\alpha_2\beta_1-\alpha_1\beta_2)\phi_{\mathrm{s}}(x) = -2(\alpha_2\delta_1+\alpha_1\delta_2). \tag{23}$$

To solve the four-order differential equation is too complicated for a simple compact model. The surface potential variation $\phi_{\mathrm{s}}(x)$, across the front channel from the source to the drain, is quite smooth and does not vary rapidly (especially for gate voltage close to the threshold voltage of MOSFET). One can neglect its fourth derivative with respect to the other terms. This approximation is quite valid as one can see in the comparison of model prediction with device simulation results given later. Thus, equation (23) can be written as

$$\frac{\mathrm{d}^2\phi_{\mathrm{s}}(x)}{\mathrm{d}x^2} - \alpha\phi_{\mathrm{s}}(x) = \beta, \tag{24}$$

where $\alpha = 2(\alpha_2\beta_1 - \alpha_1\beta_2)/(\alpha_2+\beta_1)$, $\beta = (\alpha_2\delta_1 - \alpha_1\delta_2)/(\alpha_2+\beta_1)$.

The solution for Eq. (24) is a simple second-order non-homogenous differential equation with constant

coefficients, which can be written as

$$\phi_{\rm s}(x) = A\exp(\omega x) + B\exp(-\omega x) - \delta, \tag{25}$$

where $\omega = \sqrt{\alpha}$ and $\delta = \beta/\alpha$.

Now, using boundary conditions (19) and (20) to solve for A and B, one obtains

$$A = \left[\frac{(V_{\rm bi,s-Si} + \delta + V_{\rm DS}) - (V_{\rm bi,s-Si} + \delta)\exp(-\omega L)}{1 - \exp(-2\omega L)}\right] \times \exp(-\omega L), \tag{26}$$

$$B = \left[\frac{(V_{\rm bi,s-Si} + \delta) - (V_{\rm bi,s-Si} + \delta + V_{\rm DS})\exp(-\omega L)}{1 - \exp(-2\omega L)}\right]. \tag{27}$$

The minimum potential of the front-channel can be calculated from Eq. (21) as

$$\phi_{\rm s,min} = 2\sqrt{AB} - \delta. \tag{28}$$

The minimum occurs at

$$x_{\rm min} = \frac{1}{2\omega}\ln\left(\frac{B}{A}\right). \tag{29}$$

The electric field pattern along the channel determines the electron transport velocity through the channel. The electric field horizontal components under the metal gate is given as

$$E(x) = A\alpha\exp(\alpha x) - B\alpha\exp(-\alpha x). \tag{30}$$

3.2. Two-dimensional model for threshold voltage

The threshold voltage $V_{\rm TH}$ is the value of the gate voltage $V_{\rm GS}$ at which a conducting channel of SOI MOSFET is induced. In a fully depleted thin film SOI, it is desirable that the front channel turns on before the back channel. Therefore, the threshold voltage is taken to be that value of gate source voltage for which $\phi_{\rm s,min} = 2\phi_{\rm F,Si}$, where $\phi_{\rm F,Si}$ is difference between the extrinsic Fermi level in the bulk region and the intrinsic Fermi level. For the strained Si SOI MOSFET, the threshold condition under the front gate is modified as

$$\phi_{\rm s,min} = 2\phi_{\rm F,Si} + \Delta\phi_{\rm s-Si} = \phi_{\rm th}, \tag{31}$$

where

$$\Delta\phi_{\rm s-Si} = -\frac{(\Delta E_{\rm g})_{\rm s-Si}}{q} + V_{\rm T}\ln\left(\frac{N_{\rm V,s-Si}}{N_{\rm V,s-Si}}\right);$$

$\phi_{\rm th}$ is the value of surface potential at which the volumetric inversion electron charge density in the strained Si device is the same as that in the unstrained Si at threshold, i.e., equal to the body doping.

So the threshold voltage is defined as the value of $V_{\rm GS}$ at which the minimum surface potential $\phi_{\rm s,min}$ equals $\phi_{\rm th}$. Hence, one can determine the value of threshold voltage as the value of $V_{\rm GS}$ by solving Eq. (28). Thus the threshold voltage can be expressed as follows:

$$V_{\rm TH} = \lambda\frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma}, \tag{32}$$

where

$$\gamma = \exp(-\omega L), \quad \sigma = 2\cosh(\omega L) - \sinh^2(\omega L) - 2,$$

$$\eta = V_{\rm bi1}\left(1 - \frac{1}{\gamma}\right) + \sinh^2(\omega L)\cdot(2\phi_{\rm th} - 2u) - V_{\rm bi2}(1-\gamma), \quad \xi = V_{\rm bi1}V_{\rm bi2} - \sinh^2(\omega L)\cdot(\phi_{\rm th} - u)^2,$$

$$\varphi_1 = (V_{\rm bi,s-Si} - u)(1-\gamma) + V_{\rm DS}, \quad \varphi_2 = (V_{\rm bi,s-Si} - u)\left(\frac{1}{\gamma} - 1\right) - V_{\rm DS}, \quad u = \frac{C_{\rm b}}{C_{\rm f}}V'_{\rm SUB} - \frac{qN_{\rm A}t_{\rm Si}}{C_{\rm f}} - (V_{\rm FB1})_{\rm s-Si},$$

$$u = \frac{V'_{\rm SUB}}{(\alpha_2\beta_1 - \alpha_1\beta_2)}\left[\frac{\alpha_1 C_{\rm b}(2(C_{\rm SiGe}/C_{\rm s-Si}) + 1)}{2t^2_{\rm SiGe}(C_{\rm s-Si} + C_{\rm SiGe})} - \frac{\alpha_2 C_{\rm b}}{t^2_{\rm s-Si}(C_{\rm s-Si} + C_{\rm SiGe})}\right] - \frac{qN_{\rm A}}{2(\alpha_2\beta_1 - \alpha_1\beta_2)}\left(\frac{\alpha_2}{\varepsilon_{\rm Si}} + \frac{\alpha_1}{\varepsilon_{\rm SiGe}}\right) - (1/\lambda)(V_{\rm FB,f})_{\rm s-Si},$$

$$\lambda = (\alpha_2\beta_1 - \alpha_1\beta_2)\left[\frac{\alpha_2 C_{\rm f}(2(C_{\rm SiGe}/C_{\rm s-Si}) + 1)}{2t^2_{\rm s-Si}(C_{\rm s-Si} + C_{\rm SiGe})} - \frac{\alpha_1 C_{\rm f}}{t^2_{\rm SiGe}(C_{\rm s-Si} + C_{\rm SiGe})}\right]^{-1}.$$

3.3. Model for subthreshold swing

Assuming that the drain current is proportional to the total amount of free electrons at the virtual cathode,[3] the subthreshold swing can be defined as

$$S = \frac{\partial V_{\rm GS}}{\partial \log(I_{\rm d})} \approx \frac{KT}{q} \ln(10) \left(\frac{\partial \phi_{\rm s,min}}{\partial V_{\rm GS}} \right)^{-1}. \tag{33}$$

By substituting Eq. (27) into Eq. (33), the subthreshold swing can be obtained as

$$S = \frac{KT}{q} \ln(10) \left\{ \left[(AB)^{-1/2} \left(\frac{1-\exp(-\omega L)}{1-\exp(-2\omega L)} \exp(-\omega L) B + A \frac{1-\exp(-\omega L)}{1-\exp(-2\omega L)} \right) - 1 \right] \frac{1}{\alpha} \times \left[\frac{\alpha_2}{\alpha_2+\beta_1} \left(-\frac{C_{\rm f}((2C_{\rm SiGe}/C_{\rm s_Si})+1)}{t_{\rm s_Si}^2 (C_{\rm s_Si}+C_{\rm SiGe})} \right) + \frac{\alpha_1}{\alpha_2+\beta_1} \left(\frac{C_{\rm f}}{t_{\rm SiGe}^2 (C_{\rm s_Si}+C_{\rm SiGe})} \right) \right] \right\}^{-1}. \tag{34}$$

4. Results and discussion

To verify the proposed analytical model, an FD n-channel SGOI structure shown in Fig. 1 is used. Typical values of parameters are: work function for gate metal $\phi_{\rm M} = 4.77$ eV, $t_{\rm b} = 100$ nm, $V_{\rm SUB} = 0$ V, $N_{\rm A} = 1 \times 10^{17}$ cm^{-3}, $N_{\rm SUB} = 1 \times 10^{17}$ cm^{-3}.

Figure 2 shows the curve of surface potential against the horizontal distance x in the channel $L = 50$ nm. It can be seen that the incorporation of gate stack SGOI design introduces an increasing of the potential barrier with the increase of the values of Ge mole fraction in the relaxed $Si_{1-X}Ge_X$ buffer at the source and drain end. However, in the middle of the channel, the potential barrier increases with increasing effective Ge mole fraction in the relaxed $Si_{1-X}Ge_X$ buffer, as shown in Fig. 2(a). Figure 2(b) shows the potential barrier decreasing with increase permittivity ε_2 for $x = 0.2$. However, this potential barrier decreases when the high-k thickness t_2 increases, as shown in Fig. 2(c). The shift in the potential profile screens the region near the source end from the variations in drain voltage and thus ensures reduction in threshold voltage roll-off in comparison with conventional strained Si MOSFETs.

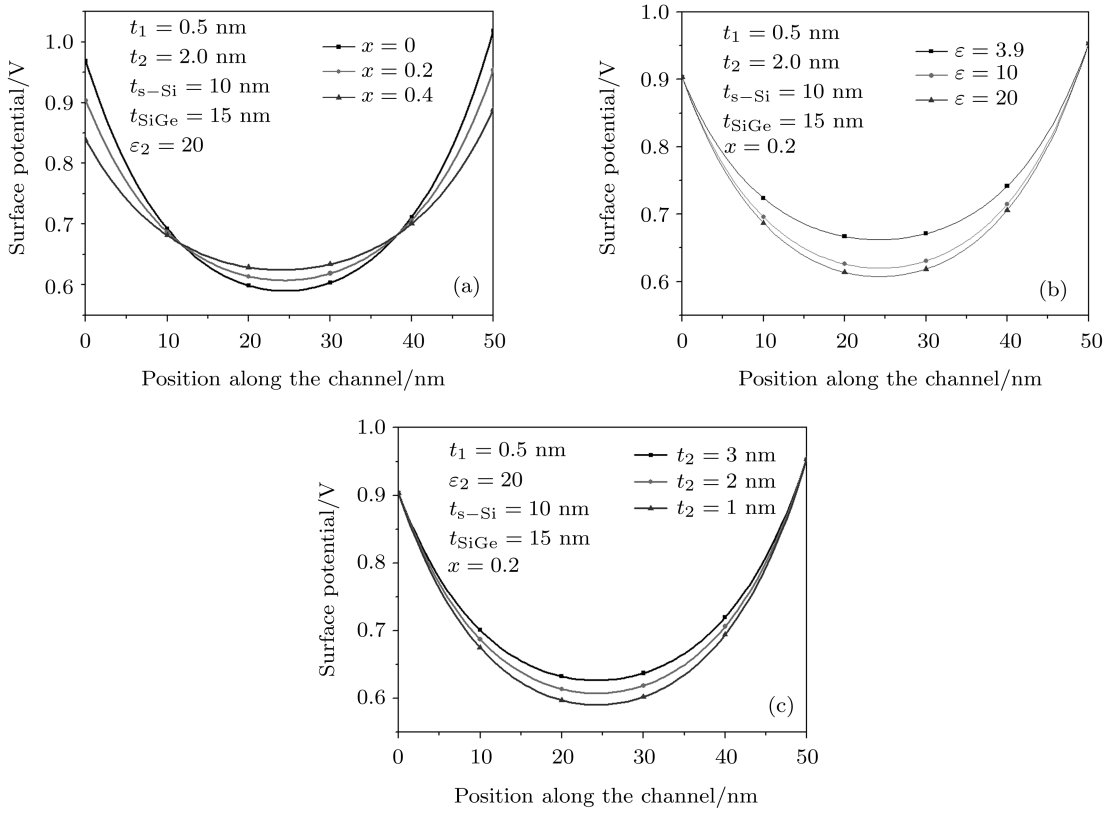


Fig. 2. Variation of surface potential along the channel for a 50-nm GSFDSGOI MOSFET as a function of position along the channel for different (a) Ge mole fraction in relaxed SiGe buffer; (b) high-k dielectric permittivity ε_2 ($x = 0.2$); (c) high-k thickness t_2.

Figure 3 shows the curve of surface electric field against the channel position x in the channel $L = 50$ nm. Figure 3(a) shows the surface electric field increases with increasing Ge mole fraction in the relaxed SiGe buffer at the source end. However, at the drain end the surface electric field decreases with increasing Ge mole fraction in the relaxed SiGe buffer. Figure 3(b) shows the surface electric field changes with the permittivity ε_2. It can be seen that permittivity ε_2 affects the surface electric field not too more than Ge mole fraction in the relaxed SiGe buffer.

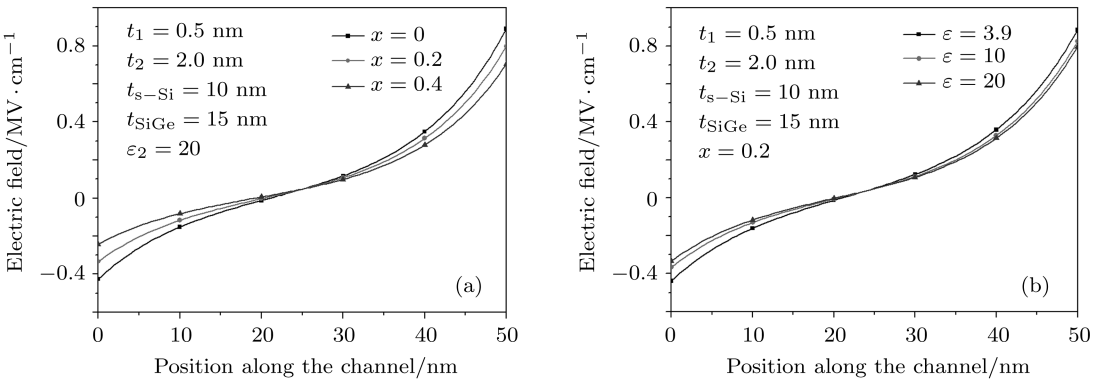


Fig. 3. Variation of surface electric field along the channel for a 50-nm GSFDSGOI MOSFET as a function of position along the channel for different (a) Ge mole fraction in relaxed SiGe buffer; and (b) high-k dielectric permittivity ε_2 ($x = 0.2$).

Figure 4 shows the variation of threshold voltage against the gate length. Figure 4(a) shows the threshold voltage against the gate length for different Ge mole fraction in the $Si_{1-X}Ge_X$ buffer for a strained Si thickness of 10 nm and $Si_{1-X}Ge_X$ thickness of 15 nm. The threshold voltage decreases almost linearly with an increasing strain, it becomes negative for a Ge content of 0.3–0.4. The threshold voltage falls sharply below ∼70 nm gate length due to short-channel effect like drain induced barrier lowing (DIBL), the gate-S/D charge sharing. Figure 4(b) shows the threshold voltage against the gate length for different permittivity ε_2. It is observed that threshold voltage decreases with the increasing of permittivity ε_2.

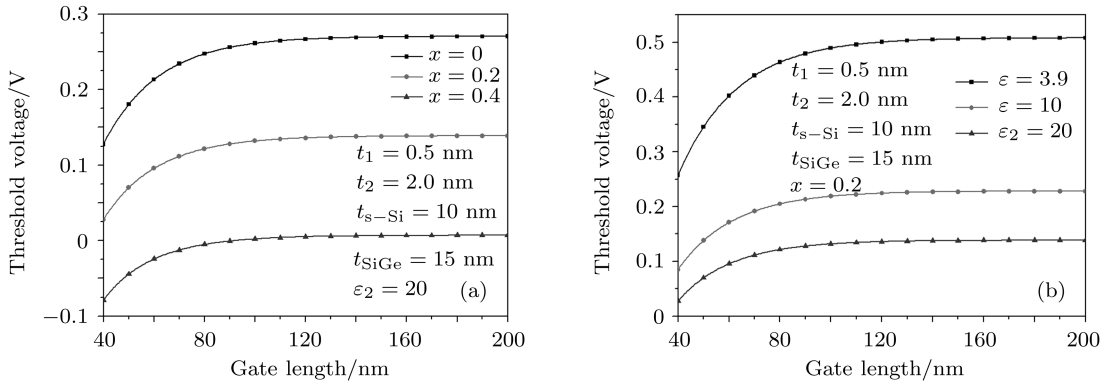


Fig. 4. Variation of threshold voltage along the channel for a 200-nm GSFDSGOI MOSFET as a function of gate length for different (a) Ge mole fraction in relaxed SiGe buffer; and (b) high-k dielectric permittivity ε_2 ($x = 0.2$).

Figure 5 shows the variation of DIBL with channel length for different high-k dielectric permittivity ε_2 for GS FD SGOI MOSFET. The DIBL is obtained from the difference between the threshold voltage at high drain–drain source voltage ($V_{ds} = 0.5$ V) and the threshold voltage value at low drain–drain source voltage ($V_{ds} = 0.05$ V). From Fig. 5, it can be seen that DIBL is lower for GS FD strained Si SGOI MOSFET than for FD SGOI MOSFET. So, it is indicated that the incorporation of GS SGOI and high-k designs leads to an improvement of short channel effect.

Figure 6 shows the subthreshold swing for dielectric constant $\varepsilon_2 = 20$ and $t_{s-Si} = 10$ nm, $t_{siGe} = 15$ nm. For this novel structure, the GS strained Si SGOI MOSFET provides a better subthreshold swing and a small off-current.

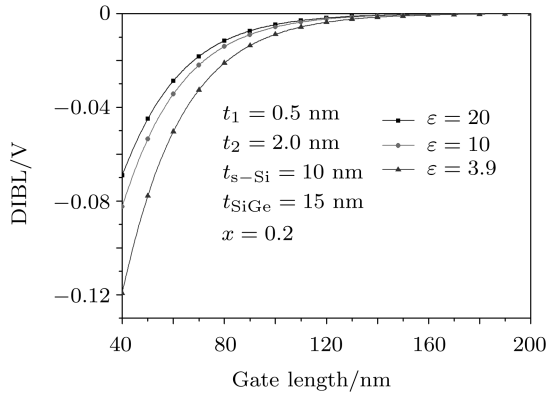


Fig. 5. Drain induced barrier lowering (DIBL) coefficient as a function of the channel length for different dielectric constants ε_2.

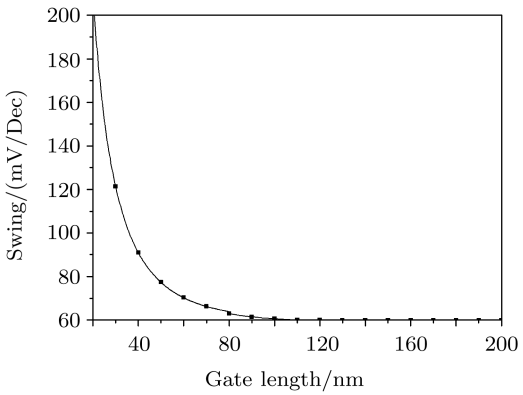


Fig. 6. Variation of threshold voltage with the channel length for a 200-nm GS FD SGOI MOSFET ($x = 0.2$).

5. Conclusion

In this paper, the 2D analytical model of surface potential, threshold voltage, surface electric field and subthreshold swing has been developed for GS SGOI MOSFET. It has been shown that the high-k region on the oxide layer reduces SCE and DIBL. The law of scaling capability of the proposed structure is compared to the conventional strained Si MOSFET, which illustrates the improved subthreshold behaviour of the GS strained Si MOSFET over conventional strained Si MOSFET. The obtained results are in good agreement with the simulated results.

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