Valence band variation in Si (110) nanowire induced by a covered insulator*

Xu Hong-Hua(许洪华)[a], Liu Xiao-Yan(刘晓彦)[a]†, He Yu-Hui(何毓辉)[a], Fan Chun(樊 春)[b], Du Gang(杜 刚)[a], Sun Ai-Dong(孙爱东)[b], Han Ru-Qi(韩汝琦)[a], and Kang Jin-Feng(康晋锋)[a]

[a] *Institute of Microelectronics, Peking University & Key Laboratory of Microelectronic Devices and Circuits, Ministry of Education, Beijing* 100871, *China*

[b] *Computer Center of Peking University, Beijing* 100871, *China*

(Received 4 May 2009; revised manuscript received 30 June 2009)

In this work, we investigate strain effects induced by the deposition of gate dielectrics on the valence band structures in Si (110) nanowire via the simulation of strain distribution and the calculation of a generalized $6\times6\boldsymbol{k}\cdot\boldsymbol{p}$ strained valence band. The nanowire is surrounded by the gate dielectric. Our simulation indicates that the strain of the amorphous SiO_2 insulator is negligible without considering temperature factors. On the other hand, the thermal residual strain in a nanowire with amorphous SiO_2 insulator which has negligible lattice misfit strain pushes the valence subbands upwards by chemical vapour deposition and downwards by thermal oxidation treatment. In contrast with the strain of the amorphous SiO_2 insulator, the strain of the HfO_2 gate insulator in Si (110) nanowire pushes the valence subbands upwards remarkably. The thermal residual strain by HfO_2 insulator contributes to the up-shifting tendency. Our simulation results for valence band shifting and warping in Si nanowires can provide useful guidance for further nanowire device design.

Keywords: silicon nanowire, valence band, thermal residual strain

PACC: 4620, 7115T, 7360F

1. Introduction

As complementary metal-oxide-semiconductor field effect transistors (MOSFETs) go on scaling down, semiconductor nanowires (NWs) have increasingly attracted attention and shown the potential of being next generation electronic devices.[1−4] Many studies have been conducted to explore nanowire (NW) applications, such as photonic, thermoelectric and electric devices.[5−7] One of the most promising techniques for improving device performance is strain induced band engineering, which tunes the nanowire band structures with strain effects. Experimentally, strain can be introduced into NWs via various processes such as the hetero-structure epitaxial process,[8] and the thermal process.[9] Studies on strain induced by lattice mismatch in hetero-structure NWs have been reported.[1,8] As is known, there are lattice mismatches between Si NWs and the coating insulator especially for the case with high K (high dielectric constant) dielectrics. Different kinds of insulators result in different magnitudes and distribution of strain in NWs.[10,11] Besides, taking the SiO_2 dielectric as an example, thermal residual strain originating from the insulator growth process is unavoidable in today's chemical vapour deposition (CVD) and thermal oxidation treatment (TOT) in NW devices. Process parameter variation also gives rise to the changes of thermal expansion coefficients and corresponding total residual strain.[12] However, these strain effects in NWs have not been studied extensively. Thus, it is imperative to study these strain effects on Si NW band structures.

In the present paper, we simulate the strain distributions in SiO_2 and HfO_2-coated Si (110) NWs based on a continuum elasticity model and then calculate valence band structures in Si (110) NW by a generalized $6\times6\boldsymbol{k}\cdot\boldsymbol{p}$ method.[13−15] Two typical cases of the strain induced by the insulator are investigated. Firstly, we discuss the lattice misfit strain modulation by calculating valence band structures in gate dielectric such as amorphous SiO_2, HfO_2 insulator-covered Si (110) NW. Secondly, the effects of thermal residual strain on valence subbands in Si (110) NW with amorphous SiO_2 and HfO_2 insulators are computed.

*Project supported by the National Basic Research Program of China (Grant No. 2006CB302705) and the Foundation for Key Program of Ministry of Education, China (Grant No. 107003).

†Corresponding author. E-mail: xyliu@ime.pku.edu.cn

© 2010 Chinese Physical Society and IOP Publishing Ltd

The influence of strain on the effective masses within the parabolic approximation is also investigated.

2. Computational method

First of all, consider the nanowire growth orientation. We make a coordinate transformation from the ordinary coordinates where $\boldsymbol{e}'_x = [1\ 0\ 0]$, $\boldsymbol{e}'_y = [0\ 1\ 0]$ and $\boldsymbol{e}'_z = [0\ 0\ 1]$, to new coordinates where $\boldsymbol{e}_x = [1\ 1\ -\sqrt{2}]/2$, $\boldsymbol{e}_y = [-1\ 1\ -\sqrt{2}]/2$, $\boldsymbol{e}_z = [1\ 1\ 0]/\sqrt{2}$ in Si (110) NW. The strain tensor is then transformed into new coordinates according to the following equation:

$$\varepsilon_{ij} = (\boldsymbol{e}_i \cdot \boldsymbol{e}'_l)\varepsilon'_{lm}(\boldsymbol{e}'_m \cdot \boldsymbol{e}_j). \tag{1}$$

In the above expression, ε_{ij} (ε'_{lm}) and $\boldsymbol{e}_i$ ($\boldsymbol{e}'_l$) are the strain tensor and basic vector in the new (original) coordinate system. Here we assume that the insulator material is isotropic. Therefore, the total strain energy U can be written as two parts, $U_{\rm Si}$ in Si NW and $U_{\rm I}$ in covered SiO_2 insulator:[15]

$$U = U_{\rm Si} + U_{\rm I} \tag{2}$$

$$\begin{aligned} U_{\rm Si} = \frac{1}{2}\iint_{\rm Si} {\rm d}s\Big\{ & D_1(\varepsilon_{xx}^2 + \varepsilon_{yy}^2) + D_2\left(\frac{a_z}{a_z^0} - 1\right)^2 \\ & + D_3\varepsilon_{xx}\varepsilon_{yy} + D_4(\varepsilon_{xx} + \varepsilon_{yy})\left(\frac{a_z}{a_z^0} - 1\right) \\ & + D_5\varepsilon_{xy}^2 + D_6(\varepsilon_{xx} + \varepsilon_{yy})\varepsilon_{xy}\Big\}, \end{aligned} \tag{3}$$

$$\begin{aligned} U_{\rm I} = \frac{1}{2}\iint_{\rm I} {\rm d}s\Big\{ & D'_1[(\varepsilon_{xx} - \varepsilon_{xx}^S)^2 + (\varepsilon_{yy} - \varepsilon_{yy}^S)^2] \\ & + D'_2\left(\frac{a_z}{a_z^0} - 1 - \varepsilon_{zz}^S\right) \\ & + D'_3(\varepsilon_{xx} - \varepsilon_{xx}^S)(\varepsilon_{yy} - \varepsilon_{yy}^S), \\ & + D'_4[(\varepsilon_{xx} - \varepsilon_{xx}^S) + (\varepsilon_{yy} - \varepsilon_{yy}^S)] \\ & \times \left(\frac{a_z}{a_z^0} - 1 - \varepsilon_{zz}^S\right) + D'_5(\varepsilon_{xy} - \varepsilon_{xy}^S)^2\Big\}, \end{aligned} \tag{4}$$

where D_i is the coordinate transform result of silicon strain tensor modulus C_{ij}:

$$\begin{aligned} D_1 &= \frac{3C_{11} + 5C_{12}}{8} + \frac{5}{16}C_{44}; \\ D_2 &= \frac{C_{11} + C_{12}}{2} + \frac{1}{4}C_{44}; \\ D_3 &= \frac{3C_{11} + 5C_{12}}{4} - \frac{3}{8}C_{44}; \\ D_4 &= \frac{C_{11} + 3C_{12}}{2} - \frac{1}{4}C_{44}; \\ D_5 &= \frac{3}{2}(C_{11} - C_{12}) + \frac{C_{44}}{4}; \\ D_6 &= \frac{C_{11} - C_{12}}{2} - \frac{1}{4}C_{44}; \end{aligned} \tag{5}$$

D'_i is the coordinate transform result of SiO_2 Young modulus E and Poisson ratio ν:

$$\begin{aligned} D'_1 &= D'_2 = \frac{E(1-\nu)}{(1+\nu)(1-2\nu)}; \\ D'_3 &= D'_4 = \frac{2E\nu}{(1+\nu)(1-2\nu)}; \\ D'_5 &= \frac{2E}{(1+v)}; \quad \varepsilon_{ii}^S = \frac{a_i^S}{a_z^0} - 1; \\ a'_{\rm silicon} &= a_z^0 + \Delta s, \quad \Delta s = s_{\rm high} - s_{\rm low}, \end{aligned} \tag{6}$$

where ε_{ij} are the silicon strain tensors; ε_{ij}^S are the gate dielectric strain tensors; a_z^0 is the lattice parameter of silicon crystal without thermal effects; C_{11}, C_{12} and C_{44} are the strain tensor modulus of silicon crystal, respectively; E is the Young modulus; v is the Poisson ratio of bulk insulator material; $a'_{\rm silicon}$ is the lattice parameter with taking into account the residual thermal strain; $S_{\rm high}$ is the silicon residual strain at high temperature; $S_{\rm low}$ is the silicon residual strain at low temperature; Δs is the difference in temperature.

The coefficient of thermal expansion $\alpha(T)$ of silicon is expressed as[16]

$$\begin{aligned} \alpha(T) = (3.725 - 3.725 \times {\rm e}^{-5.88\times(T-124)\times10^{-3}} \\ + 5.548 \times 10^{-4} \times T) \times 10^{-6}/{\rm K}. \end{aligned} \tag{7}$$

On the other hand, $\alpha(T)$ of SiO_2 by CVD is 4.1×10^{-6}/K, while $\alpha(T)$ by TOT SiO_2 is

$$\alpha'(T) = (0.5 + 0.002674 \times T) \times 10^{-6}/{\rm K}, \tag{8}$$

where T is the process temperature, and $\alpha(T)$ of HfO_2 is 6.5×10^{-6}/K.[17] The residual strain is an integral of the coefficient of thermal expansion using expressions (7) and (8). Then, the strain energy distribution and strain tensor can be calculated by the finite element method as expressions (2)–(4).

We compute the valence band structure of Si (110) NW by using a $6 \times 6\boldsymbol{k} \cdot p$ method and selecting the Bessel function as basis functions.[14,15]

3. Results and discussion

As is known, lattice mismatch or the variation of the thermal expansion coefficient is unavoidable between two different materials, thereby inducing a strain effect and further affecting the device performance. In this paper, the lattice misfit and the thermal residual strain are discussed, separately. First, we calculate the valence subbands in pure silicon (110) NW with 5 nm radius as shown in Fig. 1(a). The amorphous SiO_2 insulator and HfO_2 insulator are isotropic. The lattice constants of silicon crystal and

amorphous SiO_2 material are assumed to be identical. The lattice mismatch case without thermal residual strain is shown in Figs. 1(b) and 1(c). Figure 1(b) shows the valence subbands of pure Si (110) NW and NW with 2 nm thick amorphous SiO_2 insulator. Obviously, the valence subbands are completely matched. Our simulation also indicates that valence band structures of Si (110) NW and NW with 2 nm thick amorphous insulator deposited by CVD and TOT are also the same. The different processes have no influence on valence subband even though the Young modulus of the amorphous SiO_2 gate dielectric is different.

With the MOS scaling down, the high-K dielectric attracts more and more attention, owing to the restraining of gate leakage and process compatibility. In NW FET, the high K dielectric such as HfO_2 is widely used. Figure 1(c) shows the valence band structures in Si (110) NW with 4 nm thick HfO_2 dielectric without considering temperature factors. After depositing the HfO_2 dielectric, the valence subbands in Si (110) NW shift upwards remarkably and warp. We have reported that the upshifting tendency is more visible as the HfO_2 dielectric becomes thicker.[18]

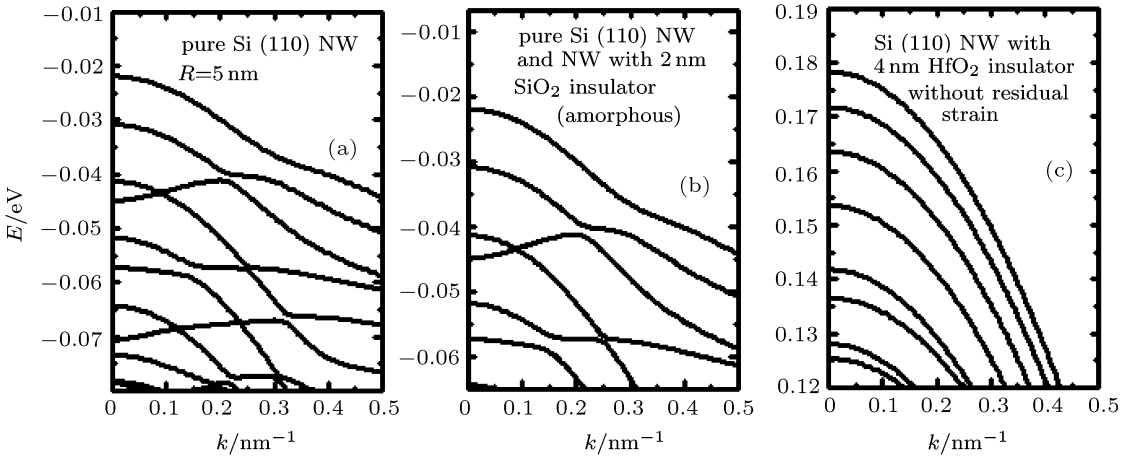


Fig. 1. Valence subbands in (a) pure Si (110) NW with 5 nm radius, (b) pure Si (110) NW and Si (110) NW with 2 nm amorphous SiO_2 insulator (complete superposition), and (c) 4 nm HfO_2 insulator-covered Si (110) NW without including thermal residual strain.

For the thermal residual strain case, the SiO_2 insulator in NW is amorphous and the lattice misfit strain does not exist. Figures 2(a) and 2(b) illustrate Si (110) NW and NW with 2 nm thick SiO_2, with the residual thermal strain taken into consideration, deposited by CVD (a) and TOT (b), respectively. Figure 2(a) shows that the subbands slightly shift upwards by CVD. But Fig. 2(b) shows that the subbands shift downwards by TOT. The shifting tendency to different extents results from different thermal strain effects. The thermal expansion coefficient of SiO_2 insulator by CVD is given as 4.1×10^{-6}/K, which is larger than that of crystal silicon (2.9×10^{-6}/K). The difference in temperature between deposition and typical operation can lead to a compressive thermal strain to the Si (110) NW. However, the thermal expansion coefficient of SiO_2 in the TOT process is smaller than that of crystal silicon at a higher temperature according to expressions (7) and (8). Then the difference in the TOT process induces a tensile thermal strain in contrast with the CVD process. Figure 2(c) shows valence subbands in Si (110) NW with 4 nm thick HfO_2 insulator deposited at 523 K. Compared with the case of HfO_2-covered NW without thermal residual strain as shown in Fig. 1(c), the subbands shift toward high energy positions. The phenomenon is caused merely by the residual strain of HfO_2 insulator. Figure 2 also shows that the thermal residual strain modulating the valence band structures should not be ignored. Therefore, when considering how the insulator modulates the energy bands in NW, we should simultaneously take into account the lattice mismatch strain and residual strain.

For comparison with amorphous SiO_2 insulator, the difference in the valence subband modulated by HfO_2 insulator is caused by lattice mismatch, thermal residual strain and different Young moduli. In the present work, the covered insulator effect comes from all radial directions. The uniaxial effect from source and drain

can be approximately regarded as a strain effect in the z axis direction. The upward tendency due to the gate-all-around insulator is in accordance with calculations by using the Boykin formalism.[7]

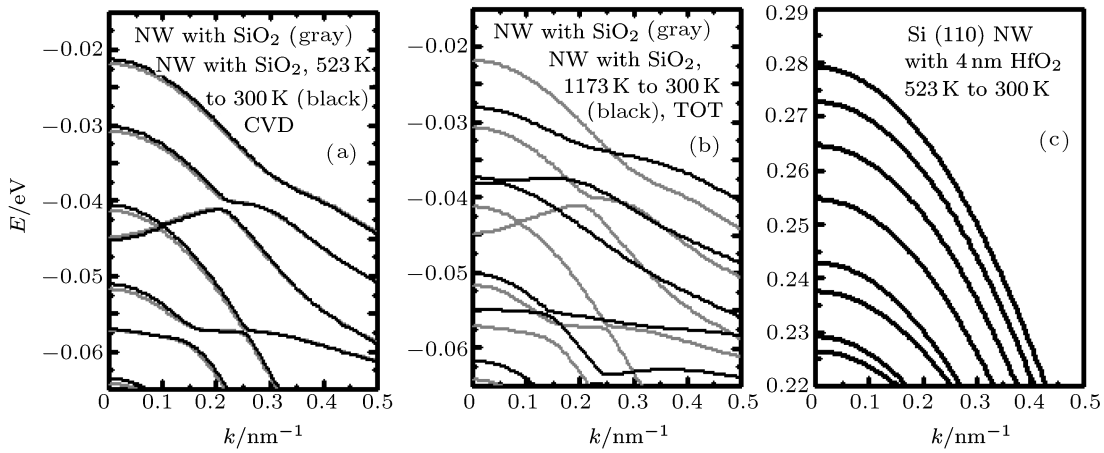


Fig. 2. Valence band structures in Si (110) NW with different kinds of gate insulators, i.e. (a) amorphous SiO_2 insulator (2 nm) deposited by CVD, (b) amorphous SiO_2 insulator (2 nm) deposited by TOT, (c) HfO_2 insulator deposited at 523 K (4 nm). Grey and black lines are for the valence band structures without and with considering thermal residual strains respectively.

As is shown above, the insulator inevitably brings a strain into Si NW. Valence band structure variation corresponds to the change of effective mass, which might guide device optimization. Figure 3 shows effective masses of the top five subbands in amorphous SiO_2-covered Si (110) NW in two processes. Pure Si NW and amorphous SiO_2-covered NW have the same band structures and effective masses. However, considering the residual strain, effective masses of the 1st,

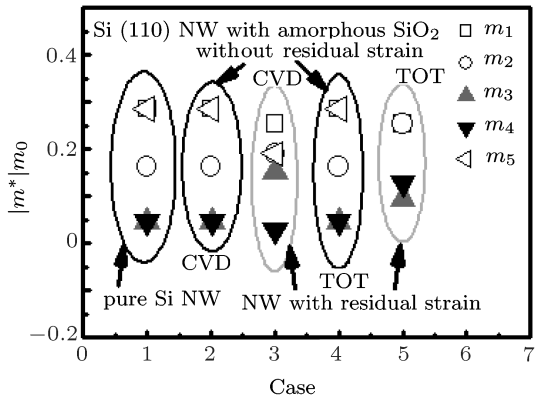


Fig. 3. Effective masses of the top five valence subbands in amorphous SiO_2-coated Si (110) NW versus residual strain effects within two processes.

4th and 5th subbands reduce, but those of the 2nd and 3rd subbands increase by the CVD process. By the TOT process, the effective mass of only the 1st subband reduces, but the all other subbands increase. The hole effective mass changes, owing to the thermal residual strain induced by the process temperature.

From the point of view of another process, the precursor gas ratio can bring about variations of the coefficient of thermal expansion $\alpha(T)$ and the thermal residual strain. Figure 4 shows effective masses of the top five subbands versus the coefficient of thermal expansion $\alpha(T)$ of amorphous SiO_2 deposited by CVD. According to expression (8), $\alpha(T)$ of SiO_2 deposited by TOT is between 3.174×10^{-6}/K at 1000 K and 4.511×10^{-6}/K at 1500 K. Our discussion below naturally involves the TOT process. With the increase of $\alpha(T)$, the effective masses of the 1st and 2nd subbands increase in the range of $\alpha(T) < 2\times10^{-6}$/K, then reduce and increase again

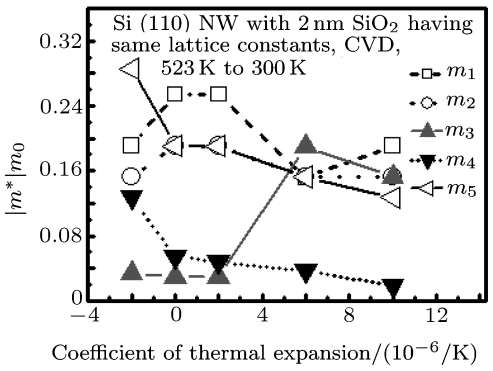


Fig. 4. Effective masses of the top five valence subbands each as a function of the thermal expansion coefficient of amorphous SiO_2 insulator prepared by CVD (the coefficient of the TOT insulator is naturally between 3.174×10^{-6}/K and 4.511×10^{-6}/K.

up to 10×10^{-6}/K. The effective mass of the 3rd sub-

band increases and then reduces. The effective masses of the 4th and 5th subbands reduce in a similar way. Thus selecting a proper ratio is a feasible method to modulate the energy band.[17]

Figure 5 shows the effective masses of the top five subbands in HfO_2-covered Si (110) NW. Compared with the effective mass of pure Si (110) NW, all effective masses of HfO_2 insulator reduce, owing to the HfO_2 insulator modulation. As the HfO_2 thickness increases, the effective mass of the 1st subband increases while that of the 4th subband reduces. The 2nd and 3rd subbands change only slightly. The covered high-K insulator inevitably modulates hole effective masses. Then, heavy holes under strain modulation can turn into light holes, which are very useful for enhancing the hole mobility in transport.

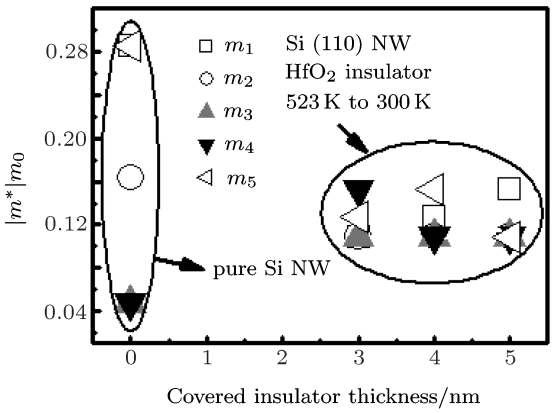


Fig. 5. Hole effective masses of the top five subbands versus covered HfO_2 insulator thickness.

4. Conclusion

The thermal residual strain can modulate the valence subbands in amorphous SiO_2-covered Si (110) NW, and the lattice mismatch strain effect on the band structure is negligible. In NW with amorphous SiO_2 insulator, this is a good way to optimize the process parameters, such as temperature and precursor gas ratio, and further modulate the band structure. But in Si (110) NW with HfO_2 gate dielectric, the up-shifting tendency of subbands is caused by lattice mismatch strain along with thermal residual strain. Therefore, valence band structures modulated by the covered gate insulator provide guidance in the design of higher performance nanowire devices.

References

[1] Cui Y, Wei Q Q, Park H K and Lieber C M 2001 *Science* **293** 1289

[2] Gudiksen M S, Lauhon L J, Wang J, Smith D C and Lieber C M 2002 *Nature* **415** 617

[3] Cui Y and Lieber C M 2001 *Science* **291** 851

[4] Zhang L D, Meng G W and Phillipp F 2001 *Chin. Phys.* **10** 117

[5] Ungersboeck E, Dhar S, Karlowatz G, Sverdlov V, Kosina H and Selberherr S 2007 *IEEE Trans. Electron. Device. Lett.* 54 2183

[6] Khakifirooz A and Antoniadis D A 2006 *IEEE Trans. Electron. Device. Lett.* **27** 402

[7] Sajjad R N and Alam K 2009 *J. Appl. Phys.* **105** 044307

[8] Welser J, Hoyt J L and Gibbons J F 1992 *IEEE Technical Digest-International Electron Devices Meeting* (New York) p1000

[9] Shimizu A, Hachimine K, Ohki N, Ohta H, Koguchi M, Nonaka Y, Sato H and Ootsuka F 2001 *IEEE Technical Digest-International Electron Devices Meeting* (New York) p433

[10] Sinha A K, Levinstein H J and Smith T E 1978 *J. Appl. Phys.* **49** 2423

[11] Carlotti G, Doucet L and Dupeux M 1997 *Thin Solid Films* **296** 102

[12] Jansen F, Machonkin M A, Palmieri N and Kuhman D 1987 *J. Appl. Phys.* **62** 4732

[13] Lin G J, Lai H K, Li C, Chen S Y and Yu J Z 2008 *Chin. Phys.* B **17** 3479

[14] He Y H, Zhao Y N, Yu S M, Fan C, Du G, Kang J F, Han R Q and Liu X Y 2008 *IEEE Technical Digest-International Electron Devices Meeting* p189–192

[15] He Y H, Fan C, Zhao Y N, Du G, Kang J F, Liu X Y and Han R Q 2008 *Int. Conf. on Simulation of Semiconductor Processes and Devices* (SISPAD 2008) p121

[16] Okada Y and Tokumaru Y 1984 *J. Appl. Phys.* **56** 314

[17] Slack G A and Bartram S F 1974 *J. Appl. Phys.* **46** 89

[18] Xu H H, He Y H, Fan C, Zhao Y N, Du G, Kang J F, Han R Q and Liu X Y 2009 *Int. Conf. on Simulation of Semiconductor Processes and Devices* (SISPAD 2009) San Diego, California, USA September 9–11, 2009 pp. 245–248