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Simulation of grain boundary effect on characteristics of ZnO thin film transistor by considering the location and orientation of grain boundary*

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The grain boundaries (GBs) have a strong effect on the electric properties of ZnO thin film transistors (TFTs). A novel grain boundary model was developed to analyse the effect. The model was characterized with different angles between the orientation of the grain boundary and the channel direction. The potential barriers formed by the grain boundaries increase with the increase of the grain boundary angle, so the degradation of the transistor characteristics increases. When a grain boundary is close to the drain edge, the potential barrier height reduces, so the electric properties were improved.

Keywords: simulation, ZnO thin film transistor, grain boundary
PACC: 7125, 7280E

1. Introduction

Thin film transistors (TFTs) have been widely used in flat panel displays. The channel layer of TFTs plays an important role in the device, which can determine the TFTs performance and its applications. ZnO is a transparent compound semiconductor with a wide band gap 3.4 eV, therefore, ZnO is considered to be an ideal material for serving as the channel layer in transparent and flexible TFTs.[1−4] Several methods are adopted to acquire high quality ZnO thin film, such as the sol–gel technique,[5] pulsed laser deposition (PLD),[6] chemical vapour deposition (CVD),[7] and so on. Usually, the ZnO thin film has a polycrystalline structure.

As the transition region between grains within a polycrystalline film, the grain boundaries (GBs) have a strong effect on the transistor characteristics.[8−12] Several works had been done to analyse the effect of the grain boundary location and grain boundary number on the ZnO TFT performance by means of device simulation.[13−17] In these works, the grain boundary is defined as a smaller planar region which is located within the channel and perpendicular to the direction of the channel. In this paper, a novel grain boundary model is developed, which not only has an alterable location but also has an alterable angle. With this model, we explored the effect of the location and the angle of the grain boundary on the ZnO TFT characteristics, using the device simulator. It is found that the potential barrier height is dependent on the variation of the grain boundary angle, and thus the transistor characteristic varies. In addition, we also investigated the dependence of the transistor characteristics on the location of the grain boundary.

2. Simulation approach

In previous works to explore the effect of grain boundary on TFT performance, the commercial two-dimensional (2D) device simulator ATLAS (vended by SILVACO, Inc), was usually used.[14,16,17] However, only an orthogonal rectangle region can be defined by ATLAS. Another commercial module from SILVACO, DEVEDIT, is a structure editor, which can define not only the orthogonal rectangle region but also the asymmetric rectangle region. In our work, the struc-

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ture of the simulated device is edited by DEVEDIT, including parameters such as device size, mesh size, impurity specification, and so on. The standard structure file (SSF) is saved and subsequently loaded by ATLAS. A key parameter describing the activities of the grain boundary, trap states, is defined in ATLAS.

Figure 1 shows the structure of a ZnO TFT for two-dimensional (2D) device simulation. The TFT is a n-channel, channel length = 4 μm, ZnO channel layer thickness = 50 nm, gate insulator thickness = 400 nm. The source and drain are n^+ doped; θ is the angle between the orientation of the grain boundary and the channel direction, defined as the grain boundary angle; d is the distance of the grain boundary from the source edge. Typically, the width of the grain boundary is about 1 nm. In order to precisely simulate the behaviour of the grain boundary, we take the minimum mesh size to be 1 nm, and at the same time refine the mesh of the grain boundary region and the ZnO–Si_3N_4 interface. In our simulation, it is assumed that there are no trap states in the ZnO–Si_3N_4 interface, and the density of trap states within all grain boundaries is the same.

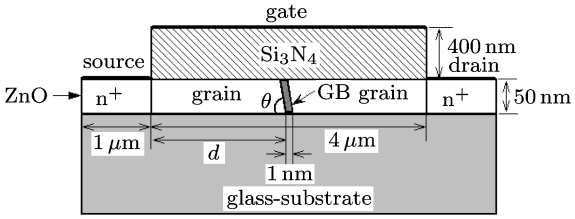


Fig.1. The structure of ZnO TFT for two-dimension device simulation.

3. Simulation results and discussions

As is well known, grain boundaries are characterized by a wide distribution of deep-level trap states; when these traps are charged, a potential barrier is produced. In the case of the same channel doping concentration, the potential height is mainly determined by the density of trap states within the grain boundary.[18,19] When a drain–source voltage is applied, a potential drop occurs across the grain boundary and a high electric field forms, which hinders the motion of carriers and degrades the characteristics of ZnO TFTs.

Figure 2 shows the energy band diagram at the ZnO–Si_3N_4 interface without any bias on the electrodes. Here, the energy band diagram in the case when there is no grain boundary and the energy band diagrams for four values of θ are plotted, these values are 5°, 30°, 60°, 90° respectively, at the same time, the grain boundary is located at the centre of the channel.

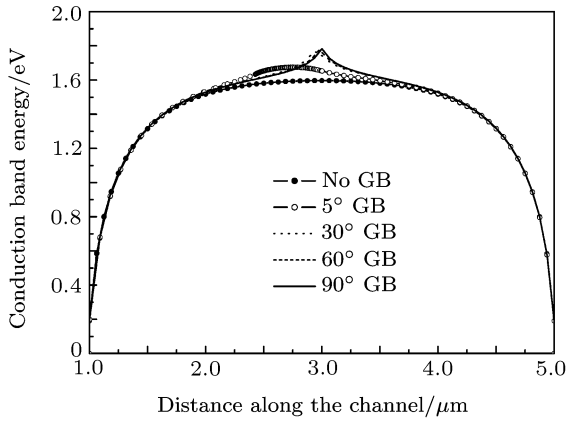


Fig.2. Conduction band diagram at the ZnO–Si_3O_4 interface along the channel for no applied bias.

Among all the grain boundaries, the 90° grain boundary has the highest potential barrier. Although the number of trap states in a smaller angle grain boundary is larger than that in a larger angle one, the overlap of potential barriers in a smaller angle grain boundary is less, so the potential barrier height is lower. Figure 3 shows the transfer characteristics of ZnO TFT with the grain boundary angle of 5°, 30°, 60°, 90°, in addition, the curve of the transistor without grain boundary is also shown. The drain–source voltage of $V_{ds} = 5$ V.

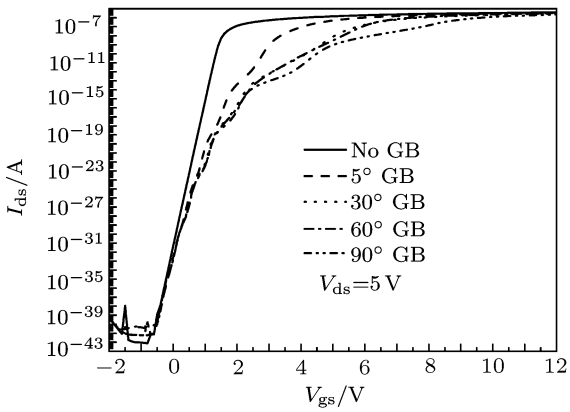


Fig.3. The transfer characteristics of ZnO TFT without grain boundary, and with the centred grain boundaries of 5°, 30°, 60°, 90°. The drain–source voltage is 5 V.

From the plots, we can see that the transistor without grain boundary exhibits a perfect saturation. When a transistor has a grain boundary in the channel, the transistor characteristics degrades, in other

words, the threshold voltage increases and the mobility decreases. With the increase of the grain boundary angle, the degradation of the transistor increases.

The transfer characteristics of ZnO TFT were then analysed by their dependence on the grain boundary location. The grain boundary angle is chosen to be 60°, and the distance of the grain boundary from the source edge, d, takes six values: 1.8, 2.2, 2.8, 3.4, 4.0, 4.6 μm, respectively. Figure 4(a) presents the transfer characteristics of the device with the above locations at $V_{ds} = 5$ V. Figure 4(b) shows an energy band diagram at the ZnO–Si_3N_4 interface. As the grain boundary is close to the drain edge, the potential barrier height decreases, and the number of carriers across the potential barrier increases, so the degradation of the transistor decreases. However, with the grain boundary close to the drain edge, the off current of the transistor is much higher. This is because the off current is controlled by the carrier generation near the drain.[20]

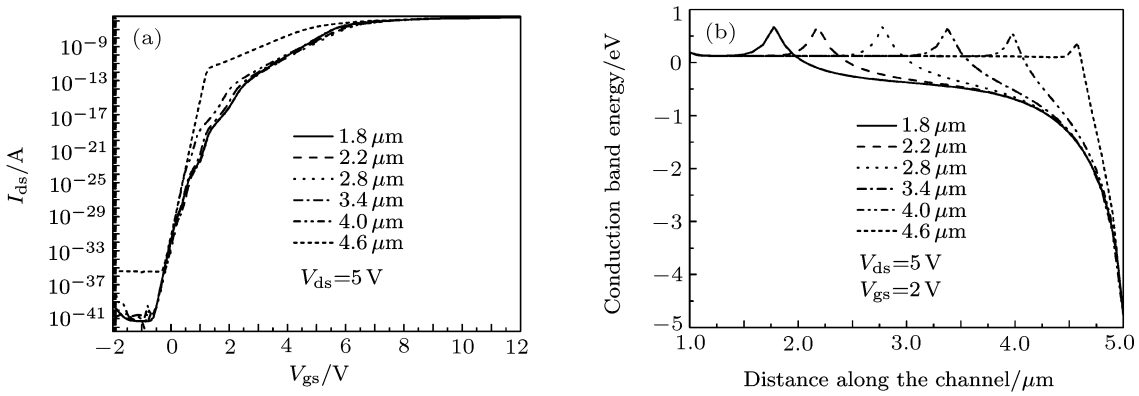


Fig.4. The effect of the 60° grain boundary located at $d = 1.8$, 2.2, 2.8, 3.4, 4.0, 4.6 μm, with the drain–source voltage 5 V and the gate voltage 2 V. (a) The transfer characteristics of ZnO TFT. (b) Conduction band diagram at the ZnO-Si_3O_4 interface along the channel.

4. Conclusions

A ZnO TFT model is developed to explore the effect of grain boundaries on the transistor characteristics. The model is characterized with different grain boundary angles and locations, which can roughly reflect the real picture in ZnO thin films. A grain boundary with a smaller angle generates a lower potential barrier, which brings less degradation of the characteristics of the transistor. A grain boundary located at the edge of the drain also brings less degradation, however, it produces higher off current. These results show how to improve the device characteristics with a proper treatment of the ZnO thin film.

References

[1] Fortunato E M C, Barguinha P M C, Pimentel A C M B G, Goncalves A M F, Marques A J S, Pereira L M N and Martins R F P 2005 *Adv. Mater.* **17** 590

[2] Carcia P F, McLean R S and Reilly M H 2006 *Appl. Phys. Lett.* **88** 123509

[3] Dhananjay and Krupanidhi S B 2007 *J. Appl. Phys.* **101** 123717

[4] Masuda S, Kitamura K, Okumura Y, Miyatake S, Tabata H and Kawai T 2003 *J. Appl. Phys.* **93** 1624

[5] Liu X C, Shi E W, Chen Z Z, Zhang H W, Zhang T and Song L X 2007 *Chin. Phys.* **16** 1770

[6] Zhou X, Wang S Q, Lian G J and Xiong G C 2006 *Chin. Phys.* **15** 199

[7] Wang F F, Cao L, Liu R B, Pan A L and Zou B S 2007 *Chin. Phys.* **16** 1790

[8] Dimitriadis C A, Kimura M, Miyasaka M, Inoue S, Farmakis F V, Brini J and Kamarinos G 2000 *Solid-State*

Electron. **44** 2045

[9] Bolognesi A, Berliocchi M, Manenti M, Carlo A D, Lugli P, Lmimouni K and Dufour C 2004 *IEEE Trans. Electron Devices* **51** 1997

[10] Farmakis F V, Brini J, Kamarinos G, Angelis C T, Dimitriadis C A, Miyasaka M and Ouisse T 2000 *Solid-State Electron.* **44** 913

[11] Edura T, Takahashi H, Nakata M, Tsutsui K, Itaka K, Koinuma H, Mizuno J and Wada Y 2006 *Current Appl. Phys.* **6** 109

[12] Yamaguchi K 2001 *J. Appl. Phys.* **89** 590

[13] Valletta A, Bonfiglietti A, Rapisarda M, Mariucci L and Fortunato G 2007 *J. Appl. Phys.* **101** 094502

[14] Hossain F M, Nishii J, Takagi S, Ohtomo A, Fukumura T, Fujioka H, Ohno H, Koinuma H and Kawasaki M 2003 *J. Appl. Phys.* **94** 7768

[15] Yoon Y, Lin J, Pearton S J and Guo J 2007 *J. Appl. Phys.* **101** 024301

[16] Kimura M, Inoue S, Shimoda T and Eguchi T 2001 *J. Appl. Phys.* **89** 596

[17] Armstrong G A, Uppal S, Brotherton S D and Ayres J R 1997 *IEEE Electron Device Lett.* **18** 315

[18] Walker P M, Mizuta H, Uno S, Furuta Y and Hasko D G 2004 *IEEE Trans. Electron Devices* **51** 212

[19] Ikeda H 2002 *J. Appl. Phys.* **91** 4637

[20] Lui O K B and Migliorato P 1997 *Solid-State Electron.* **41** 575