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Annealing effects on the structure and electrical characteristics of amorphous Er_2O_3 films*

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Amorphous Er_2O_3 films are deposited on Si (001) substrates by using reactive evaporation. This paper reports the evolution of the structure, morphology and electrical characteristics with annealing temperatures in an oxygen ambience. X-ray diffraction and high resolution transimission electron microscopy measurement show that the films remain amorphous even after annealing at 700 °C. The capacitance in the accumulation region of Er_2O_3 films annealed at 450 °C is higher than that of as-deposited films and films annealed at other temperatures. An $Er_2O_3/ErO_x/SiO_x/Si$ structure model is proposed to explain the results. The annealed films also exhibit a low leakage current density (around 1.38×10^{-4} A/cm^2 at a bias of -1 V) due to the evolution of morphology and composition of the films after they are annealed.

Keywords: Er_2O_3, gate dielectric, amorphous
PACC: 7340Q, 7360N, 7360H

1. Introduction

High k metal oxide is widely considered to replace SiO_2 as the gate dielectric material to suppress increasing gate leakage current by downscaling the size of complementary metal oxide semiconductor (CMOS) devices. Several candidate metal oxides such as HfO_2,[1,2] ZrO_2,[3,4] Al_2O_3,[5,6] and mixed oxides containing silicates[7] or aluminates,[8,9] as well as rare earth (RE) oxides (Y_2O_3,[10−13] La_2O_3,[14] and Pr_2O_3[15]) have been studied extensively. In order to get a thinner interfacial SiO_2 layer, high-k gate dielectric is generally deposited in oxygen-scarce ambience. Ultrathin (3.4–4.5 nm) Y_2O_3 and Gd_2O_3 films were deposited in an ultrahigh vacuum system, which avoids the formation of any interfacial SiO_2 layer.[10,11] However, a small effective k, $k_{\rm eff}$ of 11 and 8, respectively, before and after gas annealing at 400 °C were obtained. Very thin high-k dielectric films may contain a nonstoichiometric phase with low dielectric constant. Annealing in O_2 ambience is often necessary to adjust the stoichiometry of high k dielectric films and then to improve their electrical properties. However, interface regrowth during high temperature annealing may greatly increase the equivalent oxide thickness (EOT). Therefore, it is critical to control the annealing process for the growth of perfect high k dielectric films and at the same time to prevent the appearance of an SiO_2 interface layer.

Er_2O_3 is an attractive candidate since it has a relatively high dielectric constant, large conduction band offset with Si (about 3.5 eV),[16] and is chemically stable in contact with Si.[17] In recent years, single- or polycrystalline Er_2O_3 gate dielectric films have been successfully grown on Si substrates by different techniques.[18−24] However, the EOT increases and morphology degrades with annealing.[18−20] In this work, the evolution of structural and electrical properties of amorphous Er_2O_3 films on Si (001) by reactive evaporation with annealing at various temperatures in oxygen ambience is studied. It is found that the film annealed at 450 °C for 30 min results in a significant improvement in the morphology and electrical properties, and at the same time the interfacial layer thickness does not increase.

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2. Experimental

Clean p-type Si (001) substrates were obtained by chemical cleaning and heating to 930 °C for 30 min in ultra-high vacuum. The 5 nm thick Er_2O_3 films were grown on a wafer with a resistivity of 2–10 Ω·cm by reactive evaporation of metallic Er (3N) and oxygen gas (4N) at room temperature. The oxygen pressure, Er source temperature and the growth rate were 9×10^{-6} Torr (1 Torr = 133 Pa), 900 °C and 0.001–0.0015 nm·s^{-1}, respectively. After growth, the samples were annealed at 450 °C, 700 °C for 30 min in 1 atm O_2 ambience, respectively. The structure of Er_2O_3 films was investigated by x-ray diffraction (XRD) and cross-sectional high resolution transmission electron microscopy (HRTEM). Atomic force microscopy (AFM) was used to examine the films' morphology. Metal oxide semiconductor (MOS) structures were fabricated by evaporating an Al electrode on Er_2O_3 films. The electrical properties of capacitance–voltage (C–V) and current–voltage (I–V) characteristics were measured by an HP 4284 LCR meter and a Keithley 2400 sourcemeter, respectively.

3. Results and discussion

The AFM images given in Fig.1 show the influence of post-annealing on the morphology of Er_2O_3 films. The as-grown Er_2O_3 film was found to have a root-mean-square (rms) surface roughness of 0.49 nm. For the sample annealed at 450 °C, the roughness dramatically decreases down to 0.2 nm as shown in Fig.1(b). This value is comparable to those of the underlying silicon substrates. Such a flat surface is favorable to form a sharp interface between the Er_2O_3 film and the gate metal in MOS structures. In Fig.1(c), it is found that the surface roughness increases considerably to 0.48 nm for the films annealed at 700 °C. These results differ from the cases of polycrystalline Er_2O_3 films, where annealing causes surface roughness to develop monotonically due to grain growth,[20] which may be caused by the different film characteristics.

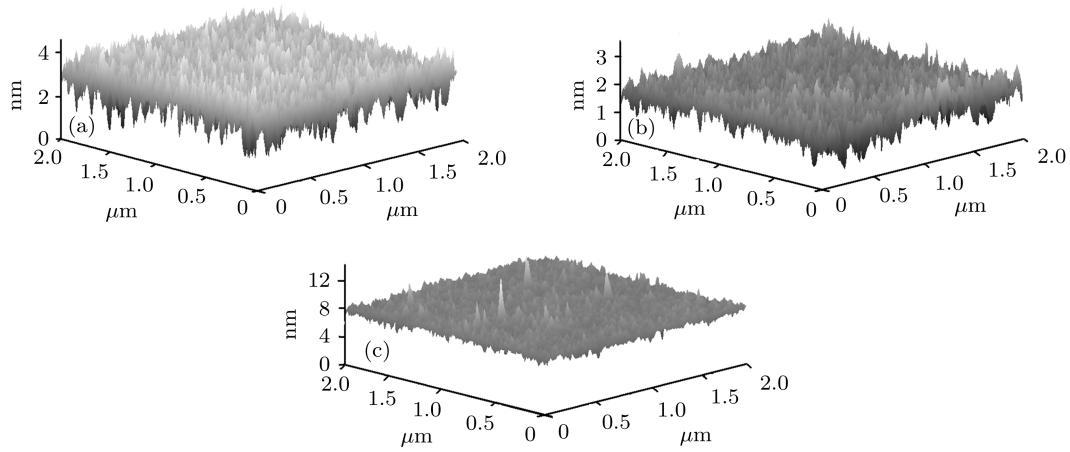


Fig.1. The AFM images of 5 nm thick Er_2O_3 films grown on Si (001) substrates: (a) as-deposited; (b) annealed at 450 °C in O_2 ambience; (c) annealed at 700 °C in O_2 ambience.

The amorphous gate dielectric has more advantages than polycrystalline and single-crystalline materials because polycrystalline dielectrics will lead to higher leakage current due to the polycrystalline grain boundaries, and the epitaxial growth of high k oxides is technically difficult and expensive. In this work, amorphous Er_2O_3 films were successfully fabricated, for XRD measurement shows no diffraction peak at $2\theta = 48.83°$, which is the location of the (440) diffraction peak of single-crystalline Er_2O_3 film,[21,22] as shown in Fig.2. After annealing in O_2 ambience, the films retained an amorphous structure, even those annealed at 700 °C, which is also confirmed by the cross-sectional HRTEM observation shown in Fig.3.

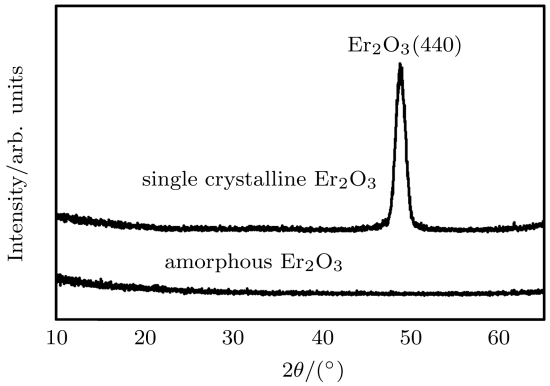


Fig.2. The XRD curves of amorphous and single-crystalline Er_2O_3 films grown on Si (001) substrates.

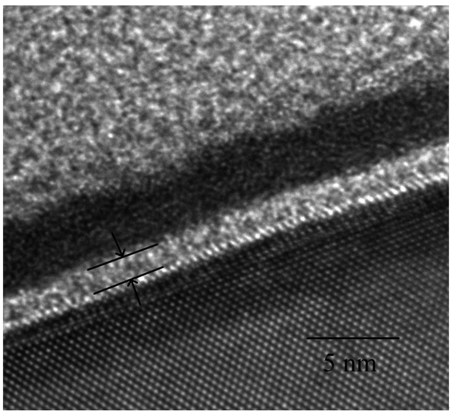


Fig.3. A cross-sectional HRTEM image of the Er_2O_3 film annealed at 700 °C for 30 min in O_2 ambience. The thickness of the interfacial SiO_2 layer is estimated to be around 1.6 nm.

HfO_2 is one of the promising high k candidates. He *et al*[25] have reported that HfO_2 films prepared by direct current reactive magnetron sputtering at room temperature were amorphous, while they crystallized in a tetragonal phase after annealing at a temperature above 500 °C in O_2 ambience. The thermal stability of amorphous Er_2O_3 is superior to that of amorphous HfO_2 films.

Cross-sectional HRTEM was performed to certify the amorphous structure of the Er_2O_3 film annealed in O_2 ambience at 700 °C and acquire the interfacial information between Er_2O_3 and Si, as shown in Fig.3. A uniform amorphous structure without obvious crystallization is presented in the Er_2O_3 film. An interfacial amorphous silicon oxide layer is presented with an average thickness of around 1.6 nm. It is noticeable that the thickness of this layer increases significantly after annealing at 700 °C in comparison with the thickness of the interfacial SiO_2 layer in the as-grown single-crystalline Er_2O_3 films.[26] We suggested that the increase of the SiO_2 layer is due to the diffusion of oxygen atoms through the Er_2O_3 film towards the Si substrate. The regrowth of the interfacial SiO_2 layer after high temperature annealing in O_2 ambience has already been reported for La_2O_3 and Gd_2O_3 films deposited on Si substrates.[27,28]

The electrical characterizations of the films were carried out on an MOS capacitor fabricated by depositing an Al metal electrode with an area of 2.8×10^{-4} cm^2 on the top of Er_2O_3 film and an Ohmic contact at the bottom of the Si substrates. Figure 4 shows the high-frequency (100 kHz) C–V curves of Er_2O_3 films for different annealing temperatures. The flat-band voltage (V_{FB}) shifts towards positive voltages, which suggests that the fixed charge density is reduced as the annealing temperature increases. The maximum capacitances in the accumulation region for the as-deposited film and the samples annealed at 450 °C and 700 °C are 396 pF, 525 pF and 436 pF, respectively, as shown in Fig.4. The capacitance increases

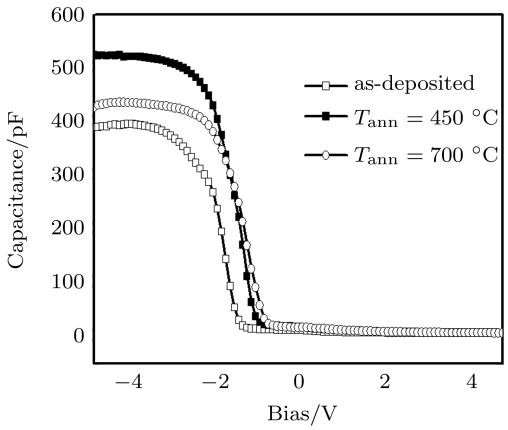


Fig.4. High-frequency C–V curves of an MOS capacitor with 5 nm thick Er_2O_3 film annealed at various temperatures.

significantly for the sample annealed at 450 °C. However, when the annealing temperature increases to 700 °C, the capacitance decreases to 436 pF. It is assumed that the as-deposited film structure is the $Er_2O_3/SiO_2/Si$. Thus the total capacitance of the sample is equivalent to the series of the capacitance of the SiO_2 interfacial layer and the Er_2O_3 layer, which can be described by $1/C = 1/C_{SiO_2} + 1/C_{Er_2O_3}$, where C_{SiO_2} and $C_{Er_2O_3}$ are the capacitances of the interfacial SiO_2 layer and the Er_2O_3 layer, respectively. The regrowth of the interfacial SiO_2 layer during annealing results in the monotonic decrease of the capacitance due to the diffusion of oxygen atoms through the Er_2O_3 film towards the Si substrate. In contrast,

the measured capacitance increases for the sample annealed at 450 °C, as shown in Fig.4. It is evident that the above two-layer model is not enough to simulate the influence of the annealing on capacitance. A three-layer model, i.e. $Er_2O_3/ErO_x/SiO_x/Si$, as shown in Fig.5, is proposed. We postulate that the as-deposited film may contain the ErO_x (ErO or any other nonstoichiometric phase), which has a lower dielectric constant than that of Er_2O_3. At the initial growth stage, oxygen atoms react with both Si atoms and Er atoms; thus it is natural to form an Er_2O_3 layer lacking oxygen (ErO_x) at the interface. However, in the subsequent growth process, only oxygen atoms and Er atoms are involved in the reaction, and a stoichiometric Er_2O_3 layer forms. The annealing process at 450 °C causes basically a transformation of ErO_x and SiO_x to Er_2O_3 and SiO_2, respectively. And there is no increase in the thickness of the interfacial SiO_2 layer as shown in Fig.5(b). Cross-sectional HRTEM of ultrathin Er_2O_3 films was performed for the samples before and after annealing for 30 min at 450 °C in O_2 ambience,[26] which is the same method as that used here. The author found that the thickness of the interfacial SiO_2 layer does not change after annealing. Thus annealing at 450 °C in O_2 ambience results in a significant improvement of the structural and electrical properties of Er_2O_3 films. The annealing process at 700 °C in O_2 ambience also turns ErO_x and SiO_x into Er_2O_3 and SiO_2; however, the thickness of interfacial SiO_2 of the sample increases significantly, which is confirmed by HRTEM measurement as shown in Fig.3. The increase of the interfacial SiO_2 layer results in a lower capacitance value in comparison with that annealed at 450 °C. For the

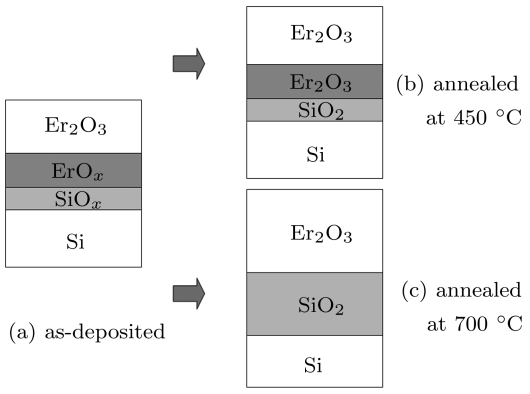


Fig.5. Diagrams summarizing the microstructure and thickness modifications induced by the annealing in O_2 ambience in comparison with that of the initial as-deposited sample.

maximum capacitance in the accumulation region, the effective dielectric constants (k_{eff}) and the EOT of the film annealed at 450 °C by taking into account of the interfacial SiO_2 layer are 10.6 and 1.8 nm, respectively. The EOT is comparable to that observed for single-crystalline Er_2O_3 films on silicon.[22]

Figure 6 shows the I–V curves of the Er_2O_3 films for different annealing temperatures. The curves were measured by sweeping the gate voltage from negative to positive with a step of 0.1 V/s. For the annealed samples, the leakage current densities are smaller by at least an order of magnitude than that of the as-deposited sample, which is due to the improvement by annealing in O_2 ambience to form stoichiometric films, and consequent lowering of the leakage current density. As expected, the leakage current density of the sample annealed at 700 °C is smaller than that annealed at 450 °C when the gate is negatively biased over 1 V. However, the leakage current density of the sample annealed at 700 °C is larger than that annealed at 450 °C at low negative bias, which may correlate with the film morphology as described in Fig.1. The nonuniform and rough surface is the main source for the so-called "weak-points"; these weak-points enhance carrier injection and further increase leakages for the film annealed at 700 °C. When the reversed bias increases to above 1 V, the leakage current density originating from the "weak-points" tends to be saturated, and the leakage current density remains at a low level. With a reversed bias voltage up to 5 V, no breakdown is observed.

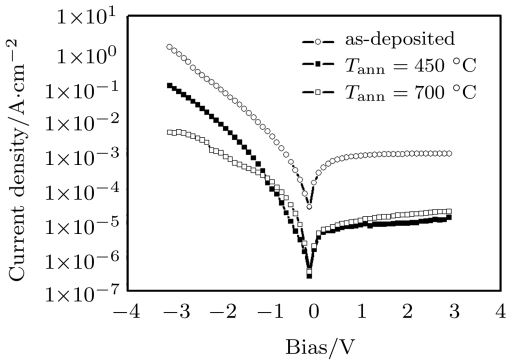


Fig.6. Leakage current density as a function of gate voltage of Er_2O_3 films as-deposited and annealed at different temperatures.

4. Conclusions

In summary, we have successfully fabricated ultrathin Er_2O_3 films on Si (001) substrates by the reac-

tion of evaporating metallic Er with oxygen gas. The XRD and the cross-sectional HRTEM measurements reveal that the films are amorphous even after thermal annealing up to 700 °C in O_2 ambience. The effects of the post-deposition annealing temperature on structure, morphology and electrical characteristics were investigated. Annealing at 450 °C is the optimal condition for the growth of Er_2O_3 high k dielectric film, and the film exhibits high capacitances and low leakage current densities. The as-deposited Er_2O_3 film contains an interfacial SiO_x layer and the ErO_x layer. The annealing process causes a transformation of ErO_x and SiO_x into Er_2O_3 and SiO_2, respectively. The k_{eff}, EOT and leakage current density of Er_2O_3 film annealed at 450 °C by taking into account the interfacial SiO_2 layer, are 10.6, 1.8 nm and 1.38×10^{-4} A/cm^2, respectively. These results indicate that the amorphous Er_2O_3 has high thermal stability and is a promising candidate to replace SiO_2 as the gate dielectric in future CMOS device.

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