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Experimental and numerical analysis of the multi-recessed gate structure for microwave silicon carbide power MESFETs*

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This paper reports that multi-recessed gate 4H-SiC MESFETs (metal semiconductor filed effect transistors) with a gate periphery of 5-mm are fabricated and characterized. The multi-recessed region under the gate terminal is applied to improve the gate–drain breakdown voltage and to alleviate the trapping induced instabilities by moving the current path away from the surface of the device. The experimental results demonstrate that microwave output power density, power gain and power-added efficiency for multi-finger 5-mm gate periphery SiC MESFETs with multi-recessed gate structure are about 29%, 1.1dB and 7% higher than those of conventional devices fabricated in this work using the same process.

Keywords: multi-recessed, microwave power, 4H-SiC MESFETs
PACC: 7340S, 7280E

1. Introduction

Silicon carbide (SiC) based metal semiconductor field effect transistors (MESFETs) are considered to be promising candidates for high power, high frequency and high temperature applications due to their excellent electrical and physical properties, i.e., wide band gap (3.26 eV), high electron saturation velocity (2×10^7 cm/s), high critical electric field (3 MV/cm), and high thermal conductivity (4.9 W/cm·K).[1−3] In recent years, SiC MESFETs have come into the market, and application areas are commercial and military communication and radars.

In the literature, a large number of SiC MESFET structures have been demonstrated for a wide range of applications. Andersson *et al* presented a SiC MESFET structure with the application of buried-gate and field-plate techniques to increase the breakdown voltage and reduce high frequency dispersion in high power applications.[4] Some researchers suggested a dual-channel structure to improve the breakdown voltage and the channel current.[5] Recently, MESFETs with buried-gate structure to reduce surface trapping effects were the most widely analysed and manufactured for power applications. However, fundamental studies on the gate-recessed structure for such devices are still limited, and the influence of gate-recessed length and number on SiC MESFETs has not been reported in detail.

In this paper, we report the fabrication of an improved structure for 4H-SiC MESFETs with multi-recessed gate which can improve electrical performance and suppress surface trapping effects. Experimental and simulation results show that the proposed structure has the best microwave output power density among all the structures. This is due to the fact that the multi-recessed region under the gate terminal modulates the electric field at the gate edge toward drain and makes the device free from drain current instability by moving the current path away from the surface of the device. In addition, SiC MESFETs with different gate-recessed numbers and length are also made and discussed.

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2. Device fabrication and physical model

2.1. Device fabrication

The MESFETs are fabricated on a SiC epi stack grown on a high-purity semi-insulating (HPSI) substrate. The substrate was purchased from Cree Inc. The epi stack consist of a 1 μm p-type buffer layer ($N_a = 3\times10^{15}$ cm^{-3}), followed by a 0.25 μm n-type channel layer ($N_d = 2.3\times10^{17}$ cm^{-3}) and a 0.2 μm highly n-type cap layer ($N_d > 2\times10^{19}$ cm^{-3}). Three different structures are fabricated and their cross sections are shown in Fig.1.

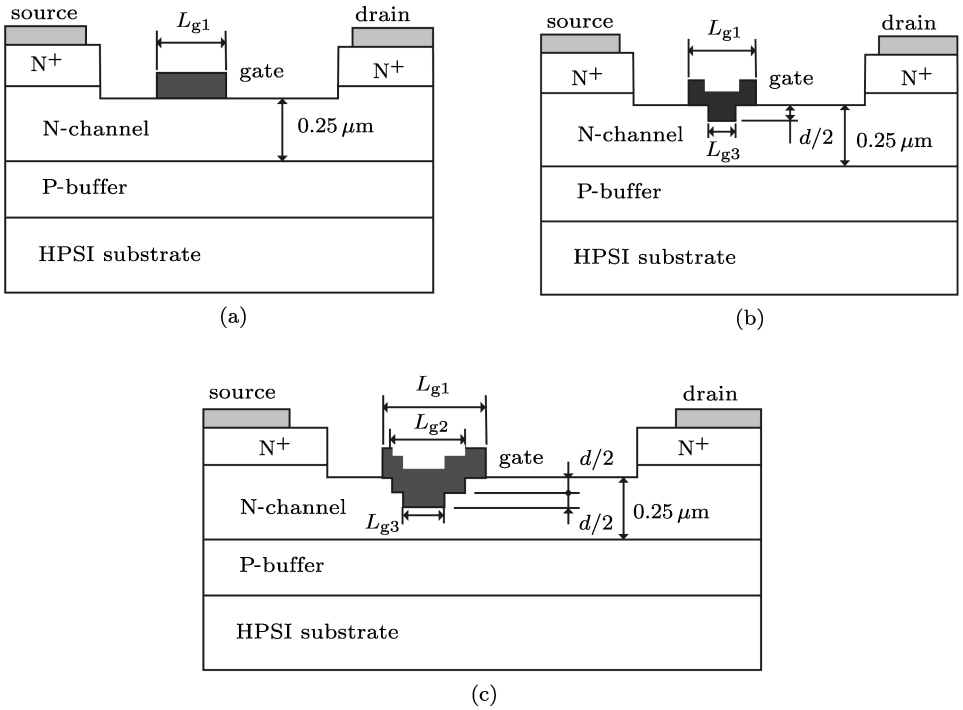


Fig.1. Schematic cross-section for different structures: (a) conventional structure; (b) single-recessed gate structure; (c) multi-recessed gate structure.

The devices were formed by mesa etching of the epi layers. ICP (inductively coupled plasma) etching was used to define the mesa and recessed region to form the gate. In order to completely remove the cap layer in the recessed etching, overetching of about 500 Å was applied. The drain current of the device was controlled by the etch depth of the gate etch, and the multi-recessed gate region (d) was etched 800 Å deep. The Γ-shaped gate length (L_{g1}) was 0.8 μm. For the multi-recessed gate structure, the recessed regions (L_{g2} and L_{g3}) were 0.6 and 0.4 μm, respectively. Ohmic contacts were also formed by etching, followed by deposition and a high-temperature annealing of Ni. Electrode patterns were formed by electron beam evapouration and liftoff. Evaluation of transmission line model fabrication on the same substrate confirmed that a specific contact resistivity of 1.0×10^{-6}–3.0×10^{-6} Ω·cm^2 was obtained. Multi-finger devices with total gate periphery up to 5-mm were made. Devices were formed on chips died from the same epi wafer to ensure that the material was the same for all devices. Figure 2(a) shows a scanning electron microscopy (SEM) image of the fabricated MESFETs. A cross-sectional SEM image of the multi-recessed gate is shown in Fig.2(b).

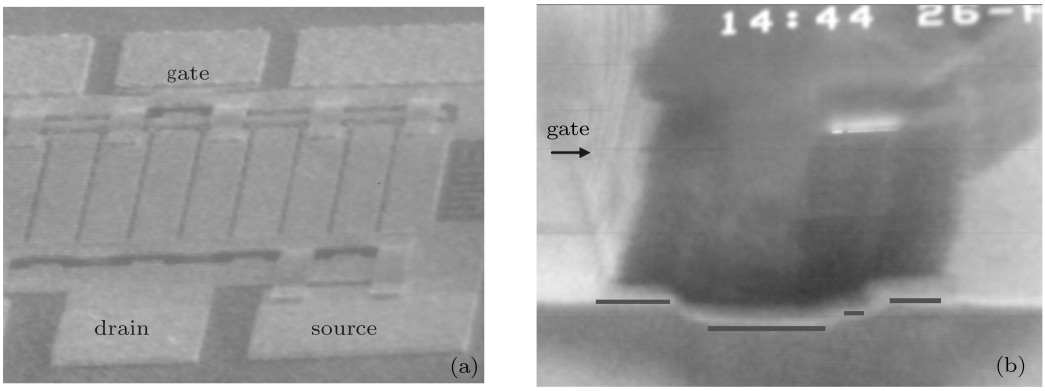


Fig.2. SEM image of (a) the fabricated MESFETs with gate width of 5 mm and (b) a multi-recessed gate structure.

2.2. Physical models

The details of the 4H-SiC material parameters used in this work are summarized in Table 1, taken from the most recent literature. The two-dimensional (2D) numerical device characteristics are realized with Atlas from Silvaco and the details of the models and simulation method are presented elsewhere.[6]

The mobility of the carriers in 4H-SiC is modeled by using the Caughey–Thomas expression, which is used to specify doping-and temperature-dependent low field mobility.[7]

$$\mu_{\mathrm{n,p}} = \mu_{0\mathrm{n,p}}^{\min}\left(\frac{T}{300\mathrm{K}}\right)^{\alpha_{\mathrm{n,p}}} + \frac{\mu_{0\mathrm{n,p}}^{\min}\left(T/300\mathrm{K}\right)^{\beta_{\mathrm{n,p}}} - \mu_{0\mathrm{n,p}}^{\min}\left(T/300\mathrm{K}\right)^{\alpha_{\mathrm{n,p}}}}{1+\left(N/N_{\mathrm{n,p}}^{\mathrm{crit}}\right)^{\gamma_{\mathrm{n,p}}}}, \quad (1)$$

where N is the total impurity concentration and $N_{\mathrm{n,p}}^{\mathrm{crit}}$ is the doping concentration at which the mobility is halfway between the minimum and maximum values, namely the mobility in highly doped and undoped material. Both $\mu_{0\mathrm{n,p}}^{\min}$ and $\mu_{0\mathrm{n,p}}^{\max}$ are the mobility values at room temperature.[8] Terms α, β and γ are fitting coefficients.

Velocity saturation at high electric fields is modeled with the Canali model.

$$\mu_{\mathrm{n,p}}(E) = \frac{\mu_{\mathrm{n_0,p_0}}}{\left(1+\left(\mu_{\mathrm{n_0,p_0}}E/\upsilon_{\mathrm{sat}}\right)^{\beta_E}\right)^{1/\beta_E}}. \quad (2)$$

Here, E is the parallel electric field, β_E is the fitting coefficient and μ_{n0} and μ_{p0} are the low field electron and hole mobilities, respectively.

The simulator Atlas accounts for impurity freeze-out with appropriate degeneracy factors G_{CB} and G_{VB} for conduction and valence bands. The ionized donor and acceptor impurity concentrations are then given by[9]

$$N_{\mathrm{D}}^{+} = \frac{N_{\mathrm{D}}}{1+G_{\mathrm{CB}}\exp\left(\dfrac{E_{\mathrm{Fn}}-(E_{\mathrm{C}}+E_{\mathrm{DB}})}{kT}\right)}, \quad (3)$$

$$N_{\mathrm{A}}^{-} = \frac{N_{\mathrm{A}}}{1+G_{\mathrm{VB}}\exp\left(\dfrac{(E_{\mathrm{V}}+E_{\mathrm{AB}})-E_{\mathrm{Fn}}}{kT}\right)}, \quad (4)$$

where E_{DB} is the donor energy level, E_{AB} is the acceptor energy level, E_{Fn} and E_{Fp} are the quasi-Fermi energy levels for electrons and holes, E_{C} and E_{V} are conduction and valence band edge energies and N_{D} and N_{A} are net compensated n-type and p-type doping, respectively.

The effect of the recombination centers can be described by the conventional Shockley–Read–Hall (SRH) recombination/generation expression.

$$R_{\mathrm{SRH}} = \frac{np-n_{\mathrm{i}}^2}{\tau_{\mathrm{p}}\left(n+n_{\mathrm{i}}\exp\left(E_{\mathrm{trap}}-E_{\mathrm{C}}\right)\right)+\tau_{\mathrm{n}}\left(p+n_{\mathrm{i}}\exp\left(E_{\mathrm{V}}-E_{\mathrm{trap}}\right)\right)}, \quad (5)$$

where

$$\tau_{\mathrm{n,p}} = \frac{\tau_{\mathrm{n0,p0}}}{1 + (N/N_{\mathrm{n,p}})}. \quad (6)$$

Here, τ_{n} and τ_{p} are electron and hole lifetimes, n_{i} is the effective intrinsic carrier concentration, n and p are electron and hole densities, E_{trap} is the difference between the trap energy level and the intrinsic Fermi level and $N_{\mathrm{n,p}}$ is a characteristic parameter for electrons and holes, respectively. For the sake of simplicity difference $E_{\mathrm{trap}} = 0$ is assumed during this analysis.

Auger recombination is also considered and calculated when we introduce the coefficients C_{n} and C_{p} given in Ref.[10] by means of

$$R_{\mathrm{AU}} = \left(C_{\mathrm{n}} n + C_{\mathrm{p}} p\right)\left(np - n_{\mathrm{i}}^2\right). \quad (7)$$

The temperature dependence of the band gap is modeled as

$$E_{\mathrm{g}}(T) = E_{\mathrm{g}}^{300} - 3.3 \times 10^{-4}\,(T - 300), \quad (8)$$

where E_{g}^{300} is the band gap energy at room temperature.

Table 1. Simulation model parameters assumed at room tempaerature.[11–13]

material parameter	unit	value
dielectric constant		9.66
intrinsic concentration	/cm^{-3}	8×10^{-9}
E_{g} (300K)	/eV	3.26
$\tau_{\mathrm{n,p}}$	/s	1×10^{-7}, 2×10^{-8}
$N_{\mathrm{n,p}}$	/cm^{-3}	7×10^{16}
$C_{\mathrm{n,p}}$	/(cm^6/s)	5×10^{-31}, 2×10^{-31}
E_{AB}	/meV	191
E_{DB}	/meV	65
G_{CB}		2
G_{VB}		4
$\mu_{0\mathrm{n,p}}^{\mathrm{min}}$	/(cm^2/(V·s))	40, 15.9
$\mu_{0\mathrm{n,p}}^{\mathrm{max}}$	/(cm^2/(V·s))	900, 124
$N_{\mathrm{n,p}}^{\mathrm{crit}}$	/cm^{-3}	1.94×10^{17}, 1.76×10^{19}
$\alpha_{\mathrm{n,p}}$		–0.5
$\beta_{\mathrm{n,p}}$		–2
$\gamma_{\mathrm{n,p}}$		0.61, 0.34
v_{sat}	/(cm/s)	2×10^7
β_E		1.2

3. Results and discussion

3.1. Direct current (DC) and radio frequency (RF) characteristics

The measured drain current–voltage ($I_{\mathrm{ds}} - V_{\mathrm{ds}}$) characteristics for the 5-mm gate periphery device are shown in Fig.3. The source contact is grounded and the gate bias (V_{gs}) is varied from 0 to –16 V in steps of –4 V. The saturated drain–source current is higher than 250 mA/mm with a pinch voltage V_{p} of –12 V. The transconductance is 24 mS/mm at a drain voltage of 20 V and a gate voltage of 0 V. Figure 4 plots the gate leakage current as a function of the gate–drain voltage under reverse bias conditions for 5-mm gate periphery multi-recessed gate SiC MESFETs, with floating source electrode. It is found that the gate–drain breakdown voltage is more than 100 V.

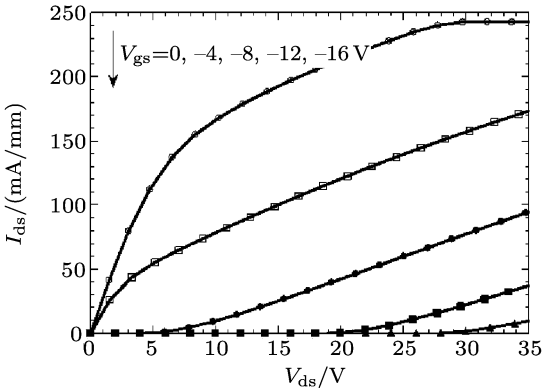


Fig.3. I_{ds} versus V_{ds} for SiC MESFETs with multi-recessed gate structure.

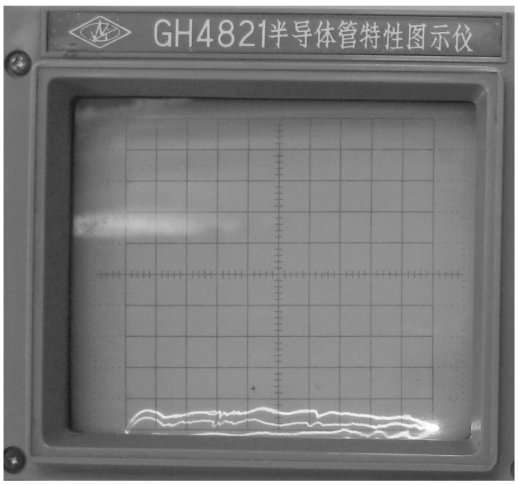


Fig.4. Gate leakage current versus gate-drain voltage with floating source electrode for the proposed 4H-SiC MESFETs (x-axis: $V_{\rm ds}$ = 10 V/div; y-axis: $I_{\rm ds}$ = 10μA/div; $V_{\rm gd} > 100$ V).

The S-parameter of the devices is measured using the Agilent E8363B PNA system. Because of our measurement system limitation, S parameter measurements were performed from 0.5 to 15 GHz with maximum voltage $V_{\rm ds}$ = 25 V, although the devices had much higher DC operation voltage. For large, multiple finger gate periphery SiC MESFETs (5-mm) with multi-recessed gate structure, the cut-off frequency $f_{\rm T}$ (defined as the frequency at which the current gain is equal to 1) and the maximum oscillation frequency $f_{\rm max}$ (defined as the frequency at which the unilateral power gain is unity) are 6 and 12 GHz, respectively. In addition to insufficient frequency sweeping at a low drain bias, the self-heating effects of large gate periphery devices result in relatively poor frequency performances due to the deterioration of current–voltage characteristics.

3.2. Gate-recessed region influence

Figure 5 shows a comparison of the gate–drain breakdown characteristics of all the structures. As can be seen from the figure, the breakdown voltage is just 50 V for the conventional MESFETs but is improved from 50 to 100 V by applying the multi-recessed gate structure. It should be noted that the multi-recessed gate SiC MESFETs have the highest breakdown voltage in comparison with normal structures and single recessed gate devices. This improvement in breakdown voltage is due to the fact that the high electric field peak at the bottom edge of the gate toward the drain side is suppressed by extension of the gate metal on the surface, which acts like a field plate resulting in a gradual field distribution.

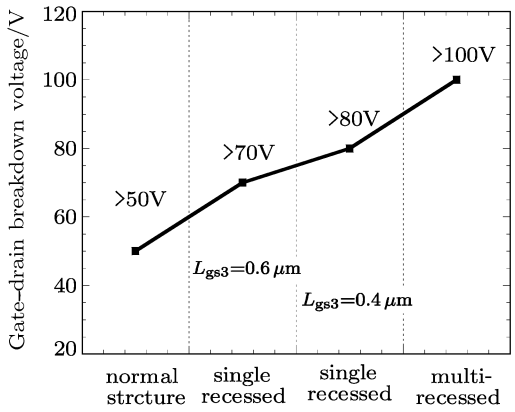


Fig.5. Comparison of gate–drain breakdown voltages for different structures.

RF power testing is performed on individually packaged 5-mm gate periphery SiC MESFETs at 2 GHz by using pulsed waveforms. The results biased for peak power are shown in Fig.6, and represent three different SiC MESFET devices with the same gate periphery. It is found that the output power, gain and efficiency for the proposed devices are higher than the conventional and single-recessed devices. For 5-mm MESFETs with multi-recessed gate structure, the maximum output power is 13.5 W (2.7 W/mm) at $V_{\rm gs}$ = −6 V and $V_{\rm ds}$ = 45 V with power-added efficiency (PAE) of 50% and power gain of 11.3 dB, whereas the normal structures provided an output power of 10.5 W (2.1 W/mm), 43% PAE, and 10.2 dB power gain at the same bias conditions. This is considered to be caused by the multi-recessed region under the gate terminal of the proposed device, which results in the elimination of electric field strength at the gate edge toward the drain and the reduction of surface trapping effects. As can be seen from Fig.7, the

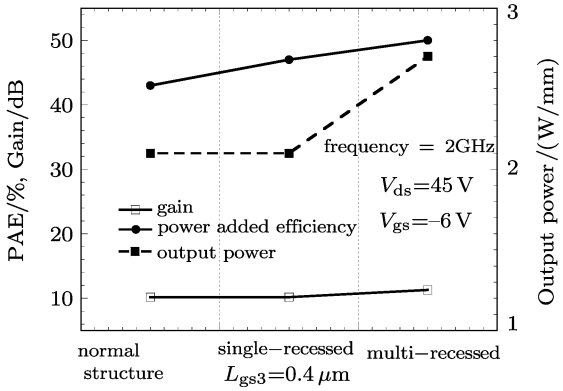


Fig.6. Comparison of power performances for different structures.

current path in the on-state is moved away from the surface in multi-recessed gate structures and, consequently, less electron tunneling and trapping is expected near this region for the proposed structure in comparison with normal devices. This also makes the control of the passivation layer less critical for devices of this kind. Some researchers have shown similar results.[14,15]

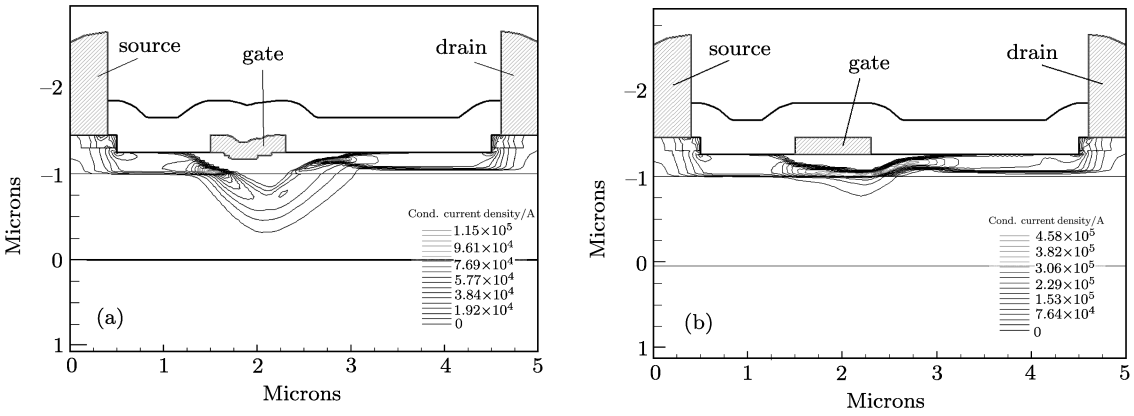


Fig.7. Electron current density profiles along the channel for different devices at $V_{ds} = 40$ V and $V_{gs} = 0$ V: (a) multi-recessed gate structure; (b) conventional structure.

4. Conclusion

In this work, SiC MESFETs with multi-recessed gate structure are fabricated for the first time. The experimental results are compared with those of conventional and single-recessed gate devices fabricated by using exactly the same process flow. As compared to normal structures, the maximum output power, power gain and PAE in the proposed structures increase by 29%, 1.1dB and 7%, respectively. These improvements are explained by the increase in breakdown voltage and the decreased surface trapping effects. Therefore, 4H-SiC MESFETs with multi-recessed gate have superior DC and RF performance compared to similar devices based on the conventional structure.

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