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The research on suspended ZnO nanowire field-effect transistor

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This paper reports that a novel type of suspended ZnO nanowire field-effect transistors (FETs) were successfully fabricated using a photolithography process, and their electrical properties were characterized by I–V measurements. Single-crystalline ZnO nanowires were synthesized by a hydrothermal method, they were used as a suspended ZnO nanowire channel of back-gate field-effect transistors (FET). The fabricated suspended nanowire FETs showed a p-channel depletion mode, exhibited high on–off current ratio of $\sim 10^5$. When $V_{\rm DS} = 2.5\,{\rm V}$, the peak transconductances of the suspended FETs were $0.396\,\mu{\rm S}$, the oxide capacitance was found to be 1.547 fF, the pinch-off voltage $V_{\rm TH}$ was about 0.6 V, the electron mobility was on average $50.17\,{\rm cm}^2/{\rm Vs}$. The resistivity of the ZnO nanowire channel was estimated to be $0.96 \times 10^2\ \Omega\,{\rm cm}$ at $V_{\rm GS} = 0\,{\rm V}$. These characteristics revealed that the suspended nanowire FET fabricated by the photolithography process had excellent performance. Better contacts between the ZnO nanowire and metal electrodes could be improved through annealing and metal deposition using a focused ion beam.

Keywords: ZnO nanowire, back-gate, suspended, field-effect transistor
PACC: 7280E, 7360L

1. Introduction

In recent years, quasi-one-dimensional (Q1D) semiconducting nanostructures have received tremendous research interest for their potential applications in nanoscale electronic and optoelectronic devices such as transistors, light-emitting diodes, photodetectors, and chemical sensors. The Q1D nanostructures include such things as nanowires (NWs), nanotubes, nanobelts, and nanoneedles. The small dimensions of these structures promise increases in device packing density, decreases in power consumption, and also increases in sensitivity in chemical sensing applications. As a II–VI compound semiconductor with a wide and direct band gap of 3.37 eV, zinc oxide (ZnO) has been shown to be a prime candidate for the electronic and optoelectronic applications described above. In particular, the synthesis,[1] properties,[2] gas sensing characteristics,[3] and electrical characteristics in field-effect transistor (FET) configuration[4] of ZnO nanowires have been reported previously. Gas sensing with nanowires is normally achieved by monitoring the conductance change of the nanowire when exposed to a particular gas. The Q1D structures have very small radii giving them a larger surface-to-volume ratio which is highly susceptible to alter electronic properties by means of chemisorptions.

However, the research of our country in this field is still in its infancy, and mostly focuses on synthesis of nanowire, with fewer reports on nanowire FET devices,[5] so the advantage of nanometre devices has been seriously restricted.

In this report the properties of ZnO nanowires in a suspended FET configuration are studied. Single-crystalline ZnO nanowires were synthesized by a hydrothermal method. They were used as a suspended ZnO nanowire channel of back-gate FET. The fabricated suspended nanowire FETs exhibited excellent performance, high $I_{\rm on}/I_{\rm off}$ of $\sim 10^5$. When $V_{\rm DS} = 2.5\,{\rm V}$, the peak transconductances of the suspended FETs were $0.396\,\mu{\rm S}$, the oxide capacitance was found to be 1.547 fF, the pinch-off voltage $V_{\rm TH}$ was about 0.6 V, the electron mobility was on average $50.17\,{\rm cm}^2/{\rm Vs}$. Continued work is underway to reveal the intrinsic properties of suspended ZnO nanowires and to explore their device applications.

2. Device fabrication

The ZnO nanowire was synthesized on semi-insulting SiO_2 substrates by hydrothermal technology, which was provided from University of Sciences and Technology of China. The nanowire SEM picture is shown in Fig.1.

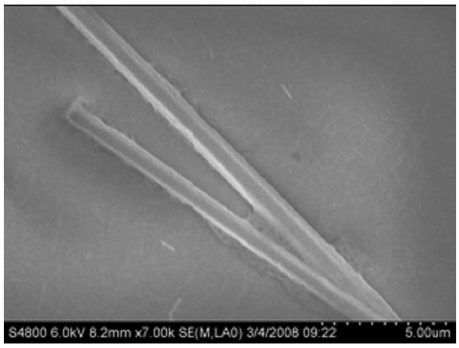


Fig.1. SEM image of the ZnO nanowires.

As shown in Fig.2, device fabrication started with a 4″ oxidized p-type Si wafer. The gate oxide thickness is 400 nm. The wafer is then etched in HF until the back oxide is etched away using the e-beam metal evaporator, 20/400 nm thick Ti/Au is deposited on the back of the wafer to form back-gate metal. The substrate containing the nanowire bundles is then sonicated in isopropyl alcohol (IPA) to release the individual nanowires. The IPA solution is dropped onto a previously prepared array of metal contacts on a p-type Si substrate with back gate. The chip is prepared by the usual lithographic techniques to form a Source–Drain, a bi-layer of titanium (30 nm) and gold (500 nm) is evaporated onto the Si in an array pattern of S-D electrodes. The distance between Source–Drain of 7 μm provides contacts for a nanowire FET. Much of the oxide layer on the Si substrate is then etched away creating a trench between adjacent electrodes with a depth of about 500 nm. Once the nanowires are deposited on the chip, it is viewed under a high-powered optical microscope so that FET devices can be found. The inset of Fig.3 shows an image of such a ZnO NW FET, note the good contact between nanowire channel and S-D electrodes.

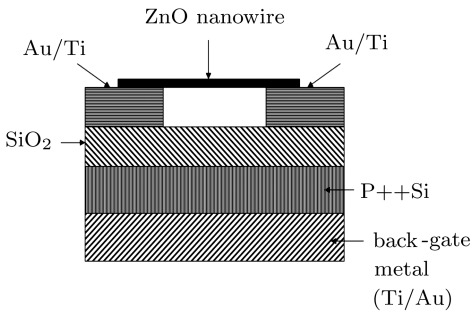


Fig.2. The schematic diagram of the suspended ZnO nanowire FET.

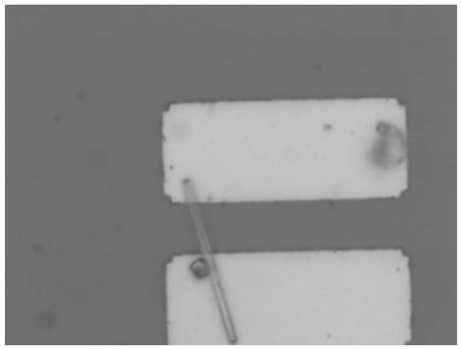


Fig.3. Image of ZnO nanowire FET.

3. Results and discussion

The DC characterization was performed using a probe station and on wafer radio frequency (RF) probes from Agilent 4155B. Typical transfer characteristics and output characteristics of a suspended ZnO device are shown in Figs.4 and 5, respectively.

The I–V characteristic was measured by sweeping the voltage from −5 to 5 V. The channel length between the source and drain electrodes is 7 μm, and the thickness of the SiO_2 gate oxide layer is 400 nm. In the I_{DS}–V_{GS} curve plotted in the inset of Fig.4, the drain current decreases with the increase of gate voltage, which shows a p-channel depletion mode device,

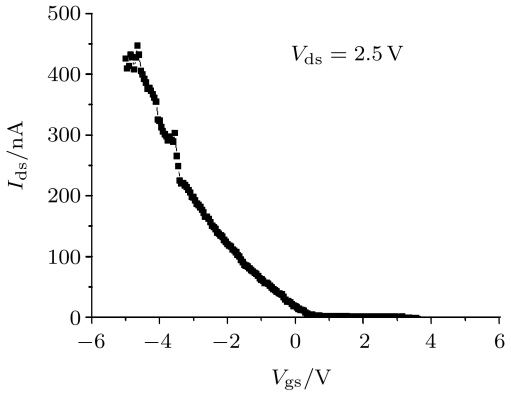


Fig.4. Transfer characteristics of ZnO nanowire FET.

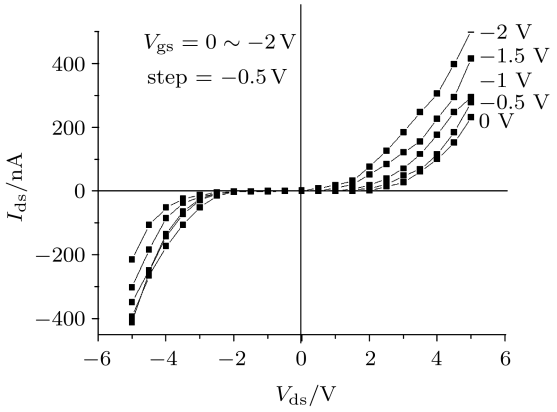


Fig.5. DC characteristic of ZnO nanowire FET.

and exhibits high on–off current ratio (I_{on}/I_{off}) of $\sim 10^5$ at $V_{DS} = 2.5$ V.

In the I_{DS}–V_{DS} curve plotted in the inset of Fig.5, the drain current of the suspended channel FET increases as the increase of drain voltage. The slopes of the I_{DS}–V_{DS} curves are dependent on the gate voltage. The largest drain-to-source current (I_{ds}) of the fabricated suspended nanowire FETs is about 506 nA. The low current owing to the high parasitic contact resistance of ZnO nanowires has been seen in other studies.[6]

The channel of the suspended ZnO nanowire FET is not fully depleted in the I_{DS}–V_{DS} curve (inset) of Fig.5. This is attributed to the high concentration of charge carriers within the ZnO nanowire channel.

The pinch-off voltage V_{TH} is about 0.6 V. The device exhibits good I–V characteristics, the extrinsic transconductance (g_m) of the device at 2.5 V drain-source voltage is 0.396 μS.

The oxide capacitance of the back-gate FET was found to be 1.547 fF from the equation,

$$C = 2\pi\varepsilon\varepsilon_0 L / \ln(2h/r_{nw})^{[7]},$$

where ε is the dielectric constant of SiO_2 (3.9), L the channel length of the nanowire FET (7 μm), h the thickness of SiO_2 (400 nm), and r_{nw} the radius of the nanowire (300 nm). The field effect mobility was estimated on the basis of the formula,

$$\mu_e = g_m L \ln(2h/r_{nw})/2\pi\varepsilon\varepsilon_0 V_{DS}{}^{[3]}.$$

The mobility of the back-gate suspended nanowire FETs is about 50.17 cm^2/Vs at $V_{DS} = 2.5$ V.

In comparison with mobility of top -gate FETs[8], the back-gate suspended ZnO nanowire FETs with gate dielectrics of native SiO_2 layer fabricated in this study operated in good performance.

The resistivity of the ZnO nanowire channel in the I_{DS}–V_{DS} curve of Fig.5 is estimated to be 0.96×10^2 Ω cm at $V_{GS} = 0$ V from the formula,

$$\rho = V_{ds} \cdot \pi r_{nw}^2 / I_{ds} L.$$

This low resistivity indicates that a number of electron carriers, due to defects such as oxygen vacancies, are present within the ZnO nanowire channel.

As gold has a work function of 5.31 eV and the ZnO nanowire has a work function of 3.37 eV, there is a mismatch in work function at the interface and a contact Schottky barrier is usually observed. Moreover, the ZnO nanowire was simply laid on the gold electrodes and was held by weak van der Waals forces. So, the Ohmic contact was bad, in order to improve the contact between the ZnO nanowire and the Au electrode, maybe annealing and focused ion beam (FIB) are the effective ways to get better characteristics.

4. Conclusion

Single crystal ZnO NWs were synthesized by a hydrothermal method. The NWs were used as a back-gate FET with a suspended ZnO nanowire channel. The fabricated suspended nanowire FET shows a p-channel depletion mode, and exhibits high on–off current ratio of $\sim 10^5$. When $I_{DS} = 2.5$ V, the peak transconductances of the suspended FETs were 0.396 μS, the oxide capacitance was found to be 1.547 fF, the pinch-off voltage V_{TH} is about 0.6 V, the electron mobility is on average 50.17 cm^2/Vs, the resistivity of the ZnO nanowire channel was estimated to be 0.96×10^2 Ω cm at $V_{GS} = 0$ V. These characteristics reveal that the suspended nanowire FET fabricated by the photolithography process has excellent performance. Further investigation into the mechanical properties of the suspended NW may shed some light on the results. Additionally, better contacts between the ZnO nanowire and metal electrodes could be improved through annealing and metal deposition using an FIB.

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