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An oxide filled extended trench gate super junction MOSFET structure*

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This paper proposes an oxide filled extended trench gate super junction (SJ) MOSFET structure to meet the need of higher frequency power switches application. Compared with the conventional trench gate SJ MOSFET, new structure has the smaller input and output capacitances, and the remarkable improvements in the breakdown voltage, on-resistance and switching speed. Furthermore, the SJ in the new structure can be realized by the existing trench etching and shallow angle implantation, which offers more freedom to SJ MOSFET device design and fabrication.

Keywords: power MOSFET, super junction, trench gate, shallow angle implantation
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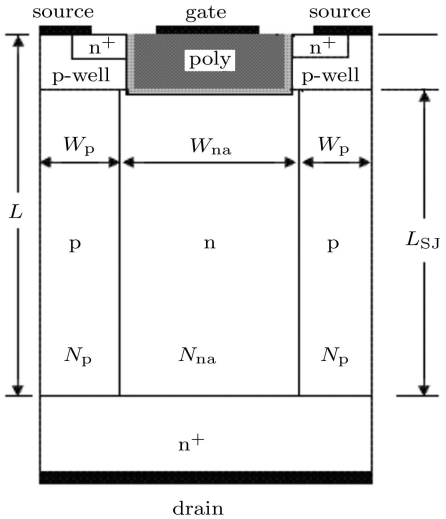
1. Introduction

In order to further reduce the conduction loss and switching loss of power MOSFETs in high frequency power switches application, a super junction (SJ) is introduced in power MOSFET structure.[1] And to obtain high frequency, an extended trench gate SJ MOSFET with polysilicon filled trench[2] and a planar gate SJ MOSFET with oxide filled trench[3] have been proposed in recent years. But these structures have hardly the better trade-off relations between the blocking, conducting and switching characteristics simultaneously. In this paper, a new trench gate SJ MOSFET is proposed, in which the extended trench is filled with oxide and the n-pillar region of SJ structure is formed by shallow angle implantation. The characteristics are simulated by ISE simulator and compared with conventional trench gate SJ MOSFET. And the results show that the new structure has optimal characteristics.

2. Device structure and features

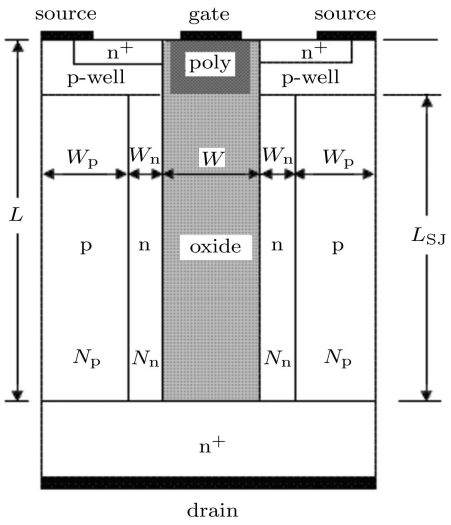
Figure 1(a) is the conventional trench gate SJ MOSFET structure (structure A), in which the drift region consists of the conventional SJ structure. Figure 1(b) is a new trench gate SJ MOSFET(structure B), in which an extended trench located below the polysilicon gate is filled with an oxide, and the n-pillar regions of SJ located in the trench sidewalls are formed by shallow angle implantation.

In SJ MOSFET structure, to obtain high breakdown voltage ($V_{\rm BR}$), it is necessary to control accurately the charge balance between n-pillar and p-pillar regions.[4,5] So the products of the width and concentration of n-pillar region of two structures must equal to the product of the width and concentration of p-pillar region. i.e. $W_{\rm n} \cdot N_{\rm n} \approx W_{\rm na} \cdot N_{\rm na} \approx W_{\rm p} \cdot N_{\rm p}$. Comparatively, the width of n-pillar region of structure B



(a) Structure-A: conventional structures

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(b) Structure-B: new structures

Fig.1. Comparison of the conventional trench SJ MOSFET and new trench SJ MOSFET structures.

is narrower than that of structure A, i.e. $W_n < W_{na}$, the concentration of n-pillar region of structure B is higher than that of structure A, i.e. $N_n > N_{na}$. This fulfils the charge balance condition of SJ.

3. Mechanism and characteristics analysis

3.1. Breakdown voltage (V_{BR})

The oxide filled extended trench region has a strong impact on the device behaviour. During blocking, the source and gate region potentials are same. With the increase of drain voltage, for structure A, the surface of n-pillar region under polysilicon gate brings some additional positive charge, which can cause charge imbalance, and result in the fall of V_{BR}. But for structure B, there is no such phenomenon during blocking because of the filled oxide. This shows that structure B achieves easily the charge balance, and its V_{BR} is higher than that of structure A.

3.2. On-resistance (R_{on})

Because there is not JFET region in trench gate MOSFET structure, R_{on} mainly consists of the accumulation layer resistance, R_A, the drift region resistance, R_D, and the channel region resistance, R_{CH}. At same gate voltage and channel region parameters, R_{CH} is same for two structures. R_D is inversely proportional to the products of the concentration and width of n-pillar region respectively, i.e. $R_D \propto (W_{na} \cdot N_{na})^{-1}$ for structure A, $R_D \propto (W_n \cdot N_n)^{-1}$ for structures-B. Because the products of $(W_n \cdot N_n)$ and $(W_{na} \cdot N_{na})$ are a constant, R_D is also same for two structures. But R_A is different for two structures. Because the width of polysilicon gate region covered on the n-pillar region in structure A is wider, it causes a higher R_A. But for structure B, the polysilicon gate covers hardly on the n-pillar region, R_A is zero, so the R_{on} of structure B only consists of the R_D and R_{CH}. i.e. $R_{on} = R_D + R_{CH} + R_A$ for structure A, $R_{on} = R_D + R_{CH}$ for structure B. This shows that R_{on} or conducting loss of structure B is smaller than that of structure A.

3.3. Input capacitance (C_{IN})

Switching characteristic of power MOSFET is related to charge and discharge of its input capacitance, C_{IN}, and the smaller C_{IN} is helpful to improving the switching characteristic.

C_{IN} of two structures can be expressed as:

$$C_{IN} = C_{GS} + C_{mi} = C_{GS} + (1 + g_m Z)C_{GD}, \quad (1)$$

where C_{GS} is the gate-source capacitance, C_{GD} is the gate-drain capacitance, C_{mi} is the Miller capacitance, which is caused by the Miller effect and increases with the increase of C_{GD}, g_m is transconductance and Z is load resistance.

C_{GS} and C_{GD} are proportional to the ratio of the permittivity, ε_{ox}, and thickness of the gate oxide layer, t_{ox}, respectively. Comparatively, C_{GS} is same for two structures, but C_{GD} is different, i.e. $C_{GD} = \varepsilon_{ox}/t_{ox}$ for structure A, $C_{GD} = \varepsilon_{ox}/(t_{ox} + L_{SJ})$ for structure B. So C_{GD} of structure B is far smaller than that of structure A. This shows that C_{IN} of structure B is far smaller than that of structure A.

3.4. Output capacitance (C_{OUT})

The switching loss of power MOSFET during turn-off is determined by the output capacitance, C_{OUT}, and the smaller C_{OUT} is helpful to reducing switching loss.

C_{OUT} of two structures can be expressed as

$$C_{OUT} = C_{DS} + C_{GD}, \quad (2)$$

where C_{DS} is the drain-source capacitance, which is caused by the depletion capacitance in n-pillar and

p-pillar regions of SJ, and the magnitude of C_{DS} is determined by the permittivity of silicon ε_{si}, and the doping concentration of pillar regions which controls the depletion width, w_d, i.e. $C_{DS} = \varepsilon_{si}/w_d \propto N_{na}$ for structure A, $C_{DS} = \varepsilon_{si}/w_d \propto N_n$ for structures-B. Because of $N_n > N_{na}$, so C_{DS} of structure B is little larger than that of structure A. But C_{GD} of structure B is far smaller than that of structure A. Synthetically, C_{OUT} of structure B is smaller than that of structure A.

4. Simulation and validation

In order to validate the performance of new trench gate SJ MOSFET, the conventional and new trench gate SJ MOSFETs with same chip area are set up, in which the thickness of gate oxide layer (t_{ox}) is 0.1 μm, and the thickness of polysilicon gate is 1.5 μm, the concentrations of n^+ source and p-well regions are $1 \times 10^{20}\,cm^{-3}$ and $5 \times 10^{17}\,cm^{-3}$ respectively, the concentration (N_p), width (W_p) and length (L_{SJ}) of p-pillar region are $5.9 \times 10^{15}\,cm^{-3}$, 3 μm and 8 μm respectively. Additionally, the concentration (N_{na}) and width (W_{na}) of n-pillar region of structure A are $5.9 \times 10^{15}\,cm^{-3}$ and 6 μm respectively, the width of oxide filled trench of structure B, W, equals to ($W_{na} - 2W_n$). Based on the structures model, the blocking, conducting and switching characteristics are simulated and compared.

4.1. Blocking

In order to analyse the influence of the W_n and N_n of n-pillar region on the V_{BR} of structure B, the blocking characteristics are simulated. The results show, when N_n and W_n can choose three groups of structural parameters, i.e. $1.7 \times 10^{16}\,cm^{-3}$and 1.0 μm, $2.2 \times 10^{16}\,cm^{-3}$ and 0.8 μm, and $3.4 \times 10^{16}\,cm^{-3}$ and 0.5 μm, respectively, V_{BR} has a maximum.

Figure 2 indicates a comparison of blocking characteristics between structure A and structure B with above three groups' structural parameters. Figure 2 shows that V_{BR} of structure A is about 140V, V_{BR} of structure B is about 163 V, which is obviously higher than that of structure A. This is because the charges balance condition of SJ in structure A is broken with the increase of V_{DS}, it results in the fall of V_{BR}. This shows that the breakdown voltage of structure B is higher than that of structure A, and the W_n has hardly influence on V_{BR}.

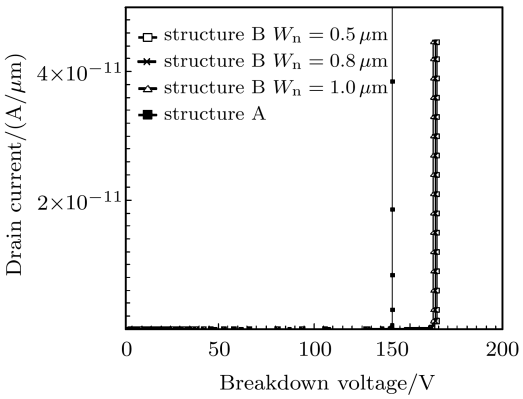


Fig.2. Comparison of blocking characteristics of structure A and structure B.

4.2. Conducting

Figure 3 indicates a comparison of the $I-V$ characteristics during conducting of structure A and structure B with above three groups' structural parameters. From Fig.3 we can see that for certain drain current density, such as, J_D is 2×10^{-5}A/ μm (or 166A/ cm^2), the on-state voltage drop of structure A is 1.2 V, the on-state voltage drop of structure B is 1.05 V, which is obviously lower than that of structure A. This shows that the on-state voltage drop of structure B is lower than that of structure A, in particular, at high current density.

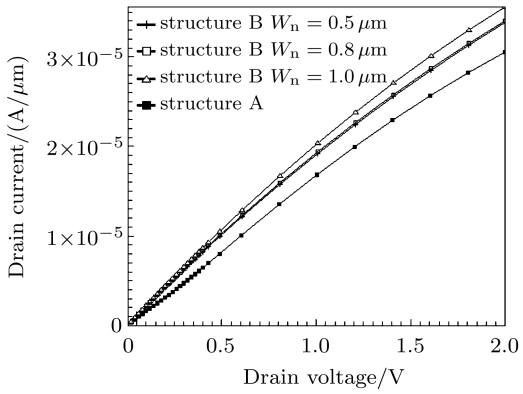


Fig.3. Comparison of conducting characteristics of structure A and structure B.

4.3. Switching

Figure 4 indicates a comparison of the variation curves of the output capacitance with drain voltage of structure A and structure B with W_n of 0.5 μm. From

Fig.4 we can see that when the drain voltage V_{DS} is 13 V, C_{OUT} of structure A is about 1.1×10^{15}F/ μm (or 9.2×10^{21}F/ cm^2), C_{OUT} of structure B is about 3.5×10^{14}F/μm (or 2.9×10^{21}F/ cm^2). It was apparent that C_{OUT} of structure B is smaller than that of structure A.

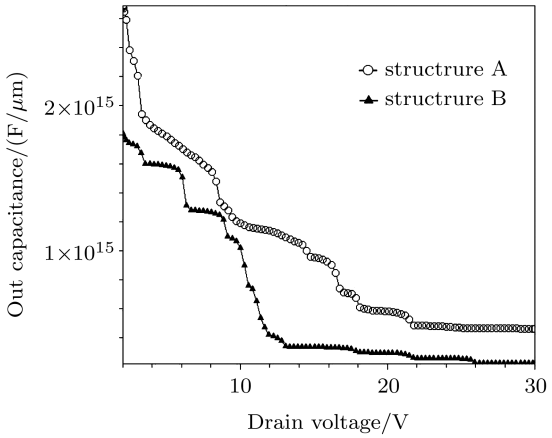
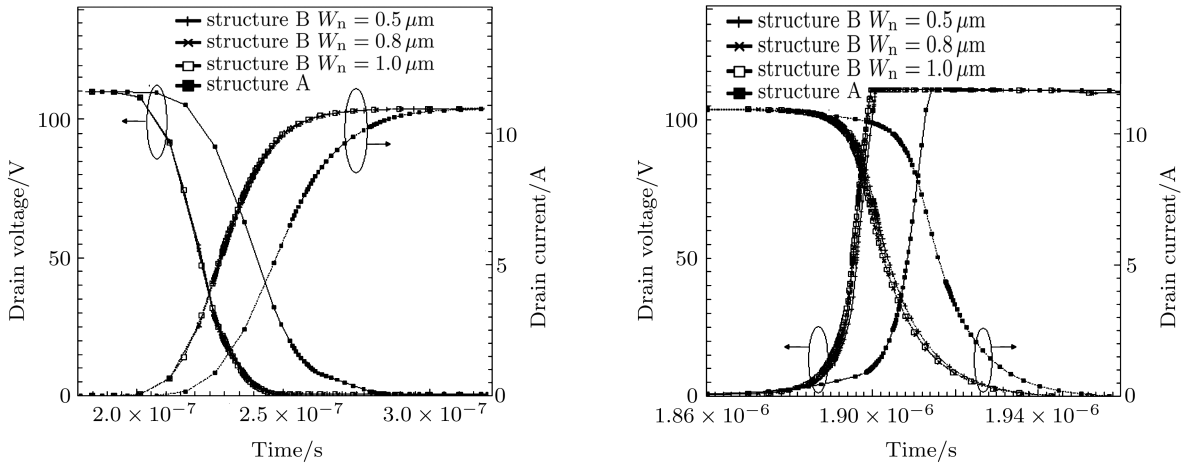


Fig.4. Comparison of output capacitance of structure A and structure B.

Figure 5 indicates a comparison of the variation curves of the drain voltage and drain current with time during switching of structure A and structure B with above three groups' structural parameters. From Fig.5 we can see that during turn-on, the fall of the drain voltage with time and the rise of the drain current with time for structure B is obviously faster than that of structure A as shown in Fig.5(a), and the turn-on time of structure B is obviously shorter than that of structure A. Similarly, during turn-off, the rise of the drain voltage with time and the fall of the drain current with time for structure B is obviously faster than that structure A as shown in Fig.5(b), and the turn-off time of structure B is obviously shorter than that of structure A. This is because the C_{IN} and C_{OUT} of structure B are obviously smaller than that of structure A. And W_n has hardly influence on switching characteristic.

The above results prove that the new trench gate SJ MOSFET has an excellent switching, blocking and conducting characteristics at the proper structural parameter, and the variation of W_n can hardly change obviously the characteristics. In other words, the new trench gate SJ MOSFET needs hardly to control exactly the width of n-pillar region, which offers more freedom to device design.



(a) turn-on characteristics (b) turn-off characteristics

Fig.5. Comparison of switching characteristics of structure A and structure B.

5. Realization

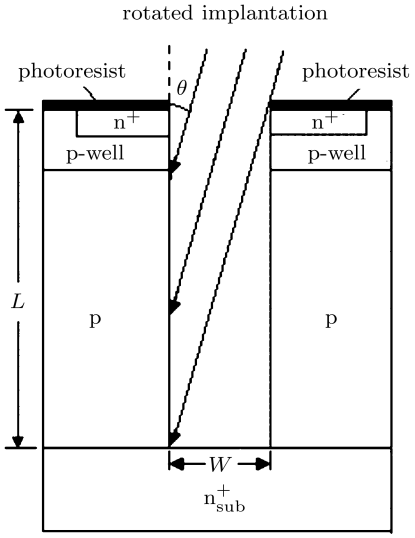
5.1. Shallow angle implantation

The n-pillar region in the new trench gate SJ MOSFET can be formed by shallow angle implantation. Figure 6 is the sketches of shallow angle implantation and the formed n-pillar regions after implantation, in which θ is the incident angle of implantation. From Fig.6(a) we can see that θ is related to the aspect ratio of the trench, and it can be expressed approximately by the following formula:

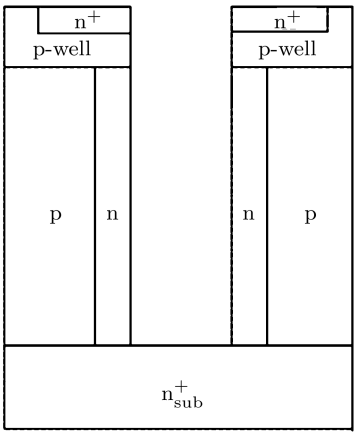
$$\theta \approx \arctan\frac{W}{L}. \tag{3}$$

Where W is above width of the trench region, and L is the depth of the trench region, which is 9.5 μm in

the new trench gate SJ MOSFET. Based on formula (3), corresponding to the W_n of 1.0 μm, 0.8 μm and 0.5 μm, θ is about 23°, 25° and 28° respectively. The larger θ angle is helpful to reduce the implantation doping error and difficulty of process, so the n pillar width can be chosen as 0.5 μm, and θ can be chosen as 28°.



(a) shallow angle implantation



(b) formed n pillar after implantation

Fig.6. The sketch of shallow angle implantation.

5.2. Process flow

The new trench gate SJ MOSFET structure can be fabricated by the following process flow. Firstly, a p-type layer and p^+ layer are grown in turn on the n^+ substrate by epitaxy, and to avoid the channel concentration is compensated by shallow angle implantation, the difference of the concentrations of p-type layer and p^+ layer equals to the concentration of n-pillar region. Secondly, p-well and n^+ source regions are formed in turn by ion implantation. After that, the trench whose width is 5 μm and the depth is 9.5 μm is formed in the whole p-type epitaxial layer by reactive ion etching, and then the n-pillar region is formed by shallow 28° angle implantation from the sidewall surface. Next, the filled oxide is formed by chemical vapour deposition. Finally, the formation of polysilicon gate and the decrease of the substrate thickness are similar to the process of conventional trench gate MOSFET.

The SJ in new trench gate SJ MOSFET structure can be implemented easily by using trench etching and shallow angle implantation, whose feasibility has been validated,[2] the formation of SJ only needs to control accurately the implantation dose of n pillar region, which offers more freedom to device fabrication. Comparatively, in conventional trench gate SJ MOSFET structure, the formation of SJ needs multi-step epitaxy growth combined with ion implantation[1] or multiple ion implantation,[6] or trench-filling combined with trench etching and epitaxy growth.[7−9] It is difficult to control accurately the doping of n pillar and p pillar regions. This shows that the new structure has simpler fabrication process than the conventional trench gate SJ MOSFET.

6. Conclusion

The presented oxide filled extended trench gate SJ MOSFET structure can further meet the requirements of higher frequency power switches application. Compared with the conventional trench gate SJ MOSFET, new structure has the smaller input and output capacitances, and has remarkable improvements in the breakdown voltage, on-resistance and switching speed. Furthermore, the n-pillar region located in the trench sidewall can be realized by the existing shallow angle implantation. This shows that the new structure can offer more freedom to the design and fabrication of SJ MOSFET device, and has simpler fabrication process than the conventional trench gate SJ MOSFET.

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