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Characteristics of high-quality HfSiON gate dielectric prepared by physical vapour deposition*

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This paper presents a method using simple physical vapour deposition to form high-quality hafnium silicon oxynitride (HfSiON) on ultrathin SiO_2 buffer layer. The gate dielectric with 10 Å (1Å = 0.1 nm) equivalent oxide thickness is obtained. The experimental results indicate that the prepared HfSiON gate dielectric exhibits good physical and electrical characteristics, including very good thermal stability up to 1000°C, excellent interface properties, high dielectric constant ($k = 14$) and low gate-leakage current ($I_g = 1.9 \times 10^{-3}$ A/cm^2@$V_g = V_{fb} - 1$ V for EOT of 10 Å). TaN metal gate electrode is integrated with the HfSiON gate dielectric.The effective work function of TaN on HfSiON is 4.3 eV, meeting the requirements of NMOS for the metal gate. And, the impacts of sputtering ambient and annealing temperature on the electrical properties of HfSiON gate dielectric are investigated.

Keywords: HfSiON, high-k gate dielectric, sputtering, leakage current
PACC: 7360, 7755

1. Introduction

With continuous scaling down of CMOS devices, SiO_2 or SiON as gate dielectric is approaching its fundamental limit. With reduction of physical thickness in the gate oxide, the gate leakage current is too large to meet the low power requirement. To overcome this limit, high dielectric constant (high-k) gate dielectrics have been introduced as a replacement for conventional gate dielectrics. High-k gate dielectrics can realize the same equivalent oxide thickness as SiO_2 with thicker physical thickness, which can reduce the gate leakage current greatly.

Many high-k materials have been investigated in these years, such as HfO_2,[1] ZrO_2,[2] HfSiON,[3] HfAlON,[4] and so on. Among these materials, HfSiON is considered as one of the most promising candidates for replacing conventional SiO_2 or SiON because of its relatively high dielectric constant, wide bandgap, superior thermal stability, better time-dependant dielectric breakdown reliability and electrical stability on charge trapping.

In the past few years, different deposition techniques have been developed to form HfSiON gate dielectric, such as physical vapour deposition (PVD), metal-organic chemical vapour deposition (MOCVD) and atomic layer deposition (ALD). Among these techniques, MOCVD can give conformal coverage over complex shapes and ALD can grow the thinnest films. But their disadvantage is that they generally introduce impurities into the high-k layers, such as C, H or Cl, depending on precursor. As opposed to MOCVD and ALD techniques, PVD has the main advantage of not suffering from contamination. Sputtering is one of a number of PVD methods, which is broadly available.

In this paper, the HfSiON high-k gate dielectric was prepared by co-sputtering of Hf and Si targets in an Ar/N_2 ambience, followed by a rapid thermal oxidation. To ensure the interface quality and isolate the high-k layer from Si surface, an ultra-thin high quality SiO_2 buffer layer was grown on Si substrate before high-k layer deposition. The TaN metal gate was deposited on the HfSiON gate dielectric as the gate electrode. The physical and electrical characteristics of HfSiON gate dielectric were analysed.

2. Fabrication

After standard clean process, silicon wafer was treated with a HF+IPA+H_2O solution to prevent the contamination of particle, metal ion and organism, as

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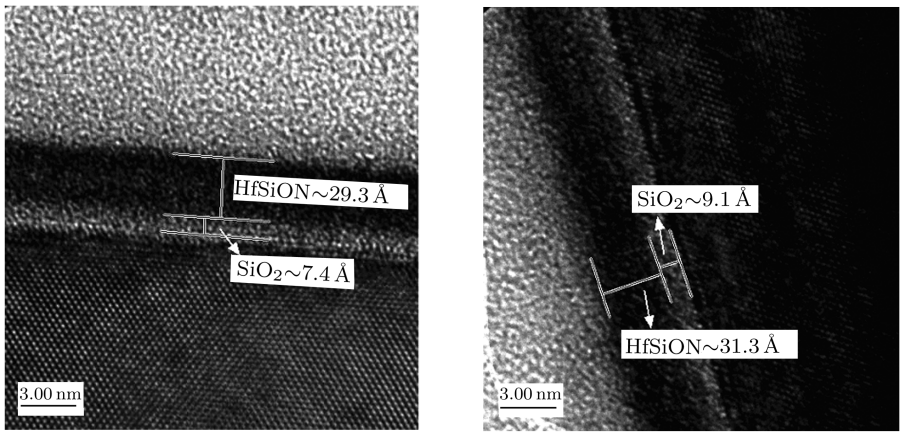
well as to suppress the growth of natural oxide.[5] SiO_2 buffer layer was grown on the silicon wafer by rapid thermal oxidation. The HfSiON (∼30Å, 1Å = 0.1 nm) film was then deposited onto the SiO_2 buffer layer by co-sputtering of Hf and Si targets at room temperature in an Ar/N_2 ambience. The work pressure was kept at 5×10^{-3} Torr (1 Torr = 133 Pa). After deposition, the post deposition annealing (PDA) using rapid thermal annealing was performed in an N_2/O_2 ambience at different conditions (800 °C/30 s, 900 °C/30 s and 1000 °C/20 s). An 1800Å TaN as metal gate electrode was deposited by PVD. Finally, all samples were metallized with Al(Si) on backside at 380 °C in an N_2 ambience for 40 min.

3. Results and discussion

3.1. Physical characteristics

In this study, high resolution transmission electronic micrograph (HRTEM) is used to analyse microstructure thickness of HfSiON film and situation of interface. The chemical composition and bonding states of HfSiON film were investigated by the x-ray photoelectron spectroscopy (XPS) measurements with the incidence of a monochromatic Al Kα(1486.6 eV) x-ray. The binding energy was referenced to C1s at 284.5 eV.

Figure 1 shows the HRTEM images for HfSiON gate dielectrics as deposition and after 1000 °C PDA, respectively. HfSiON gate dielectrics have uniform thickness and remain amorphous after 1000 °C PDA, this indicates that HfSiON gate dielectrics have high crystallization temperature and excellent thermal stability. As deposition, the thickness of SiO_2 buffer layer is 7.4 Å, as shown in Fig.1(a). After 1000 °C PDA, the buffer layer becomes thicker and its thickness increases to 9.1 Å, as shown in Fig.1(b). This is because oxygen atoms pass through HfSiON gate dielectric and react with Si substrate, forming thicker SiO_2 layer.[6,7] SiO_2 buffer layer is helpful to suppress the reaction of HfSiON gate dielectric on Si substrate, which prevents the formation of thicker low-k interfacial layer. All these are favourable for improvement of devices' electrical characteristics.



(a) As deposition (b) 1000 °C

Fig.1. HRTEM images of HfSiON gate dielectrics as deposition and after 1000 °C PDA.

Figure 2 shows the result of XPS analysis of HfSiON gate dielectric after 800 °C PDA. The nitrogen composition in HfSiON is 16 at.%, the oxygen composition is 54 at.% and the Hf composition ratio [Hf/(Hf+Si)] is about 42%. An investigation of the bonding states of HfSiON film indicates that undesirable metallic bonds (Hf-Si and Hf-Hf) do not exist in the high-k layer. Si-O-Hf bonds, which are unique to Hf-silicate, are dominant in the film. Analysis of N1s spectrum reveals that there are only Si-N bonds existed in the film. Experimental results indicate that Si-N bonds are stable and do not decompose at high temperature while Hf-N bonds are easily replaced by oxygen forming Hf-O bonds.[8] Si-N bonds can passivate the dangling Si bonds, resulting in low charge densities for both interface-state and dielectric-charge, which are beneficial to enhance reliability.[9]

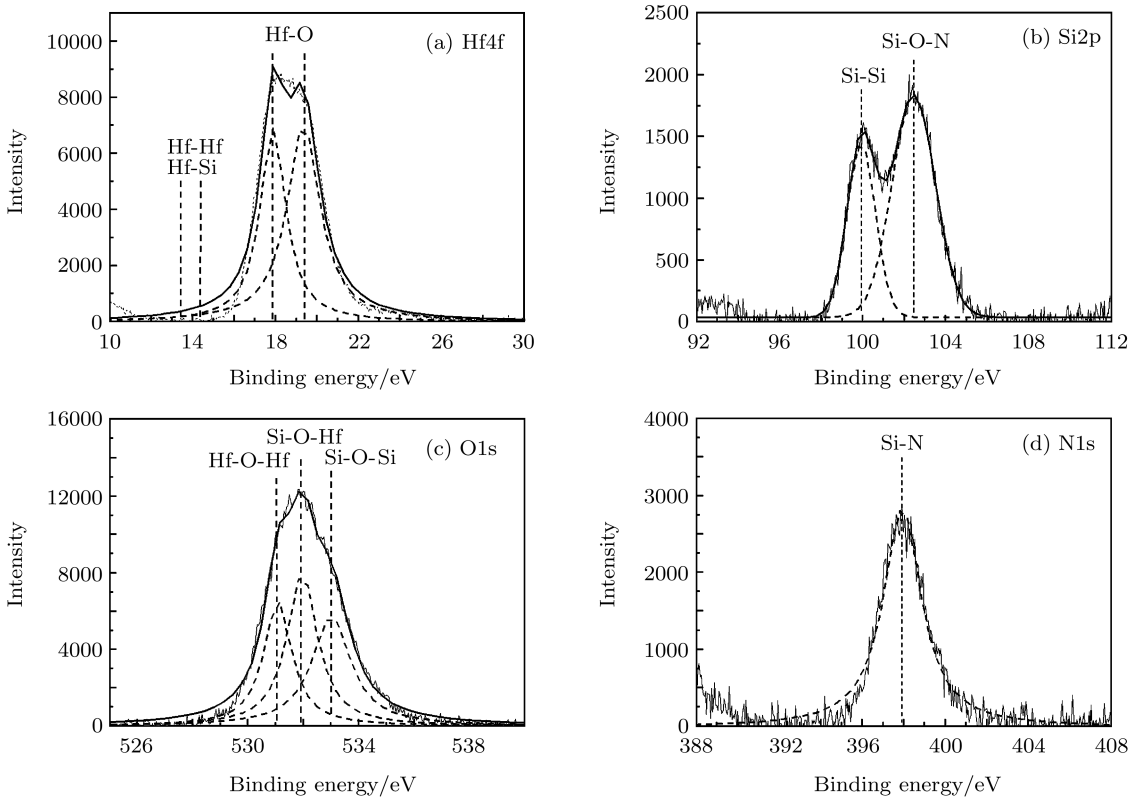


Fig.2. XPS spectra for HfSiON gate dielectric after 800 °C PDA.

3.2. Electrical characteristics

High-frequency (1 MHz) capacitance-voltage ($C-V$) characteristics were measured at room temperature by using Materials Development Corporation (MDC) $C-V$ analyser. The $I-V$ leakage-current characteristics were measured by using Keithley 4200 semiconductor parameter analyser.

The equivalent oxide thickness of 10 Å is extracted from the $C-V$ curve (not shown), which is fitted by quantum mechanical $C-V$ simulator developed by the Device Group at UC Berkeley. According to HRTEM analysis and the equivalent oxide thickness (EOT) extracted from the $C-V$ curve, we calculated that the average value of k of HfSiON gate dielectric is 14. The measurements show that the gate leakage current of HfSiON gate dielectric with EOT = 10 Å is 1.9×10^{-3} A/cm^2 at $V_{\rm fb}-1$ V, which is better than 0.036 A/cm^2 obtained from HfSiON gate dielectric prepared by MOCVD.[11] Comparing the pure SiO_2 of identical EOT, we obtain a more than 10^4 times reduction on leakage current for HfSiON gate dielectric, as shown in Fig.3. This is because HfSiON gate dielectric is physically thicker than SiO_2 as the same EOT, hence reduces the leakage current greatly. The stress-induced leakage current (SILC) of HfSiON/SiO_2 gate dielectric is measured at $V_{\rm g}=-3$ V constant voltage stressing, as shown in Fig.4. A significant increase in SILC at low $V_{\rm g}=-1$ V is observed in HfSiON/SiO_2 gate dielectric prepared by Wang X G *et al*,[10] while a small amount of SILC increase is found in the HfSiON/SiO_2 gate dielectric prepared in this work. SILC is correlated to the trap-assisted tunnelling and its increase reflects the traps generation during stressing. So, HfSiON/SiO_2 gate

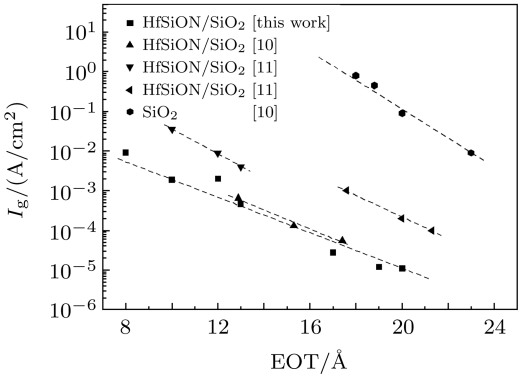


Fig.3. EOT dependence of the gate leakage current at $V_{\rm g}=V_{\rm fb}-1$ V for HfSiON/SiO_2 gate dielectrics.

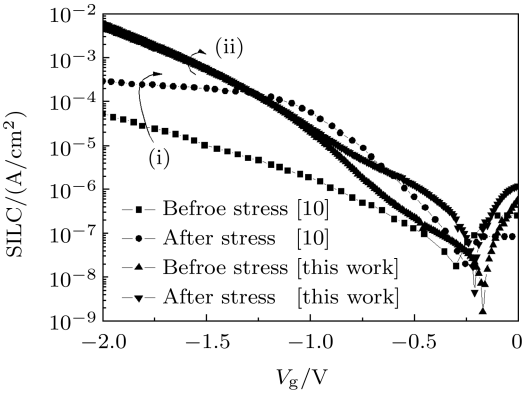


Fig.4. SILC curve of HfSiON/SiO_2 gate dielectrics. (i) HfSiON/SiO_2 (EOT = 18.1 Å) stressed at $V_g = -3$ V for 100 s.[10] (ii) HfSiON/SiO_2 (EOT = 10 Å) stressed at $V_g = -3$ V for 300 s.[This work]

dielectric prepared in this work has excellent SILC characteristics and its interface states-assisted tunnelling is smaller.

There is always Fermi-level pinning effect existed between poly-silicon and high-k gate dielectric, which causes a lot of trouble for work function tuning. In this study, TaN metal gate was used on HfSiON gate dielectric as the gate electrode. The calculation of the metal gate work function is based on the following equations:

$$\Phi_m = \Phi_s + \Phi_{ms}, \tag{1}$$

$$\Phi_{ms} = V_{FB} + \frac{Q_0}{\varepsilon_0 \varepsilon_{HK}} \times \text{EOT}. \tag{2}$$

Where, Φ_m and Φ_s are the work functions with respect to the metal gate and Si substrate, V_{FB} is the flat band voltage, Q_0 is the equivalent electronic charge, ε_0 is the vacuum permittivity and ε_{HK} is the permittivity of high-k gate dielectric. The value of Φ_{ms} is equal to V_{FB} when EOT = 0.[12] In order to exact the work function of TaN metal gate, HfSiON films were prepared with different EOT. The V_{FB} versus EOT plot is shown in Fig.5. The effective work function of TaN

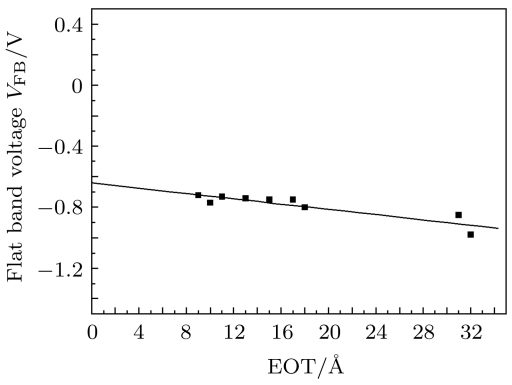


Fig.5. V_{FB} versus EOT plot of TaN metal gate on HfSiON gate dielectrics.

metal gate on HfSiON gate dielectric exacted is 4.3 eV. There is no Fermi-level pinning effect existed between TaN metal gate and HfSiON gate dielectric.

3.3. Effect of process conditions on the electrical properties of HfSiON gate dielectric

3.3.1. Effect of sputtering ambience

The nitrogen atoms in HfSiON gate dielectric may enhance the electronic and lattice polarization, both of which contribute to the enhancement of the dielectric constant.[9] In sputtering process, nitrogen atoms content in gate dielectric is modulated by adjusting N_2 flow rate. Higher N_2 flow rate can increase N_2 gas content in the sputtering chamber and more nitrogen atoms are incorporated into the gate dielectric, which enhance its dielectric constant. In this study, we compare the high frequency $C-V$ characteristics of HfSiON gate dielectrics deposited with different N_2 flow rate of 3 or 5 SCCM respectively, as shown in Fig.6. Comparing capacitances in accumulation of the two samples, we find that the capacitance increases with the N_2 flow rate, which indicates that higher dielectric constant was obtained by increasing N_2 flow rate.

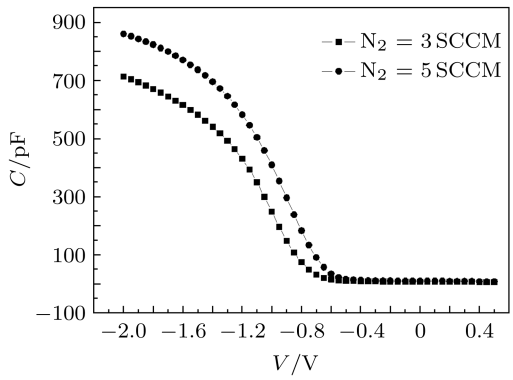


Fig.6. $C-V$ curves of HfSiON gate dielectrics deposited with different N_2 flow rate.

3.3.2. Effect of PDA

In this study, we investigate the high frequency $C-V$ characteristics of HfSiON gate dielectrics annealed at different PDA temperatures (800 °C and 900 °C), as shown in Fig.7. Comparing capacitances in accumulation of the two samples, we find that the capacitance of the sample annealed at 800 °C is higher than that annealed at 900 °C, this indicates that thicker SiO_2 buffer layer was formed at higher

temperature, resulting in the equivalent oxide thickness increase and dielectric constant decrease.

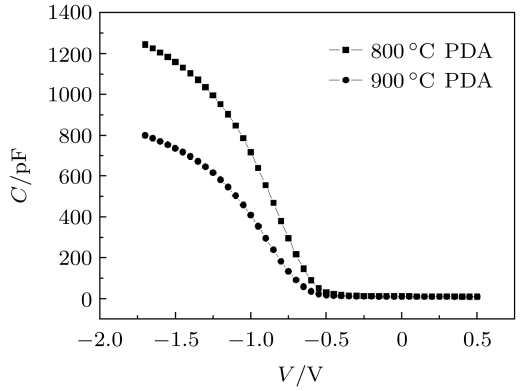


Fig.7. $C-V$ curves of HfSiON gate dielectrics annealed at different PDA temperatures.

4. Conclusion

The HfSiON high-k gate dielectrics were fabricated by co-sputtering Hf and Si targets, followed by a rapid thermal annealing in an N_2/O_2 ambience. The HfSiON gate dielectrics exhibit very good physical and electrical characteristics, including good thermal stability up to 1000 °C, excellent interface properties, high dielectric constant and low gate-leakage current. The HfSiON gate dielectric with 10Å EOT value is obtained. Its leakage current is only 1.9×10^{-3} A/cm^2 ($V_g = V_{fb}-1$ V). The introduction of SiO_2 buffer layer is helpful to suppress the interfacial layer formation and improve the quality of interface, this is important to obtain higher k value and better reliability. The k value of HfSiON gate dielectric is 14. After constant voltage stressing of -3 V for 300 s, the stress-induced leakage current increase is low. The effective work function of TaN metal gate on HfSiON gate dielectric is 4.3 eV, which indicates that there is no Fermi-level pinning existed between TaN metal gate and HfSiON gate dielectric. TaN is one of the most suitable metal gate materials for NMOS. The impacts of sputtering ambience and post-annealing temperature on the electrical properties of HfSiON gate dielectric are important and have been investigated carefully. The excellent characteristics observed in HfSiON gate dielectric suggest that it may be a very promising gate dielectric, which has the potential to replace the conventional SiO_2 or SiON as gate dielectric for advanced CMOS devices.

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