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Study on the degradation of NMOSFETs with ultra-thin gate oxide under channel hot electron stress at high temperature*

Hu Shi-Gang(胡仕刚)†, Hao Yue(郝 跃), Ma Xiao-Hua(马晓华), Cao Yan-Rong(曹艳荣), Chen Chi(陈 炽), and Wu Xiao-Feng(吴笑峰)

School of Microelectronics, Xidian University, Xi'an 710071, *China*
Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, Xi'an 710071, *China*

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This paper studies the degradation of device parameters and that of stress induced leakage current (SILC) of thin tunnel gate oxide under channel hot electron (CHE) stress at high temperature by using n-channel metal oxide semiconductor field effect transistors (NMOSFETs) with 1.4-nm gate oxides. The degradation of device parameters under CHE stress exhibits saturating time dependence at high temperature. The emphasis of this paper is on SILC of an ultra-thin-gate-oxide under CHE stress at high temperature. Based on the experimental results, it is found that there is a linear correlation between SILC degradation and $V_{\rm h}$ degradation in NMOSFETs during CHE stress. A model of the combined effect of oxide trapped negative charges and interface traps is developed to explain the origin of SILC during CHE stress.

Keywords: threshold voltage, interface traps, stress induced leakage current
PACC: 7340Q, 7300, 7340G

1. Introduction

Since hot carrier effects can pose a potential limit to device scaling, hot-carrier-induced device degradation has been one of the major concerns in modern device technology. Many researchers have studied hot carrier effects along with various structures to relieve hot carrier problems in metal oxide semiconductor (MOS) technology.[1−5] However, most of the studies were done at room temperature and little has been done for the study of hot carrier effects at high temperature.[6−11]

Stress induced leakage current (SILC) is a major concern for the long-term reliability and scaling of the tunnel oxide in nonvolatile memories.[12−18] SILC plays an important role in the reliability of devices. However, few studies have concentrated on SILC in metal oxide semiconductor field effect transistors (MOSFETs) under hot-carrier stress.

In this work, hot carrier effects in n-channel MOS devices are studied with the emphasis on high-temperature behaviour. Based on the experimental data, a comprehensive discussion of hot carrier degradation at high temperature is presented. The degradation of device parameters under channel hot electron (CHE) stress exhibits saturating time dependence at high temperature. It is found experimentally that there is a linear correlation between the degradation of SILC and that of $V_{\rm th}$ during the stress. A conclusion is drawn on the mechanism of SILC in the ultra-thin gate oxide lightly doped drain (LDD) n-channel metal oxide semiconductor field effect transistor (NMOSFET) under stress due to the combined effect of oxide charge trapping and interface traps.

2. Devices and experiments

The devices used in this paper are LDD NMOSFETs, fabricated in a standard 90-nm CMOS technology. The LDD NMOSFET is a surface device with N^+ poly-Si gate. The gate oxide thickness ($T_{\rm ox}$) of the device is 1.4 nm with decoupled-plasma-nitridation (DPN) processing. The MOSFETs have a channel length of 1 μm, width of 40 μm and gate oxide thickness of 1.4 nm. The operation voltage is 1.0 V for the MOSFETs. An Agilent B1500A high-precision semiconductor parameter analyser was used to conduct the tests.

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†Corresponding author. E-mail: hsg99528@126.com

The CHE stress and I–V measurements were made by an Agilent B1500A semiconductor parameter analyser. The CHE stress was performed at $V_{gs} = V_{ds} = +1.6$ V. Stress was interrupted at regular intervals and device parameters were measured. The SILCs were characterized by measuring the I–t (gate current–stress time) characteristics at constant, low, pre-tunnelling voltages at regular intervals. The experiments were carried out at 90, 120, and 150 °C.

3. Results and discussion

The degradation of device parameters under CHE stress at 120 °C is presented as shown in Fig.1.

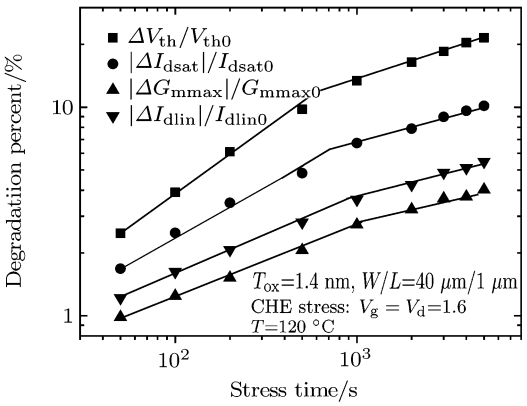


Fig.1. Time dependence of degradation of device parameters in the NMOSFET under CHE stress.

The degradation characteristics can exhibit saturating time dependence at high temperature. It is observed that the degradation rate (slope of the time dependence plots) of all the parameters decreases with increasing stress time (i.e. the rate coefficient saturates). The observed phenomenon can be explained as a two-stage degradation in the LDD NMOSFET.[19−22] The two-stage mechanism is due to the combined effect of an increase in series resistance in the LDD region, and a reduction of carrier mobility in the channel/LDD overlap region. The series resistance eventually saturates, leaving mobility reduction as the mechanism responsible for the degradation in the latter stage. These saturating characteristics make the conventional $A*t^n$ time dependence extrapolation inconsistent and inaccurate. Figure 1 shows the time dependence of degradation of device parameters on a log–log scale under CHE stress at 120 °C. The V_{th} in the NMOSFET increases and the other parameters in the NMOSFET decrease with stress time. The V_{th} degradation is the most serious, the I_{dsat} degradation is the second, and the I_{dlin} degradation is larger than the G_{mmax} degradation. Figure 2 shows the time dependence of V_{th} degradation in the NMOSFET during CHE stress at different temperatures. With increasing temperature, the degradation of V_{th} becomes severe.

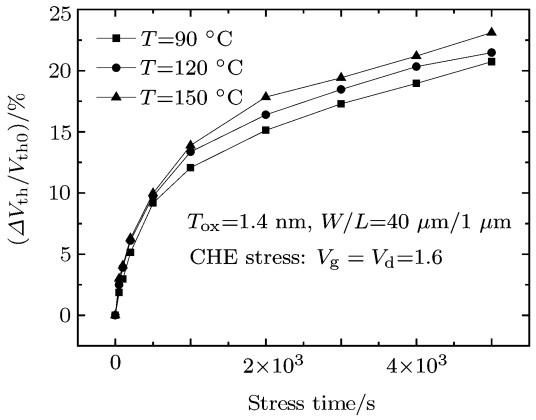


Fig.2. Time dependence of V_{th} degradation in the NMOSFET under CHE stress at different temperatures.

We suppose $(I_g - I_{g0})/(I_{g0})$ as the SILC, where I_g is the gate leakage current measured from the interruption of stresses, and I_{g0} is the initial gate leakage current. Figure 3 shows the time evolution of SILC measured at different positive gate voltages under CHE stress in LDD NMOSFET. The SILC in the NMOSFET decreases with increasing stress time and also gets saturated after a long stress time as shown in Fig.3(a). The SILC is strongly dependent on the measured gate voltage. The higher the measured gate voltage, the less the degradation of the gate current. The time evolution of SILC on a log–log scale under CHE stress in NMOSFET is shown in Fig.3(b). The degradation slope of SILC becomes smaller with increasing stress time. The degradation characteristic of SILC also shows saturating time dependence at high temperature. Figure 4 shows the time evolution of SILC measured at a fixed positive gate voltage under CHE stress at different temperatures. With increasing temperature, the degradation of SILC becomes severe.

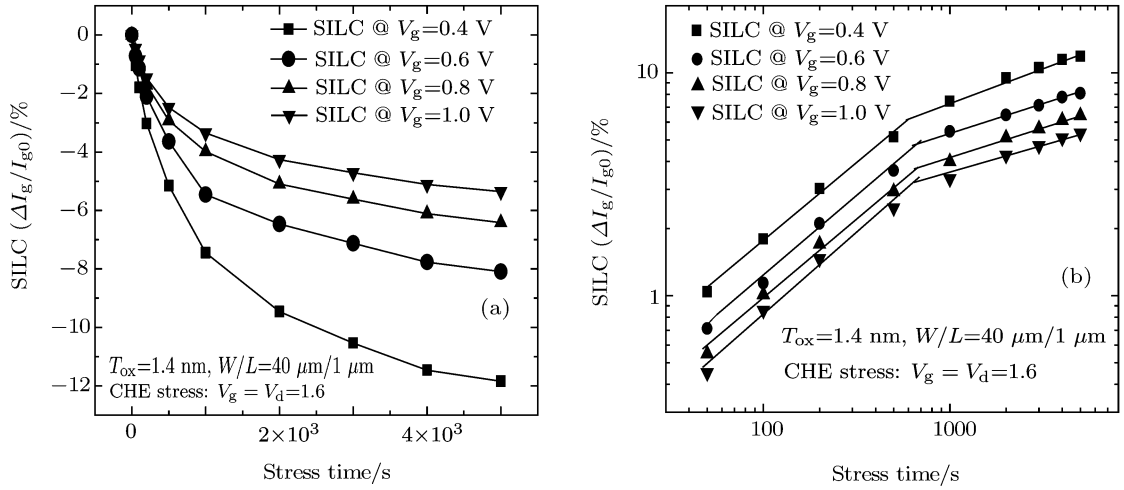


Fig.3. Time evolution of SILC at different measured gate voltages under CHE stress in the NMOSFET: (a) linear–linear scale; (b) log–log scale.

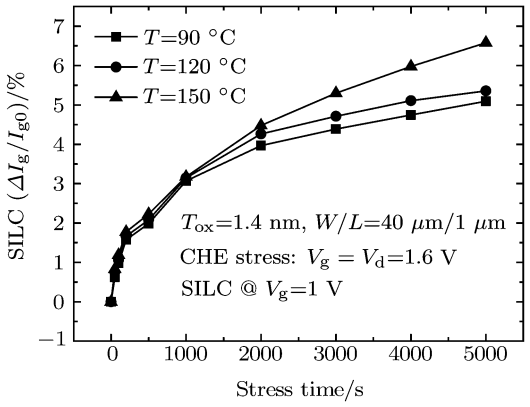


Fig.4. Time evolution of SILC measured at fixed positive gate voltage under CHE stress at different temperatures.

In our experiments, an interesting fact is observed that there is a good linear correlation between the degradation of SILC and that of V_{th} in MOSFETs during this stress as shown in Fig.5. It is also observed that the slopes of the lines in Fig.5 are smaller than 1 and V_{th} degradation is larger than SILC degradation. By making a good analysis on the result, we can investigate the origin of SILC in MOSFETs during CHE stress at high temperature.

Hot carrier effects are usually referred to damage of the Si/SiO_2 interface state and charge trapping in the oxide due to the high channel electric field. Electrons gain kinetic energy from the lateral electric field, and some can overcome the $Si–SiO_2$ barrier height and then inject into the oxide. Some of them are trapped in the oxide and become oxide trapped negative charges. There are two ways to cause interface state generation: one is due to recombination with trapped carriers, and the other is due to breakage of Si–H bonds by energetic electrons.[23] Interface states will lead to mobility degradation by scattering interaction with channel electrons. Mobility degradation leads to the drain current degradation. Charge trapping and interface state generation can change the charge distribution and influence the threshold voltage. The origin of source-drain resistance is the injection of charge, either in the form of fixed charge or as interface states, into the spacer oxide above the LDD region. At high temperature the degraded region drifts from the near-drain region toward the channel region. The degradation characteristics can

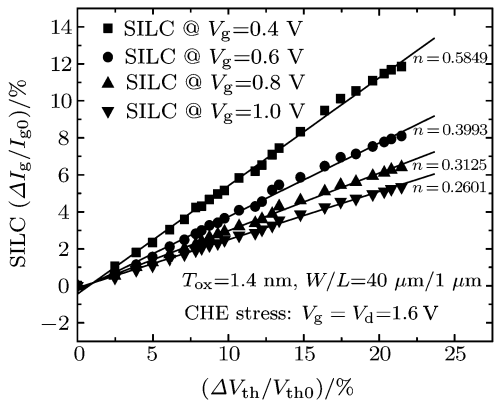


Fig.5. SILC variation versus V_{th} variation under CHE stress in the NMOSFET.

exhibit saturating time dependence at high temperature. Those saturating characteristics are due to the combined effect of an increase in series resistance in

the LDD region, and a reduction of carrier mobility in the channel/LDD overlap region.

The origin of SILC has been reported many times.[24−28] Some models have been presented to investigate the SILC, among which the trap assisted tunnelling model, the thermal assisted tunnelling model and the resonant tunnelling model are the most popular. However, no complete agreement has been reached. In this paper, it is not easy to analyse the SILC in such ultra-thin 1.4-nm thick oxide by using these models. The SILC is measured by interrupting stress at regular intervals. There is a good linear correlation between SILC degradation and $V_{\rm th}$ degradation in MOSFETs during CHE as shown in Fig.5. As the shift of $V_{\rm th}$ results from the generation of interface traps and oxide trapped negative charges, there should be some connection between the degradation of gate leakage current and their generation. We develop a model with interface traps and oxide trapped negative charges to explain the SILC here.

The model with interface traps and oxide trapped negative charges influencing SILC is schematically shown in Fig.6. The SILC is measured at constant, low and positive voltages after CHE stress. When the measurement voltage is applied, there are interface traps and oxide trapped negative charges, which have been generated. When the gate voltage is much larger than 0 V as shown in Fig.6, electrons can emit from the inverted channel. An energy band diagram for the measurement of SILC in the NMOSFET under CHE stress is drawn in Fig.6. Interface traps at the Si/SiO_2 interface can serve as a stepping stone. They can effectively capture the electrons from the inverted channel and then immediately emit them. Meanwhile, the oxide trapped negative charges prevent electrons tunnelling through the oxide by enhancing the barrier height and lowering the electric field in the oxide. The oxide trapped negative charges play a more important role in the degradation of SILC than the interface traps do. Therefore, due to the combined effect of oxide charge trapping and interface traps, SILC decreases with increasing stress time. In addition, SILC is dependent on the measuring gate voltage. When the measuring gate voltage is higher, the number of electrons in the inverted channel will increase and the electric field in the oxide will be enhanced. Then electrons from the inverted channel can emit toward the gate oxide more easily. Although the trapped negative charges can prevent electrons from tunnelling, more electrons can tunnel through the oxide with the help of interface traps at higher measuring voltage. So SILC degradation becomes less serious at higher measuring voltages.

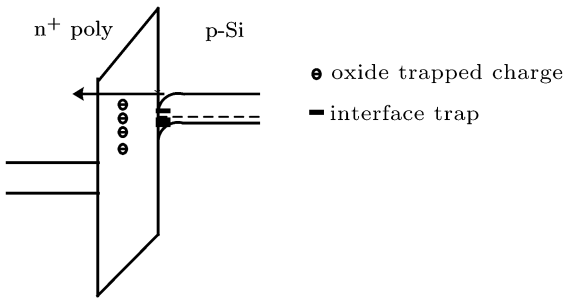


Fig.6. Schematic diagram of a model with interface traps and oxide trapped charges influencing SILC during the measurement of SILC.

The $V_{\rm th}$ is one of the most important parameters. It is well known that $V_{\rm th}$ in NMOSFETs can be expressed as

$$V_{\rm th} = 2\phi_{\rm F} + \frac{\sqrt{2qK_{\rm s}\varepsilon_{\rm o}N_{\rm A}(2\phi_{\rm F})}}{C_{\rm ox}} + \phi_{\rm MS} - \frac{\lambda Q_{\rm ox}}{C_{\rm ox}} - \frac{Q_{\rm it}(\phi_{\rm s}=2\phi_{\rm F})}{C_{\rm ox}}, \quad (1)$$

where $\phi_{\rm F}$ is the Fermi potential, q the electron charge, $K_{\rm s}$ the silicon dielectric constant, ε_0 the permittivity of free space, $N_{\rm A}$ the acceptor doping concentration, $C_{\rm ox}$ the oxide capacitance, $\phi_{\rm MS}$ the metal-semiconductor work function difference, and λ the charge distribution factor.[29] Here, $Q_{\rm ox}$ is defined as the trapped-oxide sheet charge density which includes all charge components that are not sensitive to silicon surface potential such as the trapped-oxide charge and the fixed oxide charge, λ is the charge distribution factor and $Q_{\rm it}$ is the interface trapped charge density at Si/SiO_2 interface which depends on the surface potential $\phi_{\rm s}$. The shift of $V_{\rm th}$ is caused by the increase of oxide trapped negative charges and interface traps in NMOSFET during CHE stress at high temperature. For the NMOSFET, interface traps are charged negatively during the measurement, and the trapped-oxide charges are negative. Interface traps make $V_{\rm th}$ drift positively and the oxide trapped negative charges also make $V_{\rm th}$ drift positively. But from the model as shown in Fig.6, we can see that the trapped negative charges and interface traps in NMOSFET during CHE stress temperature play different roles in the degradation of SILC. So $V_{\rm th}$ degradation is larger than that of SILC degradation as shown in Fig.5.

Figure 4 shows the SILC during CHE stress sensed at $V_g = 1$ V at different temperatures. With increasing temperature, the degradation of SILC becomes severe and a larger combined effect on SILC from oxide charge trapping and interface traps is indicated. During CHE stress, more interface traps and negative charges are generated with the increased temperature. The change in SILC with stress temperature shows that the degradation process is thermally activated. The activation energies of SILC sensed at $V_g = 1$ V and V_{th} degradation during CHE stress can be extracted from the Arrhenius plot as shown in Fig.7. The activation energies are 0.0221 and 0.0201 for V_{th} degradation and SILC degradation respectively. The similar activation energies show the correlation between SILC and V_{th} degradation during CHE stress at different temperatures, and indicate the relations to the interface traps and oxide charge trapping. Therefore, it is proven that the model is dependable.

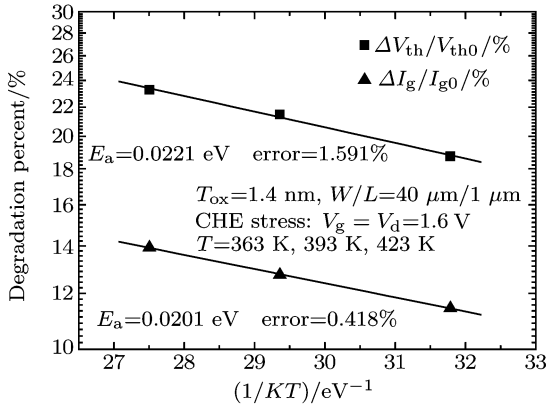


Fig.7. Arrehenius plot showing temperature dependence of SILC sensed at $V_g = 1$ V and V_{th} degradation during CHE stress.

4. Conclusion

The degradation of devices has been investigated in detail under CHE stress at high temperature in this paper. Firstly, the degradation of device parameters is presented. The degradation characteristics can exhibit saturating time dependence at high temperature. This is due to the combined effect of an increase in series resistance in the LDD region, and a reduction of carrier mobility in the channel/LDD overlap region. With increasing temperature, the degradation of devices becomes severe. Secondly, the SILC of ultra-thin gate oxide is also investigated. The degradation characteristic of SILC also shows saturating time dependence at high temperature. The SILC decreases with increasing stress time and also gets saturated after a long stress time as shown. The SILC is strongly dependent on the measuring gate voltage. The higher the measuring gate voltage, the less the degradation of the gate current. It has been found that there is a linear correlation between SILC degradation and V_{th} degradation in MOSFETs during CHE stress. We developed a model with interface traps and oxide trapped negative charges to explain the SILC here. It is confirmed that the degradation of V_{th} and that of SILC are interrelated due to the generation of interface traps and oxide charge trapping during CHE stress.

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