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A novel analytical thermal model for multilevel nano-scale interconnects considering the via effect*

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Based on the heat diffusion equation of multilevel interconnects, a novel analytical thermal model for multilevel nano-scale interconnects considering the via effect is presented, which can compute quickly the temperature of multilevel interconnects, with substrate temperature given. Based on the proposed model and the 65 nm complementary metal oxide semiconductor (CMOS) process parameter, the temperature of nano-scale interconnects is computed. The computed results show that the via effect has a great effect on local interconnects, but the reduction of thermal conductivity has little effect on local interconnects. With the reduction of thermal conductivity or the increase of current density, however, the temperature of global interconnects rises greatly, which can result in a great deterioration in their performance. The proposed model can be applied to computer aided design (CAD) of very large-scale integrated circuits (VLSIs) in nano-scale technologies.

Keywords: multilevel interconnects, temperature distribution, self-heating, via effect

PACC: 6630Q, 6185, 8160C

1. Introduction

With the development of the complementary metal oxide semiconductor (CMOS) process, the rapid scaling down of very large-scale integrated circuits (VLSIs) and interconnect size, and the continuous increase of current density and interconnect levels, the heating problem is becoming more and more serious in VLSIs. The increase of temperature rise of on-chip interconnects has been a very important restriction on high-performance VLSIs.[1−12] A serious interconnect temperature rise results in not only a great deterioration in the VLSI's performance, but also the falsity of electro-migration and reliability. In recent years, a variety of low-k insulating materials have been used to reduce the RC delay, dynamic power dissipation and crosstalk noise.[2,3] These insulating materials, however, also have poor thermal properties which result in the increase of interconnect temperature rise, thereby reducing the reliability of chips and increasing the resistance and RC delay greatly. Therefore, for VLSI design, it is important and necessary to give a detailed analysis of the self-heating and heat diffusion of interconnects, and to achieve a more realistic temperature distribution of interconnects.

The number of interconnect layers of the nano-scale CMOS process has reached 9,[12] and a low-k insulating material is used, so nano-scale interconnect temperature distribution must be more complicated than deep submicron interconnect temperature distribution, and the multilevel interconnect temperature distribution is even more complicated. At present, the main research work of thermal analysis concentrates on the single interconnect;[4−6] these thermal analysis models include only the self-heating effect and the heat fringing effect. In fact, however, heat conduction occurs between neighbouring interconnect layers, which means that the interconnect can absorb heat from the upper interconnect layer. So these thermal analysis models have a big flaw when used to estimate the temperature of multilevel interconnects.

In the present paper, based on the heat diffusion equation for multilevel interconnects, a novel thermal distribution model for multilevel interconnects considering the via effect is first proposed. Based on the proposed model and the 65 nm CMOS process parameter, the temperature rise of multilevel interconnects is computed and a discussion and analysis of its influence on the via effect and thermal conductivity are given.

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2. Thermal distribution model for multilevel interconnects

Figure 1 shows a multi-level interconnect structure model. The mth interconnect layer width is $w_{m,m}$, and its thickness and temperature distribution are $t_{m,m}$ and $T_m(x)$ respectively. The $(m+1)$th interconnect layer width is $w_{m,m+1}$, and its thickness and temperature distribution are $t_{m,m+1}$ and $T_{m+1}(x)$ respectively. The $(m-1)$th interconnect layer width is $w_{m,m-1}$, and its thickness and temperature distribution are $t_{m,m-1}$ and $T_{m-1}(x)$ respectively.

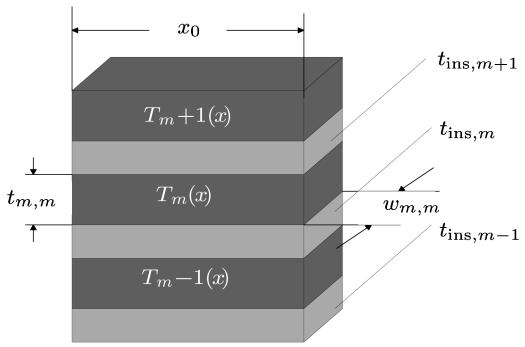


Fig.1. Multi-level interconnect structure model.

For the mth interconnect layer, under the steady-state condition, the heat diffusion equation is as follows:

$$\frac{\partial^2 T_m(x)}{\partial x^2}+\frac{\partial^2 T_m(x)}{\partial y^2}+\frac{\partial^2 T_m(x)}{\partial z^2}+\frac{Q_{\mathrm{eff}}}{K_m}=0. \quad (1)$$

Note that Q_{eff} is the effective heat generation per unit volume ($\mathrm{W/m^3}$), and K_m is the thermal conductivity of the metal ($\mathrm{W/m\cdot{}^\circ C}$).

The length of the interconnect line is sufficiently larger than its thickness or width, i.e. the thermal gradients along the thickness and the width of the interconnect line can be ignored in the study of these long interconnects. In that case, Eq.(1) can be reduced into a one-dimensional (1D) heat diffusion equation as follows:

$$\frac{\partial^2 T_m(x)}{\partial x^2}+\frac{Q_{\mathrm{eff}}}{K_m}=0. \quad (2)$$

Q_{eff} includes three parts, i.e. the heat generated by the self-heating effect, the heat flowing from the mth interconnect layer to the $(m-1)$th interconnect layer, and the heat absorbed from the $(m+1)$th interconnect layer, but most thermal models do not take this situation into consideration.[5,7] In order to give the thermal model easily, we assume that the heat conduction goes through the interlayer dielectric layer between neighbouring interconnect layers, so the heat generated by the self-heating effect at the mth interconnect layer with width $w_{m,m}$, thickness $t_{m,m}$, and length x_0 is as follows:

$$Q_{\mathrm{g},m}=(j_{\mathrm{rms},m}w_{m,m}t_{m,m})^2\frac{\rho_0 x_0}{w_{m,m}t_{m,m}}, \quad (3)$$

where $j_{\mathrm{rms},m}$ is the root-mean-square current density passing through the mth interconnect layer, and ρ_0 is the interconnect electronic resistivity.

Heat flowing from the mth interconnect layer to the $(m-1)$th interconnect layer through the interlayer dielectric layer m is given as follows:

$$Q_{\mathrm{out},m}=\frac{T_m(x)-T_{m-1}(x)}{\Delta R_m(x)}, \quad (4)$$

where

$$\Delta R_m(x)=\frac{t_{\mathrm{ins},m}}{k_{\mathrm{ins},m}w_{m,m}x_0}, \quad (5)$$

with $\Delta R_m(x)$ being the thermal resistance of theninsulator with width $w_{m,m}$, thickness $t_{\mathrm{ins},m}$, length x_0, and $k_{\mathrm{ins},m}$ being the effective insulator thermal conductivity. In fact, the heat flow path is assumed to go through the bottom side and partially through the two sides along the length of a rectangular shape, and a more accurate expression for $k_{\mathrm{ins},m}$ was given in Ref.[8] as follows:

$$k_{\mathrm{ins},m}=k_{\mathrm{ins}}\frac{t_{\mathrm{ins}}}{w_{m,m}}\cdot 1.685\left[\log\left(1+\frac{t_{\mathrm{ins}}}{w_{m,m}}\right)\right]^{-0.59}\times\left(\frac{t_{\mathrm{ins}}}{w_{m,m}}\right)^{-0.078}, \quad (6)$$

where k_{ins} is the insulator thermal conductivity.

Likewise, heat absorbed from the $(m+1)$th interconnect layer for a partial length x_0 through the interlayer dielectric layer $m+1$ is

$$Q_{\mathrm{in},m}=\frac{T_{m+1}(x)-T_m(x)}{\Delta R_{m+1}(x)}, \quad (7)$$

where

$$\Delta R_{m+1}(x)=\frac{t_{\mathrm{ins},m+1}}{k_{\mathrm{ins},m+1}w_{m,m}x_0}, \quad (8)$$

with $t_{\mathrm{ins},m+1}$ being the thickness of the interlayer dielectric layer $m+1$, and $k_{\mathrm{ins},m+1}$ being its effective thermal conductivity.

$k_{\mathrm{ins},m}$ and $k_{\mathrm{ins},m+1}$ do not include the via effect, so we introduce a via correction factor η, and $k^*_{\mathrm{eff},m}$ is defined as follows:

$$k^*_{\mathrm{eff},m}=k^*_{\mathrm{ins},m}/\eta, \quad (9)$$

where $k^*_{\mathrm{eff},m}$ is the effective insulator thermal conductivity, with the via effect included; the via correction factor η was given in Refs.[9] and [10] as follows:

$$\eta = 1 - \frac{\tanh\left(\dfrac{L_{m,m}}{2L_{\mathrm{h}}}\right)}{\dfrac{L_{m,m}}{2L_{\mathrm{h}}}}, \tag{10}$$

where $L_{m,m}$ is the length of the mth interconnect layer, L_{h} is the thermal characteristic length, and $L_{\mathrm{h}} = \left(k_m t_m t_{\mathrm{ins}}/k_{\mathrm{ins}} s\right)^{1/2}$, where s is a correction factor when the heat fringing effect is considered, and is defined as $s = w_{\mathrm{eff}}/w_m$. However, $k^*_{\mathrm{ins},m}$ given in the former part of this paper includes the heat fringing effect, so we let s=1.

Based on the above analysis, the effective heat generation per unit volume of the mth interconnect layer is as follows:

$$\begin{aligned} Q_{\mathrm{eff},m} &= \frac{Q_{\mathrm{g},m} + Q_{\mathrm{in},m} - Q_{\mathrm{out},m}}{w_{m,m} t_{m,m} x_{\mathrm{o}}} \\ &= j^2_{\mathrm{rms},m}\rho_0 + \frac{k^*_{\mathrm{eff},m+1}(T_{m+1}(x) - T_m(x))}{t_{\mathrm{ins},m+1} t_{m,m}} - \frac{k^*_{\mathrm{eff,m}}(T_m(x) - T_{m-1}(x))}{t_{\mathrm{ins},m} t_{m,m}}. \end{aligned} \tag{11}$$

Substituting Eq.(11) into Eq.(2) yields

$$\frac{\partial^2 T_m(x)}{\partial x^2} + \frac{j^2_{\mathrm{rms},m}\rho_0 + \dfrac{k^*_{\mathrm{eff},m+1}(T_{m+1}(x) - T_m(x))}{t_{\mathrm{ins},m+1} t_{m,m}} - \dfrac{k^*_{\mathrm{eff},m}(T_m(x) - T_{m-1}(x))}{t_{\mathrm{ins},m} t_{m,m}}}{k_m} = 0. \tag{12}$$

In order to simplify the computational process, we substitute average temperature T_i for $T_i(x)$, namely, assume that the temperature of each interconnect layer is constant, therefore $\partial^2 T_m(x)/\partial x^2 = 0$, and Eq.(12) can be simplified into

$$a_m T_{m-1} + b_m T_m + c_m T_{m+1} = d_m, \quad (2 \le m \le n-1), \tag{13}$$

where

$$\begin{aligned} a_m &= -t_{\mathrm{ins},m+1} k^*_{\mathrm{eff,m}}, \quad b_m = t_{\mathrm{ins},m+1} k^*_{\mathrm{eff},m} + t_{\mathrm{ins},m} k^*_{\mathrm{eff},m+1}, \\ c_m &= -t_{\mathrm{ins},m} k^*_{\mathrm{eff,m+1}}, \quad d_m = j^2_{\mathrm{rms},m}\rho_0 t_{\mathrm{ins},m} t_{\mathrm{ins},m+1} t_{m,m}, \end{aligned}$$

and n is the number of interconnect layers.

When $m = 1$, Eq.(13) is as follows:

$$b_1 T_1 + c_1 T_2 = d_1 - a_1 T_0, \tag{14}$$

where $a_1 = -t_{\mathrm{ins},2} k^*_{\mathrm{eff},1}$, $b_1 = t_{\mathrm{ins},2} k^*_{\mathrm{eff},1} + t_{\mathrm{ins},1} k^*_{\mathrm{eff},2}$, $c_1 = -t_{\mathrm{ins},1} k^*_{\mathrm{eff},2}$, T_0 is the substrate temperature, and $d_1 = j^2_{\mathrm{rms},1}\rho_0 t_{\mathrm{ins},1} t_{\mathrm{ins},2} t_{m,m}$.

When $m = n$, obviously, $Q_{\mathrm{in},n}$=0, then Eq.(13) is as follows:

$$a_n T_{n-1} + b_n T_n = d_n, \tag{15}$$

where $a_n = -k^*_{\mathrm{eff},n}$, $b_n = k^*_{\mathrm{eff},n}$, and $d_n = j^2_{\mathrm{rms},n} t_{\mathrm{ins},n} t_{m,n}$.

Combining Eqs.(13), (14) and (15) yields

$$\begin{bmatrix} b_1 & c_1 & 0 & 0 & \cdots & 0 & 0 & 0 \\ a_2 & b_2 & c_2 & 0 & \cdots & 0 & 0 & 0 \\ 0 & a_3 & b_3 & c_3 & \cdots & 0 & 0 & 0 \\ 0 & 0 & a_4 & b_4 & \cdots & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \ddots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & b_{n-2} & c_{n-2} & 0 \\ 0 & 0 & 0 & 0 & \cdots & a_{n-1} & b_{n-1} & c_{n-1} \\ 0 & 0 & 0 & 0 & \cdots & 0 & a_n & b_n \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ \vdots \\ T_{n-2} \\ T_{n-1} \\ T_n \end{bmatrix} = \begin{bmatrix} d_1 - a_1 T_0 \\ d_2 \\ d_3 \\ d_4 \\ \vdots \\ d_{n-2} \\ d_{n-1} \\ d_n \end{bmatrix}. \quad (16)$$

Equation (16) is an n-dimensional linear equation, and this matrix has a characteristic: the values of the main three diagonals are not zero, and other places are zero. So long as the substrate temperature T_0, we can easily calculate the temperature of each level through Matlab.

3. Model verification and discussion

For the 65 nm CMOS process, copper (Cu) is the interconnect material, and the interlayer dielectric is a low-k material. Based on the 65 nm CMOS process parameter of BPTM,[13] the electronic resistivity of the copper interconnect line is 2.2 $\mu\Omega$·cm, the limit current density is 1.72×10^6 A/cm^2, the effective dielectric constant of interlayer dielectric is 2.2. Assuming that all interconnect lines are on and the current density reaches its maximum value, the 65 nm CMOS interconnect process parameters are obtained as listed in Table 1.

Table 1. Thermal conductivities and dielectric constants of novel low-k materials.

	n	w_m/μm	t_m/μm	space/μm	$t_{\rm ins}/\mu$m	$k_{\rm ins}$
global	3	0.45	1.20	0.45	0.20	2.2
semi-global	3	0.14	0.35	0.14	0.20	2.2
local	3	0.10	0.20	0.10	0.20	2.2

In recent VLSIs, the vias in local interconnect lines are very crowded. If the via effect is neglected, this must result in a big temperature rise in the local interconnect lines and also cause a big error. In order to explain the importance of the via effect, we suppose a reasonable via separation for the 65 nm CMOS process parameter of BPTM with 9 interconnect layers (1, 5, 15, 30, 50, 100, 250, 500, and 1000 μm, from metal one to metal nine, respectively).

From the analytical thermal model proposed in this paper, we calculate the temperature distribution of multilevel interconnects with and without including the via effect ($\eta = 1$), separately, as shown in Fig.2 on the assumption that the substrate temperature is 0°C ($T_0 = 0$). As can be seen from Fig.2, the temperature reduces obviously when the via effect is included, which implies that it will cause a big error if the via effect is not included; the top layer has the biggest temperature error. Compared with the models in Refs.[4] and [7], the proposed model is closer to the fact. Metal one and metal two have almost no temperature rise, because local interconnect lines have small via separations, that is to say, there is a big via density in local interconnect lines, which is favourable for heat diffusion from a metal to a substrate (the thermal conductivity of the via is much bigger than that of the interlayer dielectric), and it also explains that vias are the main heat diffusion path for local interconnect lines.

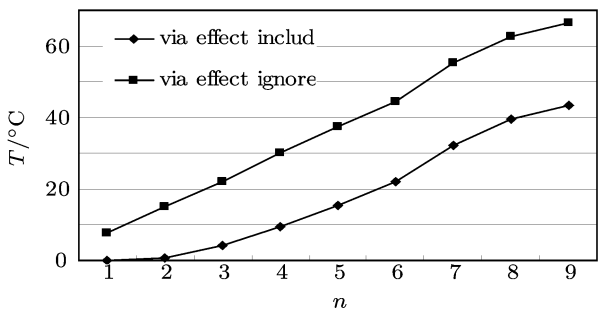


Fig.2. Temperature rise of a multilevel interconnect.

Based on the proposed model, the temperature rise of a multilevel interconnect with different double via separations is shown in Fig.3 on the assumption

that substrate temperature is 0 °C ($T_0 = 0$). As can be seen from Fig.3, almost no temperature rise takes place when there exist double global via separations (1, 5, 15, 30, 50, 100, 500, 1000, and 2000 μm, from metal one to metal nine, respectively), and only a little temperature rise is observed when both global via separations and semi-global via separations (1, 5, 15, 60, 100, 200, 500, 1000, and 2000 μm, from metal one to metal nine, respectively) are doubled; however, there is a big temperature rise when all via separations (2, 10, 30, 60, 100, 200, 500, 1000, and 2000 μm, from metal one to metal nine, respectively) are doubled. As can be seen from Fig.3, local via separation has a great effect on the temperature of the multilevel interconnect and metal two has an obvious temperature rise compared with substrate temperature; this is because when local via separations are doubled, which means a small via density and a reduction of the effective thermal conductivity of the lower interlayer dielectric layer, the heat cannot dissipate effectively for local interconnects. However, the heat generated by both semi-global interconnects and global interconnects can dissipate through the heat sink which is attached to the underlying Si substrate, so it cannot dissipate effectively too. Consequently, this results in a big temperature rise of the multilevel interconnect, and it also explains that local vias have a great effect on the temperature rise of the multilevel interconnect.

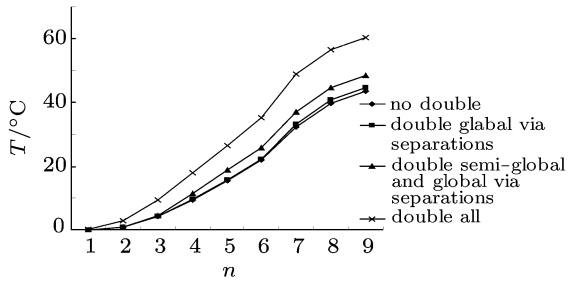


Fig.3. Temperature rise of multilevel interconnect with different double via separations.

Based on the proposed model, the temperature rise of the multilevel interconnect with increasing current density is shown in Fig.4 on the assumption that the substrate temperature is 0 °C ($T_0 = 0$). With increasing current density, temperature rises rapidly, especially for global interconnects when the current density reaches 2.00 mA/cm^2. As shown in formula (3), the joule heat generated by the global interconnect is more than that for the local interconnect with its bigger width and thickness, so the increase of current density has a great effect on the global interconnect. Although the local interconnect generates more joule heat with increasing current density, there is no or only a little temperature rise, because the presence of the via effect results in a high thermal conductivity for the lower interlayer dielectric layer and the effective dissipation of heat.

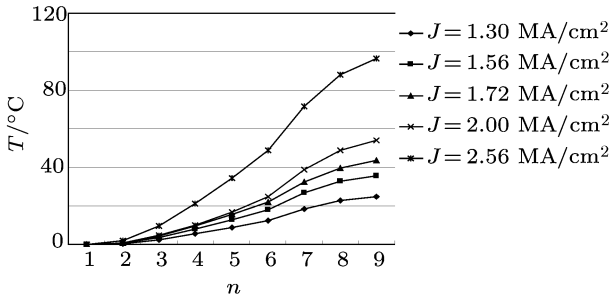


Fig.4. Temperature rise of multilevel interconnect with current density increasing.

Based on the proposed model, the temperature rise of the multilevel interconnect for different values of k is shown in Fig.5 on the assumption that the substrate temperature is 0 °C ($T_0 = 0$). The global interconnect lines have big via separations, which means a small via density, so heat must diffuse through the interlayer dielectric that has a poor thermal conductivity, and temperature rises rapidly as thermal conductivity reduces, which must leads to a great deterioration in the performance of global interconnect lines. However, the local interconnect lines have a big via density, and the thermal conductivity of the via is much bigger than that of the interlayer dielectric, so in spite of using a low-k interlayer dielectric, there is almost no temperature rise compared with the substrate temperature. Consequently, it is important for an interconnect optimization designer to pay great attention to the temperature rise of the global interconnect lines.

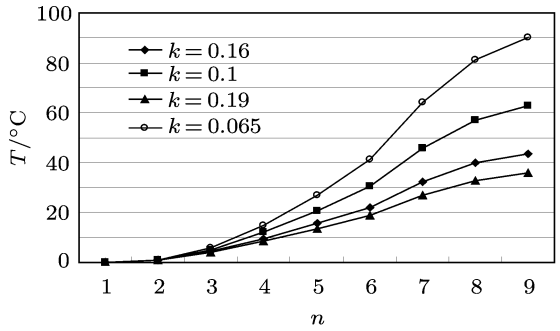


Fig.5. Temperature rise of multilevel interconnect for different values of k.

4. Conclusion

Based on the heat diffusion equation of multilevel interconnects, a novel analytical thermal model for multilevel interconnects considering the via effect is presented, which can compute quickly the temperature of multilevel interconnects, with substrate temperature given. Based on the proposed model and the 65 nm CMOS interconnect process parameter, the computed results shows that the via effect has a great effect on local interconnects, but the reduction of thermal conductivity has little effect on local interconnects. With thermal conductivity reducing or current density increasing, however, the temperature of global interconnects rises greatly, thereby leading to a great deterioration in the performance of global interconnects. The model proposed in this paper can be used to make an accurate estimation for interconnects, or a period estimation for high-performance chip design considering the effect of interconnect temperature.

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