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Physical simulations and experimental results of 4H–SiC MESFETs on high purity semi-insulating substrates

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In this paper we report on DC and RF simulations and experimental results of 4H–SiC metal semiconductor field effect transistors (MESFETs) on high purity semi-insulating substrates. DC and small-signal measurements are compared with simulations. We design our device process to fabricate n-channel 4H–SiC MESFETs with 100 μm gate periphery. At 30 V drain voltage, the maximum current density is 440 mA/mm and the maximum transconductance is 33 mS/mm. For the continuous wave (CW) at a frequency of 2 GHz, the maximum output power density is measured to be 6.6 W/mm, with a gain of 12 dB and power-added efficiency of 33.7%. The cut-off frequency ($f_{\rm T}$) and the maximum frequency ($f_{\rm max}$) are 9 GHz and 24.9 GHz respectively. The simulation results of $f_{\rm T}$ and $f_{\rm max}$ are 11.4 GHz and 38.6 GHz respectively.

Keywords: 4H–SiC, MESFET, simulation, microwave
PACC: 7340S, 7280E

1. Introduction

SiC is physically hard, chemically stable, and resistant to radiation damage. The unique material properties of SiC are favourable for broadband and microwave power applications.[1] Johnson's Figure of Merit (JMF) addresses the potential of a material for high frequency and high-power applications:

$$\mathrm{JMF} = \frac{E_{\rm B}^2 v_{\rm s}^2}{4\pi^2} ,$$

where $E_{\rm B}$ is the breakdown electric field and $v_{\rm s}$ is the electron saturation speed. In terms of this figure of merit, SiC is 260 times better than Si.

The microwave power performance of the fabricated SiC MESFETs was excellent with an output power density of 7.7 W/mm at 3 GHz and a PAE of 70% in class AB.[2] SiC MESFETs fabricated from 4H–SiC can produce an almost ideal power-added efficiency and an RF output on the order of 8 W/mm, which is a factor of seven greater than that obtainable from GaAs devices. Numerous simulation studies have been done on SiC MESFETs. The ultimate purpose of physical-based simulations, commonly referred to as Sivalco, is to reduce the time-consuming and the number of expensive clean-room experiments. Many simulation results are in good agreement with the published experimental data. For example, a thermal model of 4H–SiC MESFET is developed based on the temperature dependences of material parameters and three-region I–V model. Significant improvement on device electrical and thermal characteristics is observed for thinner and lightly doped substrate.[3] A 4H–SiC MESFET large signal drain current model based on physical expressions has been developed, which is to be used in CAD tools. The verification of the present model embedded in CAD tools is made, which shows that it accords with measurements of large signal DC I–V characteristics, PAE (power added efficiency), output power and gain.[4]

In the present article, we report on DC and S parameter simulations and experimental results of 100 μm total gate periphery 4H–SiC MESFET. First, the SiC wafer structure with three layers used for SiC MESFET and the SiC MESFET horizontal structure are designed. Then, the simulation results are obtained by using the designed structure and material parameters. The performance of SiC MESFETs fabricated on a designed material structure has been measured. A good correspondence between physical simulations and experimental characteristics is obtained.

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The simulations results of the p-type buffer layers with different doping concentrations in SiC MESFET characteristics are used to chart a new direction for the SiC devices. The fabrication process is also described in detail.

2. Experiment

The 8° off-angled 4H–SiC high-purity semi-insulating substrates with three epitaxial layers grown by CETC 55 were used for this study. The n-type dopant was nitrogen and the p-type dopant was aluminum. The SiC MESFET structures consisted of a 0.6-μm thick p-type buffer layer doped to $5\times10^{15}/\mathrm{cm}^3$, a 0.35-$\mu$m thick n-type channel layer doped to $3\times10^{17}/\mathrm{cm}^3$, and a 0.15-$\mu$m thick n^+ contact layer doped to $1\times10^{19}/\mathrm{cm}^3$. The single and total gate periphery was 100 μm. The gate-length was 0.6 μm, the gate-source and the gate-drain separations were 0.6 μm and 1.6 μm respectively.

The processes began with the standard RCA cleaning. After the formation of the mark, we lithographed and etched SiC wafer down to the n-type channel and then formed the device isolation by using the B^+ implantation. A 2.8-μm wide channel recess was fabricated by etching the n^+ and part of the active layers again by using inductively coupled plasma (ICP). Ni determined by lift-off and annealed by using a rapid thermal process at 1000 °C for 5 min in N_2 was used to form the Ohmic contacts.[5] Transmission line model (TLM) pattern fabricated on the same wafer confirmed that a specific contact resistivity of $1.0\text{–}2.0\times10^{-6}\ \Omega\cdot\mathrm{cm}^2$ was obtained.[6] A 200-nm thick $\mathrm{Si}_x\mathrm{N}_y$ layer was deposited by PECVD as a field plate dielectric. The channel thickness under the gate (of the component) was about 0.2 μm. Γ-shape gate with 0.6 μm footprint was patterned by Advanced Semiconductor Material Lithography (ASML) stepper –50. The gate contact was composed of a multilayer metal structure of Ti/Pt/Au (50/50/450 nm).[7] The thick metallization of Γ-shape gate resulted in a low gate resistance. The surface passivation was important for realizing an optimum power performance. A plasma enhanced chemical vapour deposition (PECVD) system using SiH_4 and NH_3 sources was used to deposit 200 nm $\mathrm{Si}_x\mathrm{N}_y$ on the device wafers as passivation dielectric at a base plate temperature of 280 °C. The metal layers (Ti/Au = 50/100 nm) for interconnections were deposited by sputtering. The final devices were diced, packaged and bonded for DC and RF testing.

3. Simulations

Accurate physical models of material properties are a prerequisite for device simulation. Published material data were utilised to derive physical models by adjusting model parameters to obtain the closest possible agreement with experimental data.[8]

The details of the 4H–SiC material parameter and device dimension used in the simulations are shown in Table 1.

Table 1. Parameters and dimensions used in simulation.

q	1.6×10^{-19}	$V_{\mathrm{bi},0}$	1.3 eV
ε_{s}	8.85×10^{-14}	N_{D}	$3.1\times10^{17}/\mathrm{cm}^3$
ε_{r}	9.7	N_{A}	$5\times10^{15}/\mathrm{cm}^3$
μ_0	300 $\mathrm{cm}^2/\mathrm{v}\cdot\mathrm{s}$	L_{sg}	0.6 μm
v_{s}	$2.0\times10^7\mathrm{cm/s}$	L_{g}	0.6 μm
β	1	L_{gd}	1.6 μm
$V_{\mathrm{bi,SiC}}$	1.0 eV	E_{trap}	0 eV
τ_{n}	1×10^7 s	τ_p	1×10^7 s
$\mu_{\mathrm{n,min}}$	88 $\mathrm{cm}^2/\mathrm{v}\cdot\mathrm{s}$	$\mu_{\mathrm{n,max}}$	900 $\mathrm{cm}^2/\mathrm{v}\cdot\mathrm{s}$

The velocity-field characteristics of SiC are similar to those of Si rather than GaAs in that SiC does not have velocity overshoot behaviour. The velocity of SiC is not linearly proportional to the electric field and described by a field-dependent mobility model

$$\mu_{\mathrm{E}} = \frac{\mu_0}{\left[1+\left(\dfrac{\mu_0 E}{v_{\mathrm{sat}}}\right)^{\beta}\right]^{1/\beta}},$$

where μ_0 is the low field mobility, E is the electric field, v_{sat} is the saturation velocity, and β is a fitting parameter.

Two-dimensional device models have been commonly used to analyse the characteristics of MESFETs. In GaAs-like two-dimensional models for SiC MESFETs only the intrinsic region under the gate but not the parasitic source and drain regions are considered. It is well known that the depletion region at the edge of the gate extends toward the drain side as the drain voltage increases. This extension becomes considerable in SiC metal-semiconductor-field-effect-transistors (MESFETs) which operate at high drain voltages. Surface depletion depth (d_{s}) is also taken in

account in this model

$$d_{\mathrm{s}} = \sqrt{\frac{2\varepsilon_{\mathrm{s}} V_{\mathrm{bi,SiC}}}{qN_{\mathrm{D}}}},$$

where ε_{s}, $V_{\mathrm{bi,SiC}}$, and N_{D} are the dielectric constant, built-in voltage, and channel doping concentration of SiC, respectively.

It is assumed that the doping concentration is uniform across the channel region. The L_{ext} is a function of voltage difference at the gate edge and can be expressed as

$$L_{\mathrm{ext}} = \sqrt{\frac{2\varepsilon_{\mathrm{s}}(V_{\mathrm{bi,Schottky}} - V_{\mathrm{gs}} + V'_{\mathrm{ds}})}{qN_{\mathrm{D}}}},$$

where L_{ext} is the extension of the depletion region toward the drain side, $V_{\mathrm{bi,Schottky}}$ is the barrier height of the Schottky contact, V_{gs} is the gate bias, and V'_{ds} is the voltage at the drain depletion edge.

The effect of the recombination centres can be described by the conventional Shockley–Read–Hall (SRH) recombination/generation expression

$$R = \frac{pn - n_i^2}{\tau_p \left[n + n_i \exp\left(\frac{E_{\mathrm{trap}}}{kT}\right)\right] + \tau_n \left[p + n_i \exp\left(\frac{-E_{\mathrm{trap}}}{kT}\right)\right]},$$

where E_{trap} is the difference in energy between the trap energy level and the intrinsic Fermi level.

4. Results and discussion

Pulsed I–V measurement was carried out by using a micromanipulator system to determine the actual influence of self-heating on the DC characteristics of the SiC MESFET. The SiC MESFET was located in a load–pull system for CW 2 GHz microwave power measurement. Numerical simulations were performed by using a commercial program: Atlas from Sivalco.

From Fig.1, we know that the current density of SiC MESFET is 440 mA/mm (of drain current) at a drain voltage of 30 V. The threshold voltage is –18 V. The maximum transconductance (Gm) is 33 mS/mm at a drain voltage of 30 V and a gate voltage of 0 V. An on-state breakdown voltage of V_{ds} = 150 V is measured. Figure 1 shows that the simulated output current is higher than the measured value for high values of V_{ds}. The difference between simulated and measured results can be explained by the trapping of electrons at the surface as well as in the substrate. Electrons injected from the gate and the channel region are trapped at the surface as well as in the interface/substrate region. As a result, the channel area narrows compared to the initial condition so that the drain current becomes lower. It is suggested that the good channel recess etching and the surface passivation can suppress the surface trapping effects, resulting in the enhancement of the drain current.

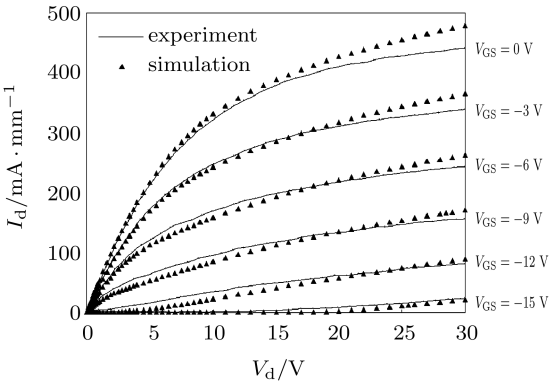


Fig.1. Comparison between experimental and simulated pulsed DC results of a 0.6-μm gate 4H–SiC MESFET.

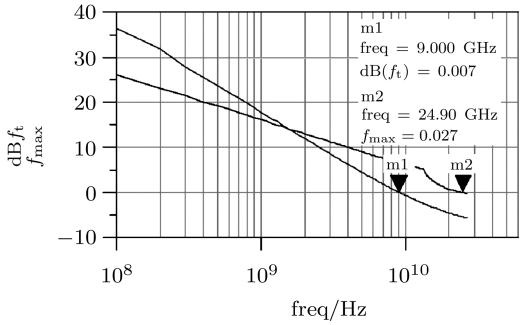


Fig.2. f_{T} and f_{max} extracted from the measured small signal S-parameters.

The cut-off frequency f_{T} of 9 GHz and the maximum frequency f_{max} of 24.9 GHz extracted from the measured small signal S-parameters were shown in Fig.2.

The measured gain, $P_{\rm out}$, and power added efficiency (PAE) at 2 GHz are shown in Fig.3. At a drain voltage of 75 V, the load–pull measurements show a cw output power of 28.2 dBm for 100 μm devices, at the same time, the gain is 12 dB and the PAE is 33.7%. The maximum power density is 6.6 W/mm. According to the pulsed DC characteristics, we believe that the output power density is thermally limited and that an active cooling or a lower thermal resistance is likely to increase even more the output power density of these devices.

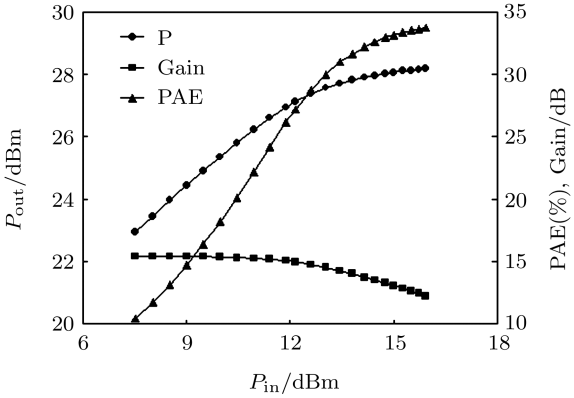


Fig.3. RF power performance of 100-μm gate width 4H–SiC MESFET at 2 GHz.

Computational simulations using two different doping concentration p-type buffer layer were performed to investigate the effects of p-type buffer. According to the comparison among p-type buffer layers with different doping concentrations shown in Fig.4, it is concluded that the high-doped buffer layer also requires a thicker channel layer, as the channel is depleted from the buffer as well.[9] in addition, figure 4 indicates that the higher doping of buffer yields the lower $V_{\rm p}$ and $I_{\rm ds}$. It is known that the effect of doping on the performance of device is larger than that of thickness.[10]

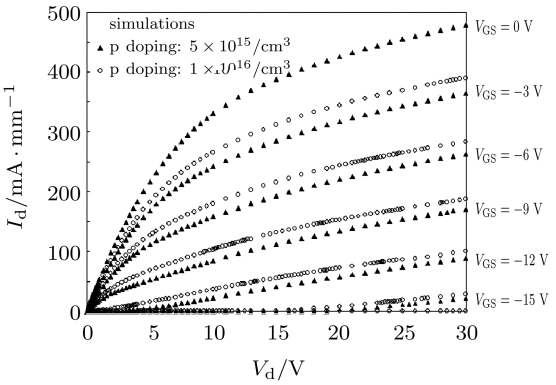
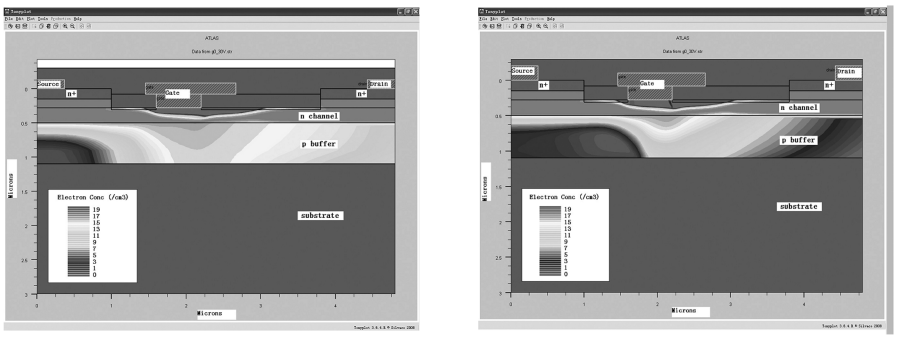


Fig.4. Simulated DC characteristics of a 0.6-μm gate 4H–SiC MESFET with p-type buffer layer for two different doping concentrations.

Figure 5 shows the structure determined in the simulation according to the fabricated SiC MESFET. Figures 5(a) and 5(b) show the electron concentrations distribution in channel and p-type buffer layers for p-type doping 5×10^{15}/cm^3 and 1×10^{16}/cm^3 respectively.

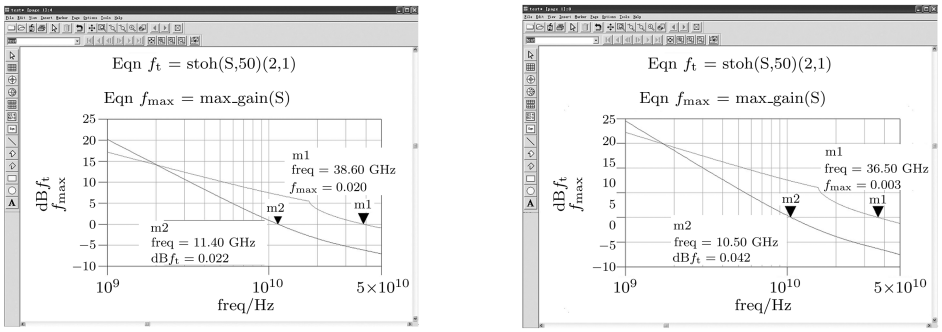


(a) (b)

Fig.5. Comparison of electron concentration distribution between p-type buffer layers with two different doping concentrations: 5×10^{15}/cm^3 (a) and 1×10^{16}/cm^3 (b).

Figure 6 shows $f_{\rm T}$ and $f_{\rm max}$ derived from the simulated S-parameters. The bias conditions for both simulation and measurements are $V_{\rm gs} = -8$ V and $V_{\rm ds} = 30$ V. In Figs.6(a) and 6(b), only p-type buffer layer doping is changed from 5×10^{15}/cm^3 to 1×10^{16}/cm^3. It is known that the higher doping of p-type buffer layer has negative influence on $f_{\rm T}$. The $f_{\rm T}$ and the $f_{\rm max}$ derived from the measured S-parameters are shown

in Fig.2 and the f_{T} and the $f_{\max}$ derived from the simulated S-parameters are shown in Fig.5(a). In addition to insufficient frequency sweeping at a low drain bias, the self-heating effects of devices result in relatively poor frequency performances due to the deterioration of current–voltage characteristics.



(a) (b)

Fig.6. f_{T} and $f_{\max}$ extracted from the simulated small signal S-parameters between p-type buffer layers with two different doping concentrations: $5\times10^{15}/\mathrm{cm}^3$ (a) and $1\times10^{16}/\mathrm{cm}^3$ (b).

5. Conclusion

We simulate and fabricate high-performance SiC MESFETs on high-purity semi-insulating 4H–SiC substrates. The SiC MESFETs are designed and fabricated according to the simulations. A good correspondence between physical simulations and experimental characteristics is obtained. By employing a channel recess technique, excellent characteristics are obtained. On-state breakdown voltage ranges from 100 V to over 150 V, depending on device structure. At 2 GHz cw, the RF power density is 6.6 W/mm, at the same time, the gain is 12 dB and the PAE is 33.7%. The cut-off frequency (f_{T}) and the maximum frequency ($f_{\max}$) extracted from measured small signal S-parameters are 9 GHz and 24.9 GHz respectively. The f_{T} and $f_{\max}$ extracted from simulated small signal S-parameters are 11.4 GHz and 38.6 GHz respectively. The simulations of different p-buffer layer parameters point out the change of the characteristics of SiC MESFETs.

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