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Formation of the intermediate semiconductor layer for the Ohmic contact to silicon carbide using Germanium implantation*

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By formation of an intermediate semiconductor layer (ISL) with a narrow band gap at the metallic contact/SiC interface, this paper realises a new method to fabricate the low-resistance Ohmic contacts for SiC. An array of transfer length method (TLM) test patterns is formed on N-wells created by P^+ ion implantation into Si-faced p-type 4H-SiC epilayer. The ISL of nickel-metal Ohmic contacts to n-type 4H-SiC could be formed by using Germanium ion implantation into SiC. The specific contact resistance ρ_c as low as 4.23×10^{-5} $\Omega\cdot cm^2$ is achieved after annealing in N_2 at 800 °C for 3 min, which is much lower than that (> 900 °C) in the typical SiC metallisation process. The sheet resistance R_{sh} of the implanted layers is 1.5 kΩ/□. The technique for converting photoresist into nanocrystalline graphite is used to protect the SiC surface in the annealing after Ge^+ ion implantations.

Keywords: SiC, Ohmic contact, Ge ion implantation, intermediate semiconductor layer
PACC: 7340C, 6170T

1. Introduction

Silicon carbide (SiC) with wide energy bandgap about 3 eV is an attractive semiconductor material. Its high critical field strength and good thermal conductivity makes SiC become an excellent candidate for the development of superior high power, high-temperature and high-frequency devices.[1−3] To utilize the excellent properties of SiC in an electronic device, thermodynamically stable Ohmic contacts with low specific contact resistance are important, since parasitic resistances generally limit or even jeopardise device operation.[2]

One of the best ways to fabricate the low-resistance Ohmic contacts for SiC is to increase the carrier density in the SiC substrates, which increases the tunneling current density through the barrier by reducing the depletion layer width. So the ion-implantation method is used to increase the carrier density.[3] An alternative method is to form an intermediate semiconductor layer (ISL) with a narrow band gap at the metallic contact/SiC interface,[4] which is mostly a deposition and annealing technique (deposit the contact metals on SiC and anneal).

In this paper a completely different way is studied to fabricate the ISL with a narrow band gap by using Germanium ion implantation. Furthermore, we discuss the mechanism of the low-resistance Ohmic contacts for SiC based ISL, which is very important to realise a new process to reduce the resistance of contacts to SiC.

2. Mechanism of ISL using SiC:Ge

The energy band diagram of a metal/interlayer/substrate structure for the case of an n-type SiC substrate is illustrated in Fig.1. From the alignment of the Fermi levels, two potential barriers form at the two interfaces, which are: (i) the Schottky barrier between the metal and the interlayer; (ii) the barrier between the interlayer and the substrate.[5]

The SiC combined with a few atomic percent of

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Ge (designated as SiC:Ge) is under investigation as a new material for SiC-device applications. The incorporation of Ge into a SiC:Ge alloy can lower the band gap of the material and there have been demonstrations of diode rectifiers and bipolar transistors using SiC:Ge.[6,7] Furthermore, as an alloy, the heterointerface between SiC:Ge and SiC could exhibit some degree of compositional grading, which will reduce or eliminate any band-edge discontinuities. So the ISL with a narrow band gap could be formed by using Germanium ion implantation into SiC, which is SiC:Ge.

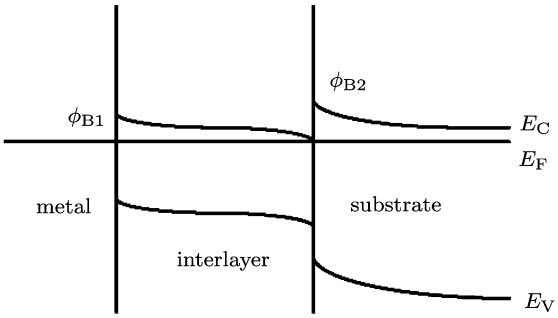


Fig.1. The energy band diagram of a metal /interlayer / substrate structure.

3. Experiment and results

The 4H-SiC wafer used in this experiment is purchased from Cree Research Company. Orientation of the substrate is 8° off-axis ⟨1000⟩ direction. The patterns are made on a p-type epitaxial layer with concentration of $N_a = 7.4\times10^{16}$ cm^{-3} and depth of 5 μm based on the n-type silicon faced substrate. N-wells are formed by P^+ ions implantation into epilayer at 550 °C. The energy and dose for ion implantation are 150 keV, 100 keV and 2.5×10^{15} cm^{-2}, 8.3×10^{14} cm^{-2} respectively. The phosphorus ion concentration for implantation is 1×10^{20} cm^{-3} and then the SiC:Ge layer is formed by Ge^+ ions implantation into SiC at 550 °C. The energies and doses for ion implantation are 300 keV, 183 keV, 107 keV, 50 keV and 7.63×10^{15} cm^{-2}, 2.66×10^{15} cm^{-2}, 2.01×10^{15} cm^{-2}, 1.66×10^{15} cm^{-2} respectively. The Ge ion concentration for implantation is about 10^{21} cm^{-3}. For comparison, the molecular density of SiC is 4.8×10^{22} atom pairs/cm^3, the data suggest that the incorporation of Ge into a SiC:Ge alloy lowers the band gap by as much as 100 meV.[6]

Post-implantation annealing is done at 1700 °C in vacuum for 30 min, using the crucible coated by poly-SiC. In order to suppress SiC surface roughening and dopant out-diffusion, a nanocrystalline graphite capping layer is used to protect the surface of SiC during post-implantation annealing. After ion implantation, the samples of all photoresists are cleaned and a layer of BN310 photoresist is spin-coated on the SiC wafer and heat treated in a conventional furnace to form a capping layer. This film is removed by oxidizing in O_2 for 15 min at 950 °C after the annealing.

The samples are cleaned in acetone before the metal deposition followed by a standard RCA cleaning process. And after HF treatment, titanium (3 nm, especially to improve adhesion), nickel (200 nm) have been deposited in sequence on the surface of SiC wafer. The Ohmic contacts are patterned through conventional photolithography and lift-off techniques. Finally, High temperature annealing is performed in N_2 for 3 min at 800 °C.

The scanning electron microscopy (SEM) image of the TLM (transfer length method) pattern used in this study is shown in Fig.2. Figure 3 shows the variation in total resistance R_T between adjacent TLM pads with gap spacing L. The lowest value of the specific contact resistances is 4.23×10^{-5} Ω·cm^2. Furthermore, sheet resistance R_{sh} is W multiplied by the slope dR_T/dL of the linear curve shown in Fig.3. The value for sheet resistance R_{sh} of the implanted layer is about 1.5 kΩ/□.

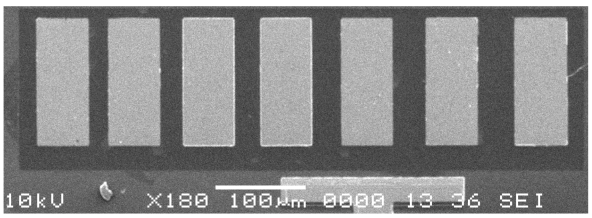


Fig.2. The SEM image of TLM structure.

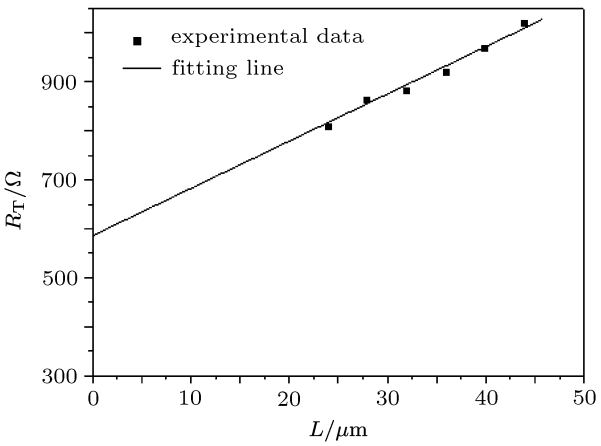


Fig.3. The TLM total resistance versus gap spacing of the contacts.

4. Discussion

The lowest value of the specific contact resistances in this research, 4.23×10^{-5} $\Omega\cdot cm^2$, is a normal result for Ni based Ohmic contacts to n-type 4H–SiC. However, the annealing temperature (800 °C) is much lower than that (> 900 °C) in the typical SiC metallization process. Generally speaking, in the formation of Ohmic contact using Ni layer on n-type SiC, it is required to anneal the contact formed on highly doped SiC substrate at high temperatures (950–1000 °C).[8,9]

The lower annealing temperature can prove that the ISL using SiC:Ge is very useful to make the formation of Ohmic contacts to SiC easier. The mechanism of ISL and the energy band model are significant and throw some new light on the formation of Ohmic contacts on SiC, which is a hard nut to crack.

The value for sheet resistance R_{sh} of the implanted layer is high in comparison with our early results.[3] The high value is perhaps induced by the implantation of Ge^+ ion, which causes more damage to decrease the carrier mobility of the implanted layer because of the large atom size and several times implantation.

Ion implantation is the only practical way of achieving selective doping of silicon carbide, and post-implantation annealing at temperatures between 1400 °C and 1700 °C is necessary to repair the damage to the crystal lattice and incorporate the dopant at electrically active lattice sites. However then, the high-temperature annealing induces the macrostep formation on the surface of the implanted SiC. Another undesirable effect of high-temperature post-implantation annealing is an out-diffusion of some implanted dopants.[10] In this paper, the technique for converting photoresist into nanocrystalline graphite is used to protect the SiC surface in the annealing after Ge^+ ion implantations.

The SEM image of the wafer surface with graphite capping layer is shown in Fig.4, which is uniform and smooth. The x-ray energy-dispersive spectrometer (XEDS) spectrum is obtained from the wafer surface (Fig.5). The atom percentage of C is 80.88% at the surface of the wafer, which proves that there is a graphite film on the SiC.

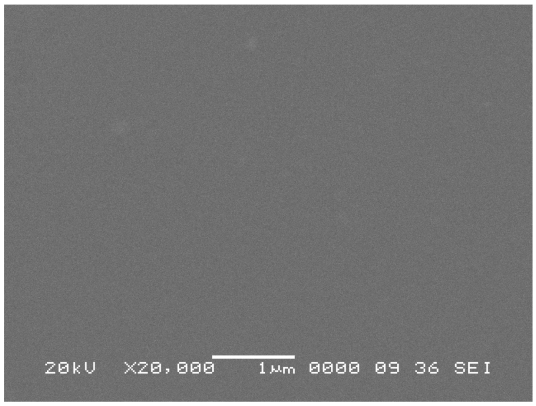


Fig.4. SEM image of the wafer surface with a graphite layer.

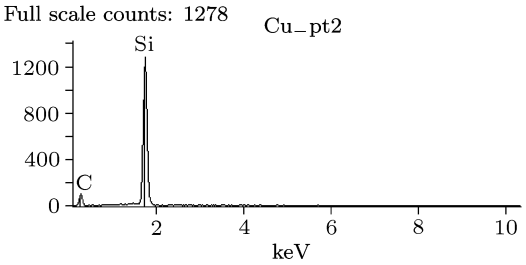


Fig.5. The XEDS spectrum of the wafer surface.

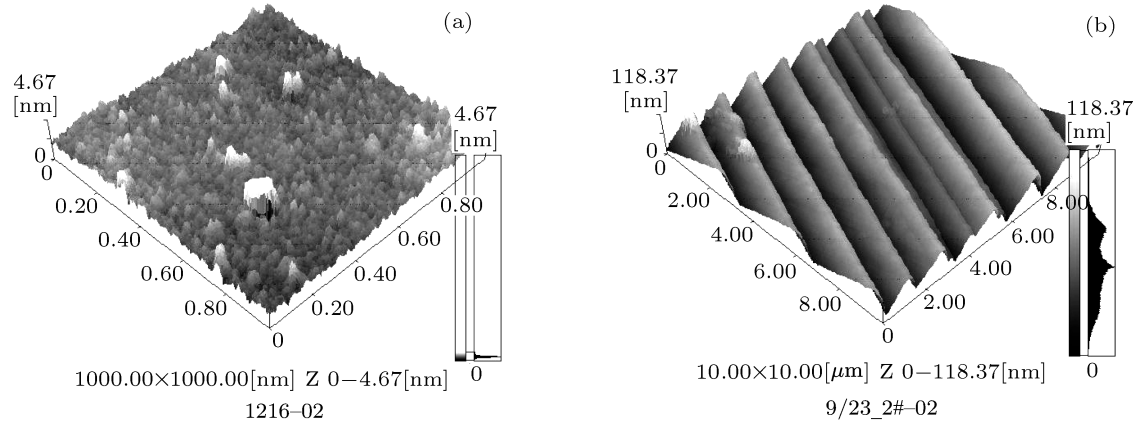


Fig.6. The surface of wafer after post-implantation annealing. (a) The surface of wafer with a graphite cap; (b) the surface of wafer without any protective graphite cap.

The atom force microscope (AFM) micrographs of SiC samples annealed, after removal of the capping layer (Fig.6(a)) and without any protective cap (Fig.6(b)), are compared. On the sample surface without any protective cap, macro-steps are obvious, which are commonly observed. The protected surface, on the other hand, is planar with a roughness of about 0.7 nm root mean square (RMS), measured by AFM scan in the 10 μm×10 μm area. This value is larger than that of a virgin epitaxial wafer (about 0.12 nm) but is good enough.

5. Conclusion

The Ge^+ ion implantation method is used to form an ISL with a narrow band gap at the metallic contact/SiC interface. The mechanism of the low-resistance Ohmic contacts for SiC based ISL is discussed, which is essential to realise a new process to reduce the resistance of contacts to SiC. The lowest value of the specific contact resistances, 4.23×10^{-5} $\Omega\cdot cm^2$, is a normal result for Ni based Ohmic contacts to n-type 4H–SiC. The lower annealing temperature can prove that the ISL using SiC:Ge is very useful to make the formation of Ohmic contacts to SiC easier.

The technique for converting photoresist into nanocrystalline graphite is used to protect the SiC surface in the annealing after Ge^+ ion implantations. The protected surface is planar with a roughness of about 0.7 nm RMS, measured by AFM scan in the 10 μm×10 μm area. This value is larger than that of a virgin epitaxial wafer (about 0.12 nm) but is good enough.

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