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The modulation of Schottky barrier height of NiSi/n-Si Schottky diodes by silicide as diffusion source technique*

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This paper reports that the Schottky barrier height modulation of NiSi/n-Si is experimentally investigated by adopting a novel silicide-as-diffusion-source technique, which avoids the damage to the NiSi/Si interface induced from the conventional dopant segregation method. In addition, the impact of post-BF_2 implantation after silicidation on the surface morphology of Ni silicides is also illustrated. The thermal stability of Ni silicides can be improved by silicide-as-diffusion-source technique. Besides, the electron Schottky barrier height is successfully modulated by 0.11 eV at a boron dose of 10^{15} cm^{-2} in comparison with the non-implanted samples. The change of barrier height is not attributed to the phase change of silicide films but due to the boron pile-up at the interface of NiSi and Si substrate which causes the upward bending of conducting band. The results demonstrate the feasibility of novel silicide-as-diffusion-source technique for the fabrication of Schottky source/drain Si MOS devices.

Keywords: Schottky barrier height, silicide-as-diffusion source, Ni silicide
PACC: 7330, 7340E, 8115N

1. Introduction

With the aggressive scaling down of the feature size of MOSFET, Schottky barrier source/drain structure has been considered as one of the most promising candidates for deca-nano scale regime to overcome the scaling limit of conventional MOSFETs.[1−5] Theoretical studies have demonstrated that an extremely low Schottky barrier height (Φ_b) is needed for SB-MOSFETs to outperform the conventional MOSFETs with p–n junctions of heavily doped S/D.[6] Various solutions have been proposed to reduce the Schottky barrier height for electron and hole, respectively, such as complementary silicides using $ErSi_x$/$YbSi_x$ for NMOS and PtSi for PMOS,[3,7,8] inserting a thin insulating layer between metal and Si,[9] using Se and S to passivate the surface states of Si.[10,11] These solutions will complicate the fabrication process and the modification of device processing is not recommended. The reliability and reproductivity are also key issues for mass production and surface-state passivation has only been shown to lead to a reduced Φ_b for electron. Furthermore, no single silicide can meet the low Φ_b requirement for both conduction carriers.[3,12] Recently, dopant segregation (DS) technique has attracted much more attention due to its compatibility with standard CMOS process and demonstrated its feasibility to effectively reduce the SB height to both electrons and holes without the use of exotic materials.[13−15] However, the traditional DS technique, that is dopant implantation before silicidation, will induce the damage to the semiconductor surface and in turn degrade the characteristics of Schottky diodes. So a novel SADS (Silicide As Diffusion Source) method is proposed to solve this problem in this paper, which is rarely reported. The modulation of Schottky barrier height is experimentally demonstrated. Besides, the thermal stability of nickel silicides has been a concern for device fabrication.[16] It is first observed that the surface morphology of nickel silicides can be greatly improved by adopting SADS technique.

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2. Fabrication process and experiments

Figure 1 shows the main process flow of novel SADS NiSi/n-Si diode fabrication. A 3000 Å (1 Å=0.1 nm) thick SiO_2 isolation layer is deposited by plasma enhanced CVD on lightly doped n-type Si (100) substrates. Lithographic process and reactive ion etching (RIE) are used to define the contact pattern. A 350-Å thick nickel layer is deposited, followed by rapid thermal annealing (RTA) performed at 600 °C for 60 s in N_2 ambient. Unreacted nickel is selectively etched using a diluted HF solution. Then, BF_2^+ ions with 33 keV are implanted at a dose of 5×10^{13}, 10^{14} and 10^{15} cm^{-2}, respectively, followed by drive-in annealing at 650 °C for 10 s in N_2 ambient. In addition, the controlled sample without BF_2 implantation is also fabricated for comparison.

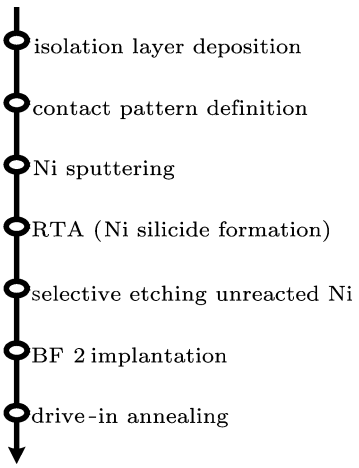


Fig.1. The main process flow of novel SADS NiSi/Si diode fabrication.

The current-voltage curves of NiSi/Si Schottky diodes are measured at room temperature using the HP 4156 semiconductor parameter analyzer. Micro-Raman spectroscopy is used to determine the phase and composition of the doped nickel silicides. Secondary ion mass spectroscopy (SIMS) is adopted to illustrate the depth profile of boron dopant. Scanning electron microscope (SEM) is carried out to study the morphology of the films.

3. Results and discussion

First, we investigate the impact of BF_2 post-implantation after silicidation on the surface morphology of nickel silicides. The thermal stability of NiSi films has been a concern for the device fabrication. Figure 2 illustrates the SEM images of nickel silicides formed without/with BF_2 post-implantation after silicidation at different doses. From Fig.2, the surface of the films is rather rough for the samples without ion implantation after silicidation, while the surface morphology of the films is greatly improved and no agglomeration is observed in the case with BF_2 implantation. It is probably due to fluorine which can retard nickel silicide film's agglomeration.[17] The result indicates that this SADS technique can improve the stability of nickel silicides films and is favorable for the fabrication of Schottky source/drain MOS devices.

Figure 3 demonstrates the current-voltage curves of NiSi/Si Schottky diodes as a function of implantation dose. The reverse current decreases with the increase of boron dose, approximately two orders of magnitude lower at a dose of 10^{15} cm^{-2} in comparison with the sample without BF_2 implantation, which indicates the increase in Φ_{bn}. Using thermionic emission model for the forward bias I–V characteristics, the current equation can be written as

$$I = AA * T^2 \exp\left(\frac{-q\Phi_b}{kT}\right) \cdot \exp\left(\frac{q(V-IR)}{nkT} - 1\right),$$

where A is the diode area, A^* the effective Richardson constant (approximately 112 A/cm^2K^2 for n-Si), T the temperature in Kelvin, k the Boltzmann constant, Φ_b the Schottky barrier height, n the ideality factor, and R the series resistance. The Φ_{bn} is extracted from the I–V curves according to Cheung's method.[18] Figure 4 shows the implanted boron dose dependence of the extracted Schottky barrier height (Φ_{bn}) and the modulation of Schottky barrier height ($\Delta\Phi_{bn}$) of the Ni silicide/n-Si diodes. The circle and triangle symbols stand for Φ_{bn} and $\Delta\Phi_{bn}$, respectively. The Φ_{bn} is 0.66 eV for the samples without BF_2 implantation. With the increase of dose, the Φ_{bn} increases to 0.77 eV at the dose of 10^{15} cm^{-2}. The modulation of Schottky barrier height is successfully realised by SADS technique. The $\Delta\Phi_b$ can reach to ~0.11 eV in comparison with the undoped sample and shows strong dependence on implantation dose. The successful modulation of Φ_{bn} demonstrates the feasibility of SADS technique in NiSi/Si Schottky diodes and Schottky source/drain devices. The modulated value can be further improved by optimizing the process conditions. Besides the dose, the post annealing condition after implantation is also a key factor. The annealing temperature and time are fixed in this paper. Further optimization is under investigation and better results can be expected.

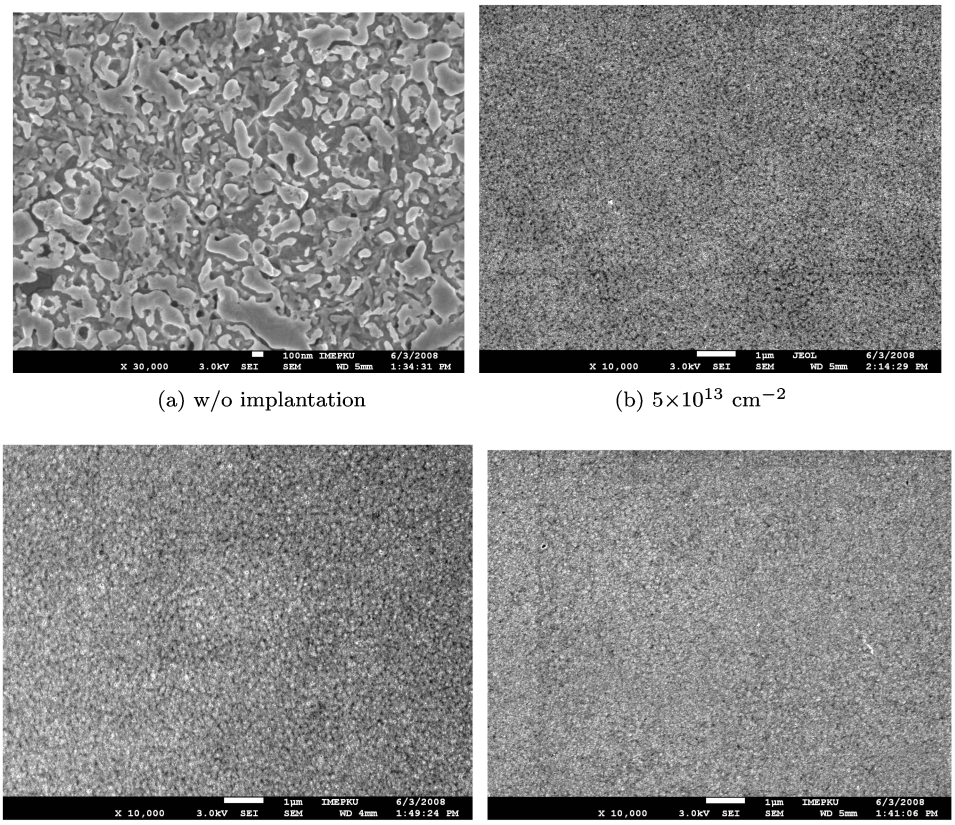


Fig.2. The SEM images of nickel silicides with/without (w/o) BF_2 post-implantation (a) and with BF_2 implantation at different doses ((b), (c), (d)).

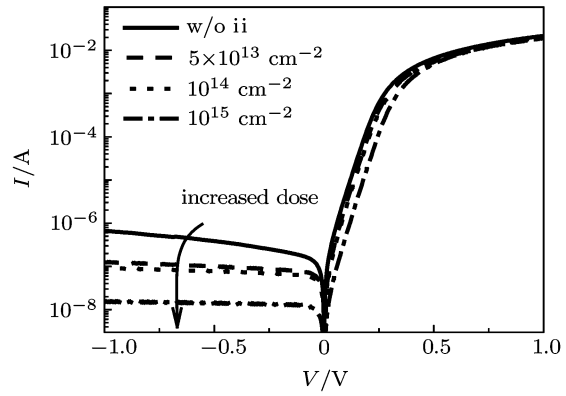


Fig.3. The I–V characteristics of NiSi/n-Si Schottky diodes fabricated by SADS technique as a function of BF_2 implantation dose. The area is 450×450 μm^2.

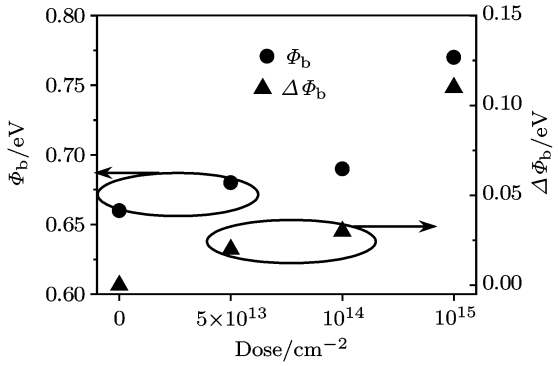


Fig.4. The Φ_b and $\Delta\Phi_b$ of NiSi/n-Si Schottky diodes as a function of implantation dose. The circle and triangle symbols stand for the extracted Φ_{bn} and $\Delta\Phi_{bn}$, respectively.

Micro-Raman spectroscopy was performed to determine the material phase, which is a very powerful technique for phase identification. Figure 5 demonstrates the Raman spectra of the samples with and without BF_2 implantation. For all the samples, two major peaks at 195 cm^{-1} and 215 cm^{-1} are observed, with minor peaks at 255, 293, and 364 cm^{-1}. It is well known that the peaks at 195 and 215 cm^{-1} are the typical Raman peaks corresponding to NiSi phase, and the other three minor peaks are also attributed to

NiSi.[19,20] The Raman results suggest that no phase change occurs for all the analyzed samples. Thus, the possible impact of phase change on the change of SBH is excluded.

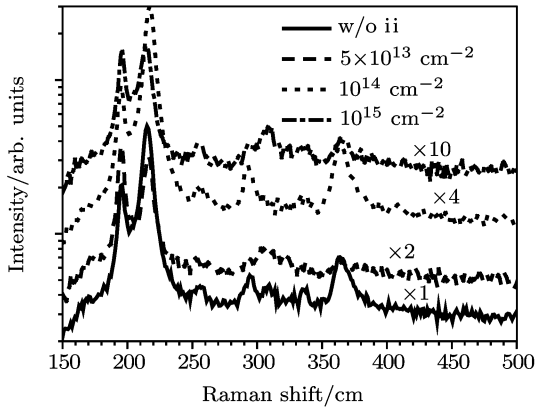


Fig.5. Raman spectra of nickel silicides with/without (w/o) BF_2 implantation after silicidation at different doses.

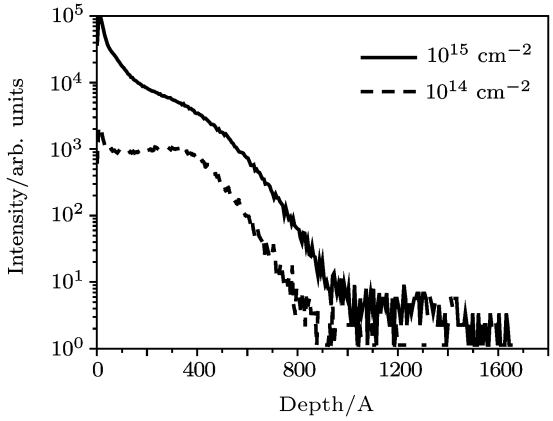


Fig.6. The depth distribution of boron in the samples with different implantation dose measured by SIMS.

Figure 6 gives the depth distribution of boron in the samples with different implantation dose measured by secondary ion mass spectroscopy (SIMS). During the subsequent drive-in annealing, dopants are driven out of the silicides and become piled up at the silicide/silicon interface. From Fig.6, the boron pile-up is formed at the NiSi/Si interface during the annealing process, although the boron concentration is not high enough. The low boron concentration is due to the relatively low annealing temperature as discussed above, which cannot effectively induce more boron pile-up at the interface. The boron pile-up at the NiSi/Si interface causes the upward bending of the conduction band, as illustrated in Fig.7, which results in the increase of the effective Φ_{bn}. The higher tempearature is, the sharper conduction band and the higher Φ_{bn} are.

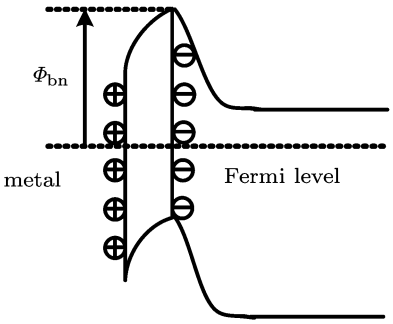


Fig.7. Schematic diagram of the energy band bending induced by dopant pile-up at the silicide/silicon interface.

4. Conclusions

The Schottky barrier height modulation of NiSi/n-Si by novel SADS technique is demonstrated in this paper. The electron Schottky barrier height is successfully modulated by 0.11 eV at a boron dose of 10^{15} cm^{-2} in comparison with nonimplanted samples. No phase change is observed in the Ni silicide films after BF_2 implantation with different dose. The modulation of SBH is attributed to upward bending of conduction band induced from the dopant pile-up at the silicide/Si interface. Besides, the surface morphology of nickel silicides is greatly improved for the BF_2 doped samples after silicidation. The results indicate that the SADS technique is feasible for the fabrication of Schottky source/drain Si MOS devices.

References

[1] Larson J M and Snyder J P 2006 *IEEE Trans. Electron Dev.* **53** 1048

[2] Fritze M, Chen C L, Calawa S, Yost D, Wheeler B, Wyatt P, Keast C L, Snyder J and Larson J 2004 *IEEE Electron Device Lett.* **25** 220

[3] Kedzierski J, Xuan P Anderson E H, Bokor J, King T J and Hu C 2000 in *IEDM Tech. Dig.* **57**

[4] Lepselter M P and Sze S M 1968 *Proc. IEEE* **56** 1400

[5] Li D Y, Sun L, Zhang S D, Wang Y, Liu X Y and Han R Q 2007 *Chin. Phys.* **16** 240

[6] Xiong S, King T J and Bokor J 2005 *IEEE Trans. Electron Dev.* **52** 1859

[7] Jang M, Kim Y, Shin J, Lee S and Park K 2004 *Appl. Phys. Lett.* **84** 741

[8] Zhu S Y Chen J, Li M F, Lee S J Singh J, Zhu C X, Du A Y, Tung C H, Chin A and Kwong D L 2004 *IEEE Electron Device Lett.* **25** 565

[9] Connelly D, Faulkner C, Grupp D E and Harris J S 2004 *IEEE Trans. Nanotechnol.* **3** 98

[10] Tao M, Udeshi D, Basit N, Maldonado E and Kirk W P 2003 *Appl. Phys. Lett.* **82** 1559

[11] Zhao Q T, Breuer U, Rije E, Lenk S and Mantl S 2005 *Appl. Phys. Lett.* **86** 062108

[12] Snyder J P, Helms C R and Nishi Y 1995 *Appl. Phys. Lett.* **67** 1420

[13] Kinoshita A, Tsuchiya Y, Yagishita A, Uchida K and Koga J 2004 in *VLSI Symp. Tech. Dig.* 168

[14] Ko C H, Chen H W, Wang T J, Kuan T M, Hsu J W, Huang C Y, Ge C H, Lai L S and Lee W C 2007 in *VLSI Sym. Tech. Dig.* **80**

[15] Kinoshita T, Hasumi R, Hamaguchi M, Miyashita K, Komoda T, Kinoshita A, Koga J, Adachi K, Toyoshima Y, Nakayama T, Yamada S and Matsuoka F 2006 in *IEDM Tech. Dig.* **71**

[16] Zhu S Y, Ru G P, Zhou J and Huang Y P 2005 *Chin. Phys.* **14** 1639

[17] Wong A S, Chi D Z, Loomans M, Ma D, Lai M Y, Tjiu W C, Chua S T, Lim C W and Greene J E 2002 *Appl. Phys. Lett.* **81** 5138

[18] Cheung S K and Cheung N W 1986 *Appl. Phys. Lett.* **49** 85

[19] Zhao F F, Zheng J Z and Shen Z X 2004 *Microelectron Eng.* **71** 104

[20] Donthu S K, Chi D Z and Tripathy S 2004 *Appl. Phys.* A **79** 637