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A new analytical model of high voltage silicon on insulator (SOI) thin film devices*

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A new analytical model of high voltage silicon on insulator (SOI) thin film devices is proposed, and a formula of silicon critical electric field is derived as a function of silicon film thickness by solving a 2D Poisson equation from an effective ionization rate, with a threshold energy taken into account for electron multiplying. Unlike a conventional silicon critical electric field that is constant and independent of silicon film thickness, the proposed silicon critical electric field increases sharply with silicon film thickness decreasing especially in the case of thin films, and can come to 141 V/μm at a film thickness of 0.1 μm which is much larger than the normal value of about 30 V/μm. From the proposed formula of silicon critical electric field, the expressions of dielectric layer electric field and vertical breakdown voltage ($V_{\rm B,V}$) are obtained. Based on the model, an ultra thin film can be used to enhance dielectric layer electric field and so increase vertical breakdown voltage for SOI devices because of its high silicon critical electric field, and with a dielectric layer thickness of 2 μm the vertical breakdown voltages reach 852 and 300V for the silicon film thicknesses of 0.1 and 5 μm, respectively. In addition, a relation between dielectric layer thickness and silicon film thickness is obtained, indicating a minimum vertical breakdown voltage that should be avoided when an SOI device is designed. 2D simulated results and some experimental results are in good agreement with analytical results.

Keywords: silicon critical electric field, breakdown voltage, thin silicon layer, SOI high voltage device

PACC: 7340Q, 7390, 4110F

1. Introduction

A series of structures and new concepts has been developed to solve the problems of low vertical breakdown voltage $V_{\rm B,V}$ of silicon on insulator (SOI) high voltage (HV) devices[1−11] where thin film device is attracting more and more attention because of its small dimension and easy isolation. Actually, a high breakdown voltage (> 700 V) has been experimentally obtained by using a top silicon layer with a thickness ($t_{\rm S}$) of 0.1 μm and a dielectric layer with a thickness ($t_{\rm I}$) of 2 μm.[2] It implies that silicon critical electric field $E_{\rm S,C}$ must be not a conventional constant of about 30 V/μm which is independent of $t_{\rm S}$, but it should vary with $t_{\rm S}$ especially at small values of $t_{\rm S}$, i.e. in the case of thin layers. In the present paper we aim at quantifying the dependence of $E_{\rm S,C}$ on $t_{\rm S}$, thereby analytically express the dielectric layer electric field $E_{\rm I}$ and vertical breakdown voltage $V_{\rm B,V}$ of SOI HV devices. Analytical results are compared with 2D simulated and some experimental results.

2. The analytical model

The cross-sectional view of an SOI device is shown in Fig.1, and the vertical electric field distribution is also shown there.

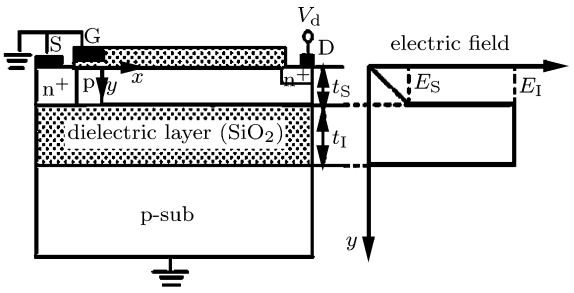


Fig.1. Cross-section of an SOI device and the vertical electric field distribution, where $V_{\rm d}$ denotes the applied voltage, $E_{\rm I}$ refers to the dielectric layer electric field, and $E_{\rm S}$ represents the electric field of top silicon: when it arrives at a silicon critical electric field $E_{\rm S,C}$, the breakdown takes place.

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Set a coordinate system as indicated on the right-hand side of Fig.1, then the 2D potential $\phi(x,\ y)$ in the drift region will be written as $\phi(x,\ y) = \omega(x,\ y) + \psi(x,\ y)$, where $\omega(x,\ y)$ and $\psi(x,\ y)$ are the contributions of $V_{\rm d}$ and depleted impurities in the drift region at complete depletion, respectively, and they satisfy the 2D Poisson equation

$$\frac{\partial^2\omega(x,0)}{\partial x^2} - \frac{\omega(x,0)}{t^2} = 0,$$
$$\frac{\partial^2\psi(x,0)}{\partial x^2} - \frac{\psi(x,0)}{t^2} = -\frac{qN(x)}{\varepsilon_{\rm s}}, \qquad (1)$$

where $N(x)$ is the drift region concentration; $t = t_{\rm S}\sqrt{0.5 + t_{\rm I}\varepsilon_{\rm s}/\varepsilon_{\rm I}t_{\rm S}}$ is characteristic thickness of SOI devices; $\varepsilon_{\rm S}$ and $\varepsilon_{\rm I}$ are permittivities of silicon layer and dielectric layer, respectively. From the boundary condition with $N(x) = N_{\rm d}$, the vertical electric field is obtained:

$$E_y(x,y) = \frac{qN_{\rm d}}{\varepsilon_{\rm S}}\left[1 - \frac{{\rm sh}\left[(W-x)/t\right]}{{\rm sh}\left(W/t\right)}\right]y, \qquad (2)$$

where $W = t{\rm arcth}\left[\dfrac{{\rm sh}(L_{\rm d}/t)}{V_{\rm d}/\phi + {\rm ch}(L_{\rm d}/t) - 1}\right]$, and $L_{\rm d}$ is the drift region length.

Taking the threshold energy $\varepsilon_{\rm T}$ into account for electron multiplying because the influence of threshold energy cannot be ignored in very narrow junction, an effective ionization rate $\alpha_{\rm eff}$, which is suitable for the calculation of breakdown voltage and obeys Chynoweth's law, is experimentally obtained as $\alpha(E) = A{\rm exp}(-B/E)$ with A=70.3 $\mu{\rm m}^{-1}$, and B=146.8 V/μm.[12] From the avalanche breakdown condition,

$$I = \int_0^{t_{\rm S}} A{\rm exp}\left(-\frac{Bt_{\rm S}}{E_{\rm S,C}y}\right){\rm d}y = 1, \qquad (3)$$

the following equation is obtained:

$$t_{\rm S} = \frac{1}{A[{\rm e}^{-\gamma} - \gamma E_{\rm i}(\gamma)]}, \qquad (4)$$

where $\gamma = B/E_{\rm S,C}$, and $E_{\rm i}(\gamma)$ is an exponential integral which can be obtained by referring to manual of numerical mathematics.

Expression (4) implicitly indicates a relationship between $E_{\rm S,C}$ and $t_{\rm S}$. Plotting $t_{\rm S}$ (μm) versus silicon critical field $E_{\rm S,C}$ (V/μm), their relationship is found to be approximately fitted by

$$E_{\rm S,C} = \frac{9.783(21.765 - \ln t_{\rm S})}{3.975 + \ln t_{\rm S}},$$
$$\text{when} \quad t_{\rm S} \geq 0.05\mu{\rm m}. \qquad (5)$$

Deviation of expression (5) is smaller than 3 percent when $t_{\rm S}$ is not more than 10 μm, and about 4–9 percent when $t_{\rm S}$ is between 10 and 100 μm. In addition to expression (5), we can have another formula of the silicon critical field, i.e. $E_{\rm S,C} = 1.24\times10^5 t_{\rm S}^{-1/7}$, which is derived from the habitually-used Fulop's ionization rate.[13]

Based on the continuity of electric displacement including interface charges, a dielectric layer electric field $E_{\rm I}$ (V/cm) is obtained from expression (5) as

$$E_{\rm I} = \left\{\left[\frac{9.783\varepsilon_{\rm s}(21.765 - \ln t_{\rm s})}{3.975 + \ln t_{\rm s}} \times 10^4\right] + q\sigma_{\rm in}\right\}/\varepsilon_{\rm I}, \qquad (6)$$

where $\sigma_{\rm in}$ is the interface charge density.

Expressions (5) and (6) are used to calculate $V_{\rm B,V}$ of SOI HV devices. From Fig.1, $V_{\rm B,V}$ is obtained as

$$V_{\rm B,V} = \left\{\left[\frac{9.783(21.765 - \ln t_{\rm S})}{3.975 + \ln t_{\rm S}}\right](\varepsilon_{\rm S}t_{\rm I} + 0.5\varepsilon_{\rm I}t_{\rm S}) + q\sigma_{\rm in}t_{\rm I}\times10^{-4}\right\}/\varepsilon_{\rm I}. \qquad (7)$$

Expression (7) shows the analytical dependence of $V_{\rm B,V}$ (V) on top silicon thickness $t_{\rm S}$ (μm) and dielectric layer thickness $t_{\rm I}$ (μm).

3. Results and discussion

Expression (5) shows that $E_{\rm S,C}$ is concerned only with $t_{\rm S}$, and so does the above expression derived from Fulop's ionization rate.[13] A comparison among the values of $E_{\rm S,C}$ calculated from expression (5), the experimental results from Grove[14] and Miller,[15] and the values from the *Esc* expression obtained from Fulop's ionization rate[13] is shown in Fig.2. It can be seen that $E_{\rm S,C}$ increases always with $t_{\rm S}$ decreasing, and when the layer thickness $t_{\rm S} > 1\mu$m, i.e. in the thick layer case, several curves well merge into one curve corresponding to about 30 V/μm. But distinctions appear when $t_{\rm S} \leq 1\,\mu$m: the values of $E_{\rm S,C}$ obtained from the proposed expression (5) and Grove and Miller's experimental values increase more sharply than those obtained from the expression derived from the Fulop's ionization rate. The value of $E_{\rm S,C}$ from expression (5) can reach 141 V/μm at $t_{\rm S}$=0.1 μm. The experimental values from Grove[14] and Miller,[15] some other experimental results[2,11] and 2D simulative results accord well with the proposed analytical results, which implies that expression (5) is applicable both for thin silicon films and for thick silicon films.

Figure 2 shows the dependence of $E_{\rm I}$ on $t_{\rm S}$ from expression (6), too. It is obvious that $E_{\rm I}$ increases with $t_{\rm S}$ decreasing especially when the values of $t_{\rm S}$ are small, i.e. in the thin layer case, as $E_{\rm S,C}$ does, which is favourable for increasing $V_{\rm B,V}$ because a certain thickness of dielectric layer can support a higher voltage. Interface charge $\sigma_{\rm in}$ which can be induced by special structures[6] has an obvious positive effect on $E_{\rm I}$, i.e. the value of $E_{\rm I}$ is enhanced from 11.1% (at $t_{\rm S}$=0.1 μm) to 28.6% (at $t_{\rm S}$=1 μm) with $\sigma_{\rm in}$ increasing from 0 to $1\times10^{12}\,{\rm cm}^{-2}$, respectively as shown in Fig.2. The effect of interface charge is more evident for thick silicon layer than for thin one.

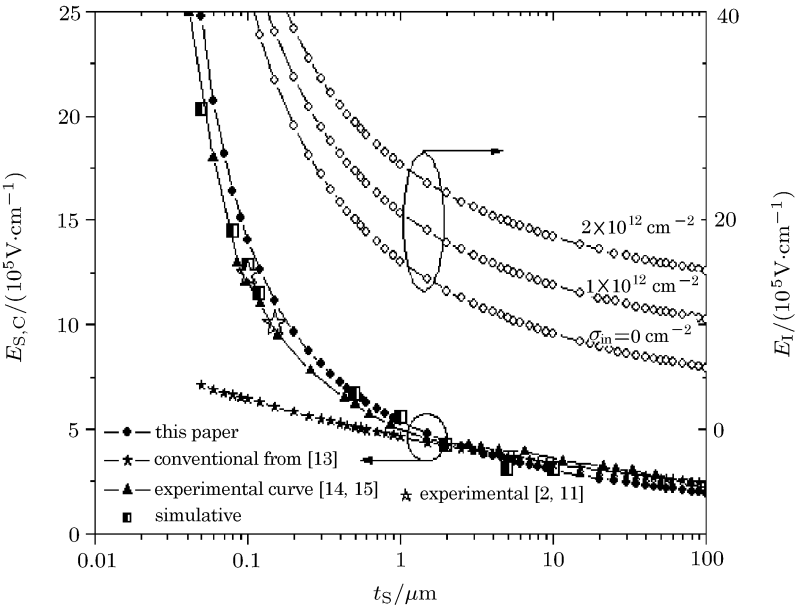


Fig.2. Dependences of $E_{\rm S,C}$ and $E_{\rm I}$ on $t_{\rm S}$. After some approximate transformations with $t_{\rm S}N_{\rm d}=\varepsilon_{\rm S}E_{\rm S,C}/q$, the experimental results from Grove[14] and Miller[15] are compared, and the effect of interface charge on $E_{\rm I}$ is also shown there.

The dependence of $V_{\rm B,V}$ (V) on $t_{\rm S}(\mu{\rm m})$ obtained from expression (7) with $\sigma_{\rm in}$=0 cm^{-2} is shown in Fig.3.

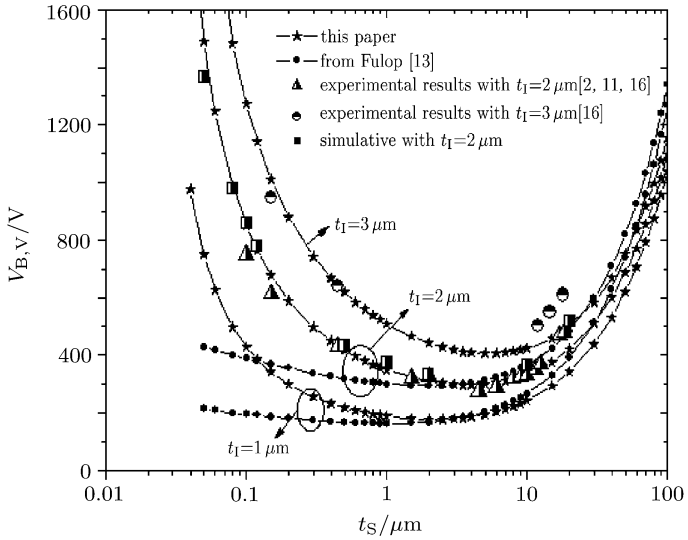
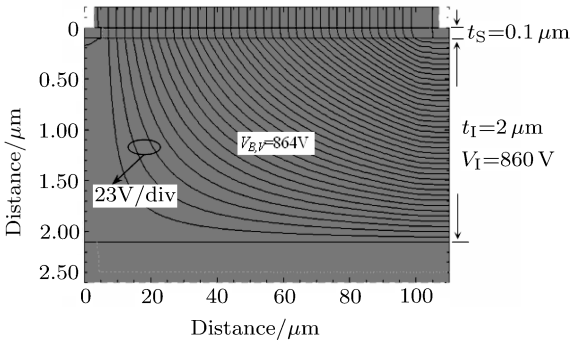


Fig.3. Dependences of $V_{\rm B,V}$ on $t_{\rm S}$ for $t_{\rm I}$=1, 2, 3 μm, separately. For simulation, linear impurity in the SOI layer is used in the same device structure as that shown in Fig.1, with $L_{\rm d}$=100 μm, $\sigma_{\rm in}$=0 cm^{-2} adopted for all cases.

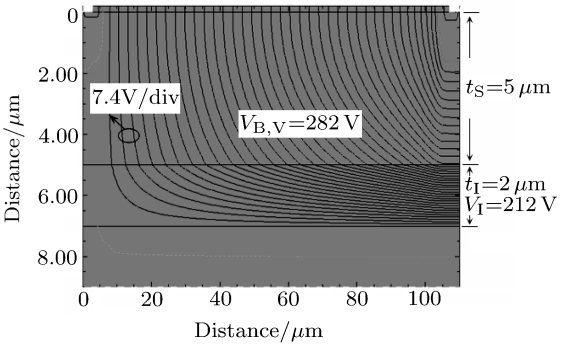
Because of the increasing of $E_{S,C}$ and E_I, $V_{B,V}$ increases sharply with t_S decreasing when the values of t_S are less than 5 μm, and when t_I=2 μm, the values of $V_{B,V}$ are 300 and 852 V when the values of t_S are 5 and 0.1 μm, respectively. When the value of t_S becomes large, i.e. when layer turns thicker, the value of $E_{S,C}$ is almost a constant of about 30 V/μm as shown in Fig.2, and so $V_{B,V}$ increases in a way of crescent t_S. The 2D simulated results by MEDICI and some experimental results[2,11,16] accord well with analytical results as shown in Fig.3. It indicates that using a thin SOI layer to enhance the value of $E_{S,C}$ is an effective approach to increasing the value of $V_{B,V}$. Moreover, it is obvious that a thicker layer (large value of t_I) can lead to a higher value of $V_{B,V}$ for the same value of t_S.

Potential profiles of SOI devices with t_S=0.1 and 5 μm are given in Fig.4, with t_I=2 μm adopted for both cases. Linear doping is used in the drift region for obtaining a uniform surface electric field. It is clear that the portion of equipotential contours falling into dielectric layer in Fig.4(a) is much more than that in Fig.4(b). Hence, voltage supported by dielectric layer, V_I, becomes very high: V_I=860 V for t_S=0.1 μm, and V_I=212 V for t_S=5 μm. In other words, the same thickness of dielectric layer will take on higher voltage, and so the value of $V_{B,V}$ increases.

Simulated distributions of vertical electric field under drain where breakdown occurs are shown in Fig.5. In accord with the analytical model, $E_{S,C}$ and E_I both sharply increase with t_S decreasing especially at small values of t_S, i.e. in the thick film case. Moreover, the effect of interface charge on E_I is also simulated. It is clear that interface charge can effectively enhance the value of E_I and so increase the value of $V_{B,V}$. For example, the value of $V_{B,V}$ is enhanced from 282 to 303 V when the value of σ_{in} increases from 0 to 2×10^{11} cm^{-2} with t_S=5 and t_I=2 μm respectively.



(a) $E_{S,C}$=128 V/μm and E_I=430 V/μm



(b) $E_{S,C}$=35 V/μm and E_I=106 V/μm

Fig.4. Potential profiles of SOI devices with t_S=0.1 (a) and 5 μm (b). Drift region length L_d is 100μm, t_I=2 μm. Drain is on the right-hand side and source is on the left-hand side for both cases. Linear doping is used in the drift region and $N_{dn} = (1.5n + 1)N_{d0}$, where n is the number of subregions, an integer ranging from 0 to 100; N_{dn} is the impurity concentration in the nth region; N_{d0} is starting doping (source region); N_{d0}=3.2×10^{15} cm^{-3} for t_S=0.1 μm and 5×10^{12} cm^{-3} for t_S=5 μm.

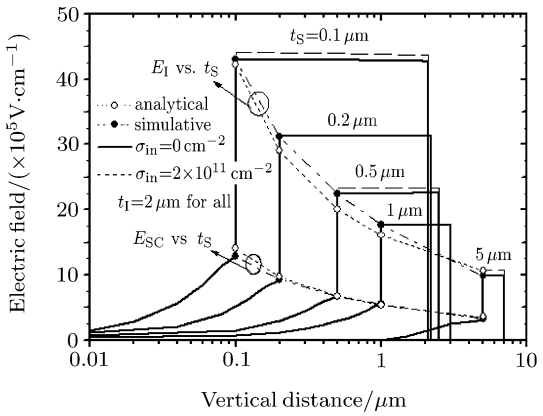


Fig.5. Simulated distributions of vertical electric field of SOI devices on the drain side, with L_d=100 μm and t_I=2 μm adopted for all cases. Analytical results of $E_{S,C}$ and E_I with σ_{in}=0 cm^{-2} are compared. The effect of interface charge on E_I is also given there.

From Fig.3, it is clear that $V_{B,V}$ with a marked t_I has a minimum if t_S and t_I satisfy a certain relation, and so this scenario should be avoided in order to obtain a higher value of $V_{B,V}$. Taking the minimum of $V_{B,V}(t_S)$ from expression (7) for σ_{in}=0 cm^{-2} and $V'_{B,V}(t_S)$=0, t_I is related to t_S by the following expression:

$$t_I = \frac{t_S(3.975 + \ln t_S)(21.765 - \ln t_S)}{154.44} - \frac{t_S}{6}, \qquad (8)$$

which means that once t_I and t_S satisfy expression (8), their corresponding value of $V_{B,V}$ is a minimum. Therefore, the dependence of t_I on t_S in expression (8) should be avoided when an SOI device is designed

because of the lowest voltage appearing on this condition.

4. Conclusion

A new analytical model of high voltage SOI thin film devices is given by solving 2D Poisson equation. The formula of silicon critical electric field $E_{S,C}$ is derived for the first time, based on which the expressions of E_I and $V_{B,V}$ are obtained. The values of $E_{S,C}$ and E_I both increase with t_S decreasing especially in the case of thin silicon layers. In addition, the relationship between t_I and t_S, leading to a minimum of $V_{B,V}$, is given, which should be avoided when an SOI device is designed. 2D simulated and some experimental results are in good agreement with analytical results.

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