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Effect of substrate bias on negative bias temperature instability of ultra-deep sub-micro p-channel metal–oxide–semiconductor field-effect transistors*

Cao Yan-Rong(曹艳荣)†, Hao Yue(郝 跃),
Ma Xiao-Hua(马晓华), and Hu Shi-Gang(胡仕刚)

School of Microelectronics, Xidian University, Xi'an 710071, *China*

Key Laboratory of Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, Xi'an 710071, *China*

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The effect of substrate bias on the degradation during applying a negative bias temperature (NBT) stress is studied in this paper. With a smaller gate voltage stress applied, the degradation of negative bias temperature instability (NBTI) is enhanced, and there comes forth an inflexion point. The degradation pace turns larger when the substrate bias is higher than the inflexion point. The substrate hot holes can be injected into oxide and generate additional oxide traps, inducing an inflexion phenomenon. When a constant substrate bias stress is applied, as the gate voltage stress increases, an inflexion comes into being also. The higher gate voltage causes the electrons to tunnel into the substrate from the poly, thereby generating the electron–hole pairs by impact ionization. The holes generated by impact ionization and the holes from the substrate all can be accelerated to high energies by the substrate bias. More additional oxide traps can be produced, and correspondingly, the degradation is strengthened by the substrate bias. The results of the alternate stress experiment show that the interface traps generated by the hot holes cannot be annealed, which is different from those generated by common holes.

Keywords: negative bias temperature instability (NBTI), substrate bias, hot holes, oxide traps
PACC: 7340Q, 7300, 7220J

1. Introduction

With the aggressive scaling down of metal–oxide–semiconductor field-effect transistors (MOSFETs) without the corresponding scaling of their supply voltages, especially when the gate oxide thickness turns thinner than 2 nm, the negative bias temperature instability (NBTI) receives more and more attention and becomes one of the most important reliability concerns for modern integrated circuits.[1−5] The NBTI is an effect occurring in p-channel metal–oxide–semiconductor field-effect transistors (PMOSFETs) under a negative gate bias stress at high temperatures. It leads to an increase in $V_{\rm th}$ and a reduction in drain current $I_{\rm d}$ and transconductance $G_{\rm m}$.[6,7] The origins of NBTI are generally thought to be the generation of interface states and the oxide charges due to the breaking of Si–H bonds and the diffusion of H related species into or the trapping of holes in the oxide respectively.[8−10] Though there are many papers reporting on NBTI resulting from the effect of holes from an inversion layer, there are relatively few papers dealing with the influence of hot carrier injection on the generation of interface states and oxide charges. Mahapatra *et al*[11] reported that hot holes could break not only Si–H but also Si–O bonds during applying a strong field stress. Tsuchiya[12] studied the effects of trapped electrons and interface traps, induced by a channel-hot-electron stress. In order to study the mechanism in detail, different conditions including drain voltage or substrate voltage stress are considered. Shiue *el al*[13] studied the interface trap generation under a substrate-hot-hole (SHH) stress for 4 nm thick gate oxides. Doyle *et al*[14] reported that the NBTI strengthened the hot carrier damage in p-channel MOSFET's. However, the microcosmic mechanism of generating interface traps or oxide charges is still not clear, and the exact role of the holes has not been fully understood yet. In this paper, to clarify the problem, a substrate voltage stress is supplied

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†E-mail: yrcao200@163.com

during applying a negative bias temperature (NBT) stress and the effect of holes on NBTI degradation is studied. A model that is based on the hot hole injection is developed to explain the reinforced effect on the degradation of the positive substrate bias V_b applied during applying an NBT stress.

2. Experiment

The PMOSFETs used here are of surface channel. They were manufactured by using a 90 nm process technology with a lightly doped drain (LDD) structure and the shallow trench isolation (STI) scheme. The gate oxides of all devices were annealed in an N_2O atmosphere after thermal growth. The devices used here had an ultra-thin gate oxide thickness of 1.4 nm, a gate width of 10 μm, and a gate length of 0.1 μm. Agilent B1500A, a high precision semiconductor parameter analyser, was used to perform the tests. Substrate voltage stress $V_{bstress}$ is supplied during applying an NBT stress $V_g = V_{gstress}$ with V_d(drain voltage) $=V_s$ (source voltage)=0 at elevated temperatures. Stress was interrupted at regular intervals, and device parameters such as threshold voltage V_{th}, subthreshold slope S and stress induced leakage current (SILC) were measured.

3. Results and discussion

Figure 1 shows the threshold voltage shift as a function of stressing time when a substrate bias stress is applied during applying a static NBT stress of –1.8 V ($V_{gstress}$=–1.8 V) at T=120°. With the value of V_b varying from 0 to 5V, the degradation of V_{th} is

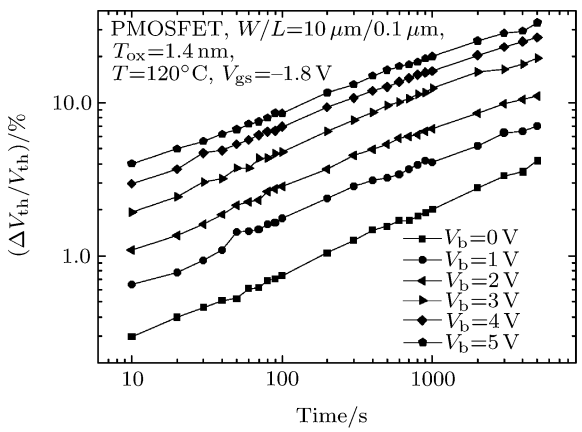


Fig.1. The threshold voltage shifts as a function of stressing time under a static NBT stress and several different substrate bias stresses.

increasing. All V_{th} shifts exhibit a similar time dependence. When the degradation values for stress times: 100, 1000, and 5000s are plotted against substrate bias stress, there appears an inflexion point at about 2 V turning up as displayed in Fig.2. The degradation slope at V_b values lower than 2 V is smaller than that at V_b values higher than 2 V.

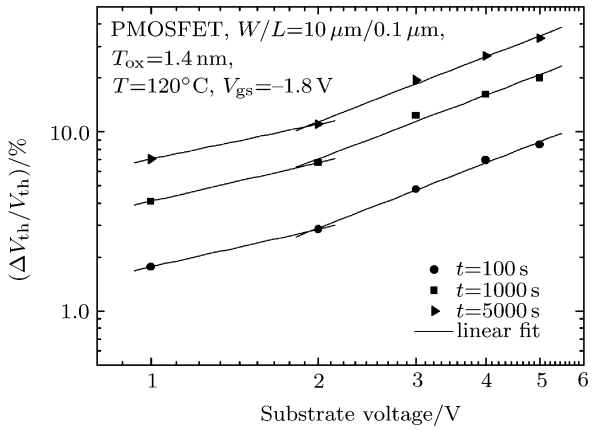


Fig.2. The threshold voltage shifts as a function of substrate bias stress under a static NBT stress and some different stressing times.

The origins of NBTI are generally thought to be the generation of interface states and the oxide charges, and now it is believed that holes are responsible for the breaking of Si–H bonds during applying an NBT stress.[15] When a positive substrate bias ($V_b > 0$) is applied, the hole population in the inversion layer of channel decreases with the V_b increasing due to the bulk effect.[16] Figure 3 shows the hole concentration in the inversion layer, simulated by using the software SILVACO. When the substrate bias changes from 0 to 5 V, the hole concentration decreases more than 10 times. When a positive bias is applied to the n-type substrate, with the source and the drain grounded, the p–n junction formed by the hole inversion layer and the n type substrate semiconductor is reverse-biased. The depletion region is widened by the reverse bias, and then the positive charges of the depletion region increase and the holes of inversion layer decrease. Though the hole concentration in the inversion layer decreases, the degradation of parameters such as threshold voltage V_{th}, drain current I_d, transconductance G_m (I_d and G_m are not shown here) and SILC, turns serious under conditions of NBT stress, with V_b supplied. In other words, the substrate bias stress can strengthen the degradation. Through the study in the following sections, we find that when a positive bias is applied to the substrate,

a number of hot holes will be generated and the generation of energetic (hot) holes should be the origin of the degradation enhancement.

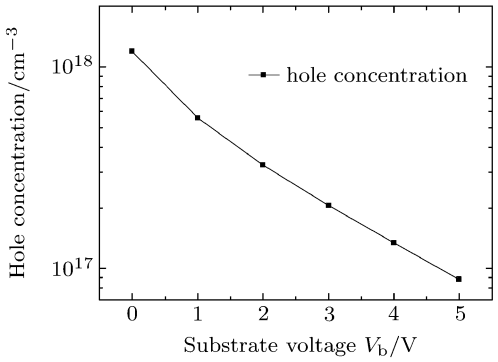


Fig.3. Hole concentration in the inversion layer of channel (V_g=–1.8 V) with V_b varying from 0 to 5 V, simulated by using the software SILVACO.

Figure 4 shows the energy band diagrams of PMOSFET under an NBT stress with V_b=0, $V_b > 0$, and W denoting the width of depletion region. During applying an NBT stress with V_b=0, there are holes present in the inversion layer at the substrate as shown in the left panel of Fig.4. There is a probability for some holes to tunnel into the oxide and break the Si–H bonds and generate the Si dangling bonds Si•, where the black dot denotes the dangling bonds, namely, the interface states. We refer to the effect of the normal holes as the normal hole effect. When $V_b > 0$ as shown in the right panel of Fig.4, the width of depletion region becomes much wider,[16] and some holes can be accelerated by this space charge region and under the action of the electric field they move from the substrate to the channel. Therefore, hot holes with higher energies are generated and then there come into being two types of holes in the inversion layer: the normal holes with common energy and the hot holes with higher energy. The hot holes with higher energies can tunnel into the oxide and break Si–H bonds more effectively than the normal holes.[17] With the substrate bias further increasing, some hot holes may obtain enough energy to break the Si–O bonds,[11] and generate the associated defects, namely oxide traps which can trap the diffusing H related species or holes injected into the oxide. Meanwhile, some of them at or near the interface of Si/SiO_2 can play a role as interface traps.[18] Then the drastic degradation caused by hot holes occurs. Therefore, it is very possible for smaller population of holes (as shown in Fig.3) to induce more degradations. We refer to the effect of hot holes on the degradation of device as the hot hole effect. When substrate voltage is smaller, the effect of the hot holes is not as severe as that with higher values of V_b, and with the population of holes reducing, the first stage of smaller pace degradation is produced as shown in Fig.2 in front of the inflexion point 2 V. When substrate voltage increases, the hot hole effect increases quickly[19] and becomes the main factor for degradation during stressing. And the more the substrate voltage increases, the higher the efficiency for the hot holes to break the Si–H bonds and Si–O bonds will be, thereby the degradation enhancement comes to appear as the second stage of larger pace degradation in Fig.2 in rear of the inflexion point 2 V. The inflexion point is such a voltage point that if a voltage is higher than it then the substrate bias can strengthen the hot hole effect. However, it is related to many respects such as the energies consumed for transporting and tunnelling for holes, the dissociation of the Si–O bonds and so on. Therefore, the confirmation of the inflexion point in theory needs more detailed and deeper study.

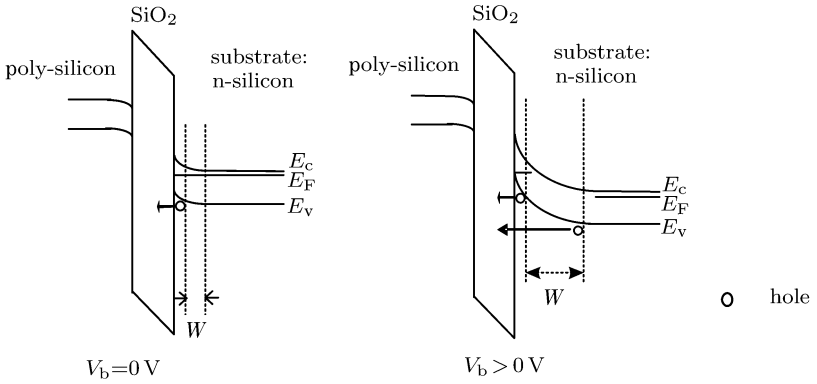


Fig.4. Energy band diagram for PMOSFET under an NBT stress with V_b=0 and $V_b > 0$.

Figure 5 shows the SILC and the threshold voltage shift as a function of substrate bias during applying a static NBT stress of –1.8 V ($V_{\rm gstress}$=–1.8 V) at T=120°. And the SILC shows a similar dependence to that of the threshold voltage shift on substrate bias. There is also an inflexion point at 2 V in the SILC degradation and the degradation pace is lower when $V_{\rm b}$ is smaller than 2 V but higher when larger than 2 V. As broken Si–O bonds can give rise to SILC,[19] when the SILC is measured at $|V_{\rm g}|$ >1 V, it can be seen as a good monitor for oxide trap.[20] The degradation of SILC implies that the oxide traps are generated and their generation is enhanced when $V_{\rm b}$ >2 V, as the hot hole injection probability is increased quickly, which is consistent with the result in Ref.[19].

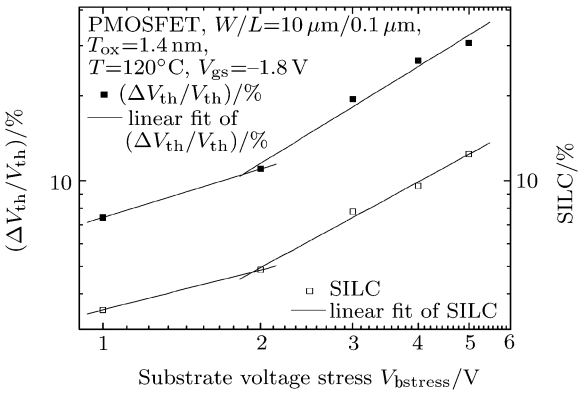


Fig.5. Stress induced leakage current (SILC) measured at $|V_{\rm g}|$=1.2 V and the threshold voltage shift plotted together as a function of substrate bias during applying a static NBT stress of –1.8 V ($V_{\rm gstress}$=–1.8 V) at T=120°.

Figure 6 shows the dependence of the threshold voltage shift and the SILC on gate voltage stress when a constant substrate bias stress is applied. A similar inflexion phenomenon comes forth at $V_{\rm g}$=–1.8 V. However, when the substrate electrode is grounded, the threshold voltage shift shows a logarithmic dependence on the gate voltage stress, namely it takes on linearity in double-log scale.[21] Therefore, the enhanced degradation of threshold voltage under higher values of $V_{\rm g}$ should be induced by the effects of substrate bias stress and hot holes injection. The same inflexion of SILC is obtained to assure the generation of oxide traps and implies the close correlativity between the oxide traps and hot holes.

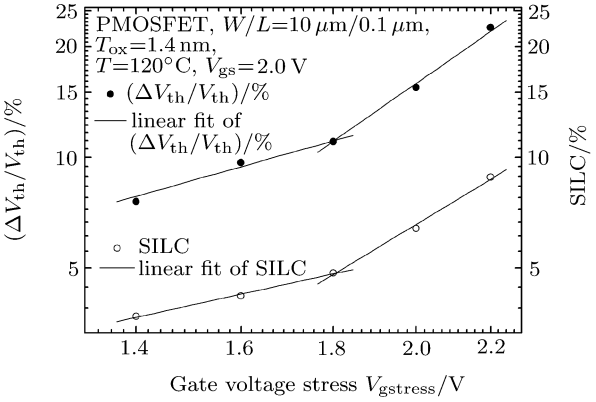


Fig.6. Threshold voltage shift and SILC measured at $|V_{\rm g}|$=1.2 V as a function of gate voltage stress when $V_{\rm b}$=2 V is applied.

The energy band diagrams of PMOSFET under higher values of NBT stress with $V_{\rm b}$=0 and $V_{\rm b}$ > 0 are shown in Fig.7. At a higher value of $V_{\rm g}$ ($V_{\rm b}$=0 V), the electrons tunnel from the poly and into the substrate and generate electron–hole pairs by impact ionization (the effect of impact ionization can be ignored when the value of $V_{\rm g}$ is smaller). The generated holes and the holes present at the substrate in the inversion layer all can play a role in breaking Si–H bonds, thereby generating the interface traps. However, fewer Si–O

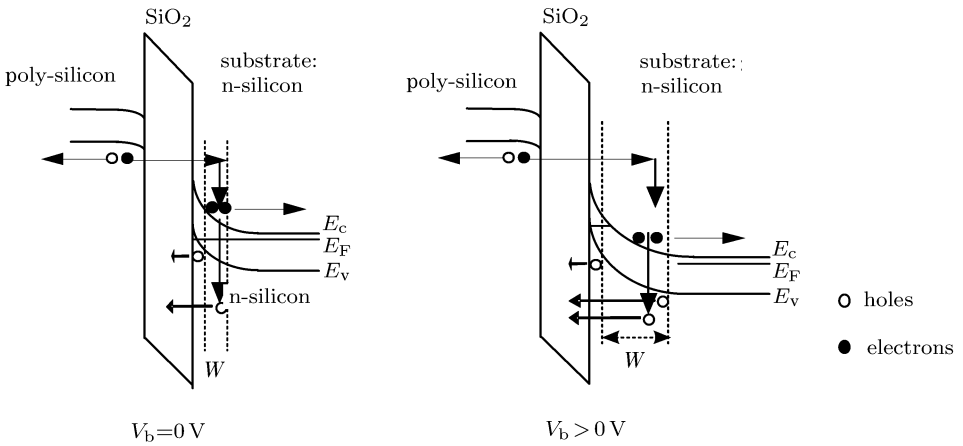


Fig.7. Energy band diagram for PMOSFET under a high NBT stress with $V_{\rm b}$=0 V and $V_{\rm b}$ > 0.

bonds are broken as the number of energetic holes is small. When substrate bias is supplied, the impact ionization holes can be accelerated to high energies as the depletion region is widened. Therefore, the number of hot holes is larger as it is composed of two parts, i.e. impact ionization hot holes and substrate hot holes. Then more energetic holes can tunnel into the oxide and generate more oxide traps, and thereby enhance the degradation to such an extent that the degradation can be seen in rear of the inflexion point as shown in Fig.6.

The broken Si–O bonds at or near the interface of Si/SiO_2 can play a role as interface traps.[18] The alternate stress is applied to clarifying the characteristic of interface traps generated by hot holes. First, a constant negative gate bias stress, V_g=–1.8 V, coupling with different values of substrate bias is applied for 1000 s. And then a constant positive gate bias, V_g=+1.8 V, is supplied without applying any substrate bias for another 1000 s. Sub-threshold slope S is measured to monitor the change of interface traps.[22] The results are plotted in Fig.8(a). In the degradation process, when the substrate bias stress changes from 0 to 5 V, the degradations are increased, which shows that there are additional interface traps generated by the hot holes. In the recovery process, there are clear recoveries occurring. After about 400 s, the recoveries enter into a saturation state, and the recovered sub-threshold slopes (recovered S = the last point value of the degradation process—the last point value of the recovery process) are calculated and shown in Fig.8(b). From Fig.8(b), we can see that the recovered sub-threshold slopes with applying a substrate bias are almost the same as that without applying any substrate bias, namely, there is no dependence of the recovered sub-threshold slope on substrate bias stress. The shift of sub-threshold slope during the degradation process with applying the substrate bias arises from the generation of interface traps produced by the hot holes and common holes together. However, the recovered part of sub-threshold slope is caused by the recovery of interface traps generated by common holes not hot holes, namely, only the interface traps induced by common holes can be annealed, which is accordant to the previous results.[18]

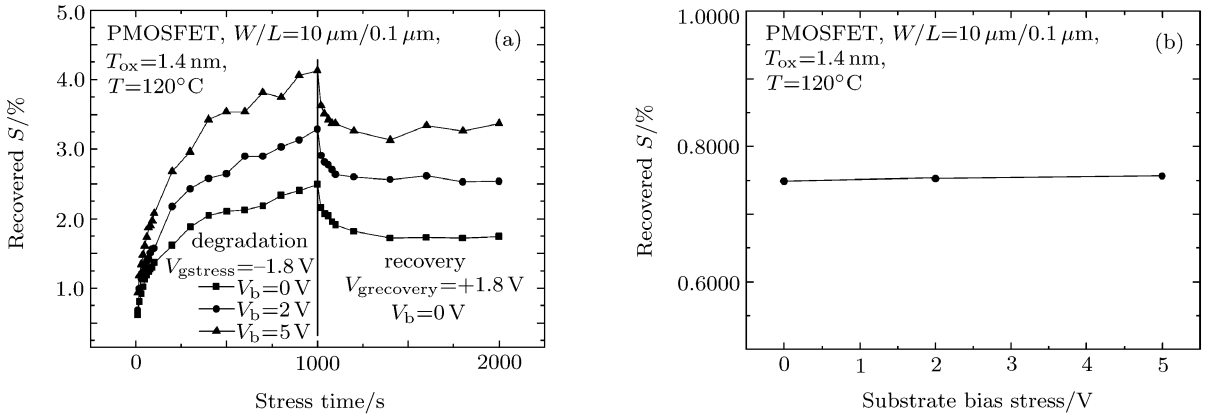


Fig.8. Sub-threshold slope shifts of degradation under constant $V_{gstress}$=–1.8 V and various V_b and recovery under constant $V_{gstress}$=+1.8 V and V_b=0 V (a) and the same recovered sub-threshold slope versus substrate stress (b).

4. Conclusions

In this paper, we investigate the effect of substrate bias on the degradation during applying an NBT stress. When a smaller gate bias stress is applied, the degradation of NBTI is enhanced by the substrate bias stress, and there appears an inflexion point at 2 V. The degradation pace becomes larger when the substrate bias is higher than the inflexion point. This phenomenon is explained by the effect of substrate hot holes. Under the influence of widened depletion region, the holes from the substrate can be accelerated to high energies and injected into the oxide, thereby generating additional oxide traps that cause the inflexion phenomenon. When a constant substrate bias stress is applied, with the gate voltage stress increasing, the inflexion comes into being also. The higher gate voltage causes the electrons to tunnel into the substrate from the poly, and the electron–hole pairs are generated by impact ionization. Therefore, there

are two kinds of holes, i.e. the holes generated by impact ionization and the holes from the substrate, which can be accelerated to high energies by the substrate bias. Then more additional oxide traps can be produced and so the degradation is enhanced by the substrate bias. The results of alternate stress experiment show that the interface traps generated by the hot holes cannot be annealed, which are different from those generated by common holes.

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