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# A CMOS-compatible silicon substrate optimization technique and its application in radio frequency crosstalk isolation*

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In this paper, a complementary metal–oxide semiconductor (CMOS)-compatible silicon substrate optimization technique is proposed to achieve effective isolation. The selective growth of porous silicon is used to effectively suppress the substrate crosstalk. The isolation structures are fabricated in standard CMOS process and then this post-CMOS substrate optimization technique is carried out to greatly improve the performances of crosstalk isolation. Three-dimensional electro-magnetic simulation is implemented to verify the obvious effect of our substrate optimization technique. The morphologies and growth condition of porous silicon fabricated have been investigated in detail. Furthermore, a thick selectively grown porous silicon (SGPS) trench for crosstalk isolation has been formed and about 20dB improvement in substrate isolation is achieved. These results demonstrate that our post-CMOS SGPS technique is very promising for RF IC applications.

**Keywords:** substrate optimization, selectively grown porous silicon (SGPS), radio frequency, crosstalk isolation
**PACC:** 8160C, 8116D, 6140G

## 1. Introduction

With the development of mobile communication, the rapidly growing market presents an urgent need for high-performance mixed-signal integrated circuits technology. More and more radio frequency integrated circuits (RFICs) have been made on a single chip. There are many promising advantages for single chip RFICs, such as high density of package, low cost, small volume and so on. However, RF crosstalk through conventional Si substrate with low resistivity is still a main problem for single chip RFICs. Noise from switching transient in digital circuits can travel through the Si substrate to degrade the performance of noise sensitive circuit elements such as low noise amplifier (LNA), voltage-controlled oscillator (VCO) and phase-lock loop (PLL). Therefore, effective isolation between different function circuits is becoming major challenges to single chip RFICs. Several methods such as junction isolated well,[1] micromachining process,[2,3] silicon on insulator (SOI) substrate[4,5] and Faraday cage isolation structures[6] have been proposed to achieve effective isolation. Although these techniques obviously can suppress the crosstalk, they may be difficult to be integrated into the standard complementary metal–oxide semiconductor (CMOS) technology because modifying or adding process steps are required. As a result, the above methods may increase the cost and reduce the yield.

Recently, porous silicon (PS) has been proposed as a promising solution for effective crosstalk isolation,[7−10] due to its much higher resistivity, simple fabrication process and near-zero mismatch with bulk Si.[11] In the above reports, PS layers have been formed on the whole Si wafer firstly, and then isolation structures are fabricated on these existing PS layers. The pre-formation and the whole-wafer growth of PS layer may contaminate Si wafer and may not provide strong mechanical support, which will influence the subsequent fabrication of isolation structures.

In this paper, we report the design and realization of crosstalk isolation using CMOS-compatible silicon substrate optimization technique. A post-CMOS selectively grown porous silicon (SGPS) technique, which is used to effectively achieve the crosstalk isola-

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tion, is demonstrated. Different from other PS-based techniques,[7−10] the SGPS technique is completely post-CMOS based, convenient to be realized and completely compatible with conventional VLSI process without modifying any step in the standard CMOS process. The thick PS layer is selectively grown under inductors from the backside of silicon wafer when all standard CMOS processes are finished. Three-dimensional electro-magnetic simulator HFSS is used to characterize the obvious effect of crosstalk isolation with the use of our proposed SGPS technique. High quality thick PS layers are selectively grown using the electrochemical etching technique. The structure, morphology and growth rate of PS for substrates with different resistivities are investigated in detail, which further demonstrates the feasibility of our SGPS substrate for crosstalk isolation. Furthermore, a thick SGPS trench for crosstalk isolation is formed and the improvements in substrate isolation are measured and discussed.

## 2. Crosstalk isolation structure and three-dimension electro-magnetic simulation

The behaviour of substrate crosstalk includes three aspects: noise generation, transmission and noise reception. For noise transmission, the substrate resistivity and the distance between injector and victim pattern are the main impact factor to noise coupling. As to the injector and victim patterns, the area, perimeter, shape and the angle can influence the final crosstalk. Furthermore, the substrate crosstalk and loss will have great effect on the performance of RF integrated circuits, such as the noise figure for LNA and phase noise for VCO. It is expected that these critical performance can be effectively improved by suppressing the substrate crosstalk and loss. These concepts will be adequately verified in the following simulation.

In order to illustrate the influence of crosstalk between noise-generating pads and the noise-sensing pads, the specific simulation structure has been designed as shown in Fig.1. Figure 1(a) is the typical G–S–G structure where the "*S*" port is connected with the signal pads we concentrate on. Figure 1(b) shows the schematic cross section of the designed structure. The pads are designed to be 80$\mu$m×80$\mu$m in area, and the distances between two signal sources are varied in the range of 100, 150 and 200$\mu$m, to investigate the influence of pad-distance on crosstalk isolation.

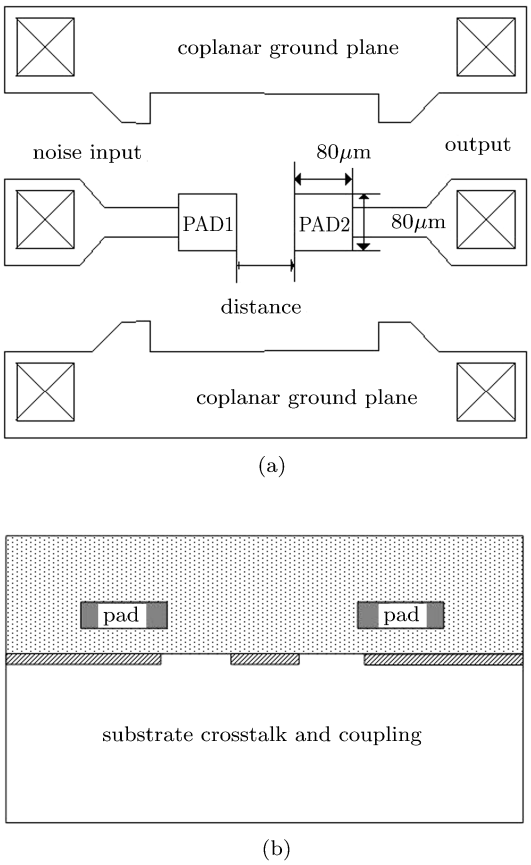



**Fig.1.** (a) The simulation structure for substrate crosstalk and (b) the schematic cross section of the designed structure.

In our simulation, the thickness of Si substrate is 400$\mu$m, which is commonly adopted in VLSI foundries. The simulations are implemented for conventional and optimized substrates to investigate the effect of our substrate optimization technique. For conventional substrate, the resistivity and the effective dielectric constant are 5Ω·cm and 11.9, respectively. Our CMOS-compatible silicon substrate optimization technique is introduced to improve the substrate characteristics effectively, especially to greatly increase substrate resistivity and obviously decrease substrate effective dielectric constant. Therefore, for optimized substrate, the resistivity and the effective dielectric constant are $10^6$Ω·cm and 3.75, respectively. Note that the selections of our simulation parameters above are based on and homologous with the practical situation in our further experimental research.

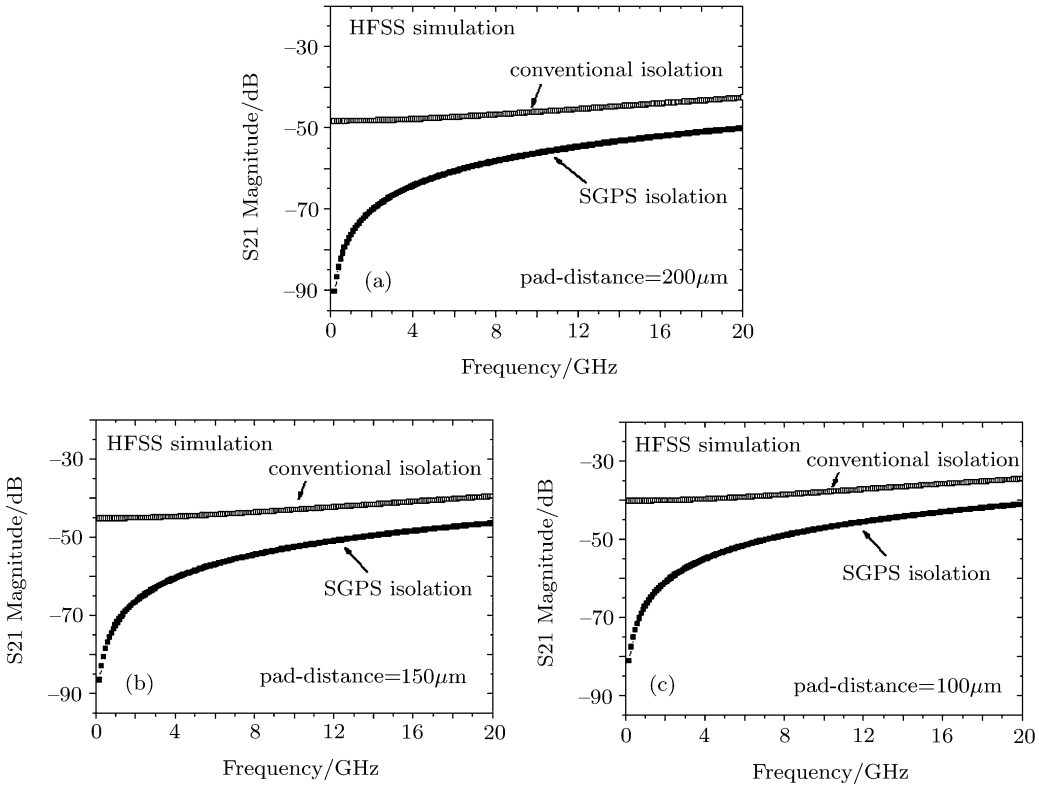



**Fig.2.** The three-dimension electro-magnetic simulation results for different pad distances. (a) 200$\mu$m, (b) 150$\mu$m and (c) 100$\mu$m.

Three-dimensional electro-magnetic simulator HFSS is used to calculate the crosstalk isolation on different substrate types. Figures 2(a), 2(b) and 2(c) illustrate the $S_{21}$ magnitude versus frequency in the range from 0 to 20 GHz. From these figures, it can be observed obviously that the optimized substrate is able to suppress effectively and obviously the crosstalk between the two pads as compared with the conventional substrate. About 10–40dB improvement in substrate isolation has been achieved under different frequencies due to much higher resistivity and lower effective dielectric constant of the optimized substrate. For recent wireless RF applications such as Bluetooth, Zigbee and IEEE 802.11b/g, the frequency ranges of which are concentrated in ISM (Industrial Scientific Medical) Band (from 2.4 to 2.4835GHz), the improvement of 20–25dB is very obvious. Note that for the same type of substrate with different pad-distances, about 2–5dB difference in $S_{21}$ magnitude is attributed to the strong dependence of the overall crosstalk on the pad separation.[7]

Therefore, from the simulations above, it has been verified that substrate crosstalk can be suppressed effectively with the optimization of substrate parameters, which implies that a new approach for making substrate is to be proposed and studied in our following research. In summary, the utilization of optimized substrate is a promising approach which can evidently improve the crosstalk isolation of Si substrate.

## 3. Experimental research on porous silicon growth to obtain substrate optimization

The growth of thick PS layer is the crucial process of the proposed post-processing procedure. In our experiment, the thick PS layer growth was carried out in an electrochemical cell with the silicon substrate used as the anode and a graphite rod as the cathode.

Figure 3 shows the schematic diagram of the electrochemical cell for the anodization process. The chip was fixed at one side of the Teflon etching cell to make sure that the backside of the chip should contact the electrolyte. The electrodes on the front side of the chip were connected with the anode of a precise DC current power. The PS growth followed a conventional electro-chemical process[12] and generally, the proper-

ties of PS, such as thickness, pore diameter and microstructure of the silicon, depended on the anodization conditions, including the electrolyte, current density, wafer type and resistivity, anodization duration and temperature.[11−16] Herein, silicon wafers with a thickness of 400$\mu$m and a diameter of 10 cm were of (100) p-type single crystals, as commonly adopted by CMOS industry. The polished front sides of the wafers were ion implanted, and aluminium films were deposited to ensure a perfect ohmic contact with the electrode to the wafer. Silicon nitride masks were grown on the backsides of the wafers with low pressure chemical vapour deposition (LPCVD).

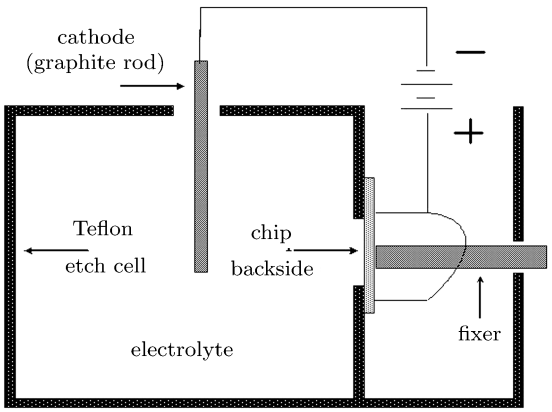



**Fig.3.** Schematic diagram of the electrochemical etching cell for anodization in the SGPS process.

In this work, a special mixed solution (40% HF and 99.9% dimethyl formamide with volume ratio of 1:4) was adopted. This kind of mixed solution is commonly used in PS growth and can effectively help to achieve regular and valuable pores in PS.[11,12] All samples in this experiment were fabricated at room temperature. After the anodization process, the fabricated samples were immersed in the acetone solution for an hour and dried subsequently. Finally, the samples were taken out from the drying vessel for characterization. The morphologies of the grown PS samples were characterized using scanning electron microscope (STARTA DB235).

Some papers have reported the surface morphologies of PS under different anodic current densities.[11−15] However, none of them reported the conditions of PS growth for silicon substrates with different resistivities. Nowadays, silicon wafers with different resistivities have been widely adopted in modern VLSI foundry. Therefore, it is necessary to investigate the conditions of PS growth for Si substrate with different resistivities, which is also very important for our further work. In our investigations, silicon substrates with different resistivities are studied in detail. Figure 4 shows the surface morphologies of a series of PS samples with different resistivities. The substrate resistivities of five samples are 3, 8, 15, 35 and 100Ω·cm, respectively. Note that substrates with resistivities of these values are most commonly adopted by many factories in standard VLSI industry. From these SEM images, the formed pores with diameters about 0.8–1.2$\mu$m indicate that the PS grown in this work belongs to macropore PS.[11]

The contour, distribution and surface roughness of the formed pores show different characteristics of silicon substrates with different resistivities. Note that the doping density of substrate has a great influence on the anodization etching process. Due to the sufficient carriers to carry out the electro-chemical reaction, the growth of PS for Si substrate with high doping density shows more active characteristics. Since the substrate of the sample in Fig.4(a) has the lowest resistivity (3Ω·cm), the morphologies of the formed macropores are the most uniform, dense and symmetrical. With the increase of substrate resistivity, the number of carriers in the substrate decreases due to the reduction of doping density. Therefore, the morphologies of the formed macropores begin to change in substrates with different resistivities. The diameters of the formed macropores in Figs.4(b)–4(d) are not as uniform as that in Fig.4(a). However, observation reveals that the formed macropores in the Si substrate have similar surface morphologies when the substrate resistivities are controlled in the range of 8–35Ω·cm. Furthermore, if the value of the substrate resistivity exceeds 100Ω·cm, the surface state will become worse. Figure 4(e) shows the SEM image of the anodized substrate sample with a resistivity of 100Ω·cm. In this figure, the cylindrical pores are covered by the oxidized PS and the contours of the pores become blurred. Some pore walls are disconnected due to the higher current density to maintain the PS formation.

Note that for some rare situations, one kind of silicon wafer is also possible to be adopted in some CMOS processes, i.e. one side of silicon wafer is polished while the other side remains unpolished (coarse side). The surface morphologies may show different characteristics of this special silicon wafers due to the effect of induced growth.[17,18] As shown in Fig.4(f), the pores of PS are very irregular and the effect of induced growth can be observed obviously. Despite

the anomalous morphologies of PS, the growing condition of the silicon wafer with single side unpolished is proved to be the same as that with both sides polished. Therefore, our substrate optimization technique can be effectively implemented for all kinds of silicon wafers used in modern VLSI foundry.

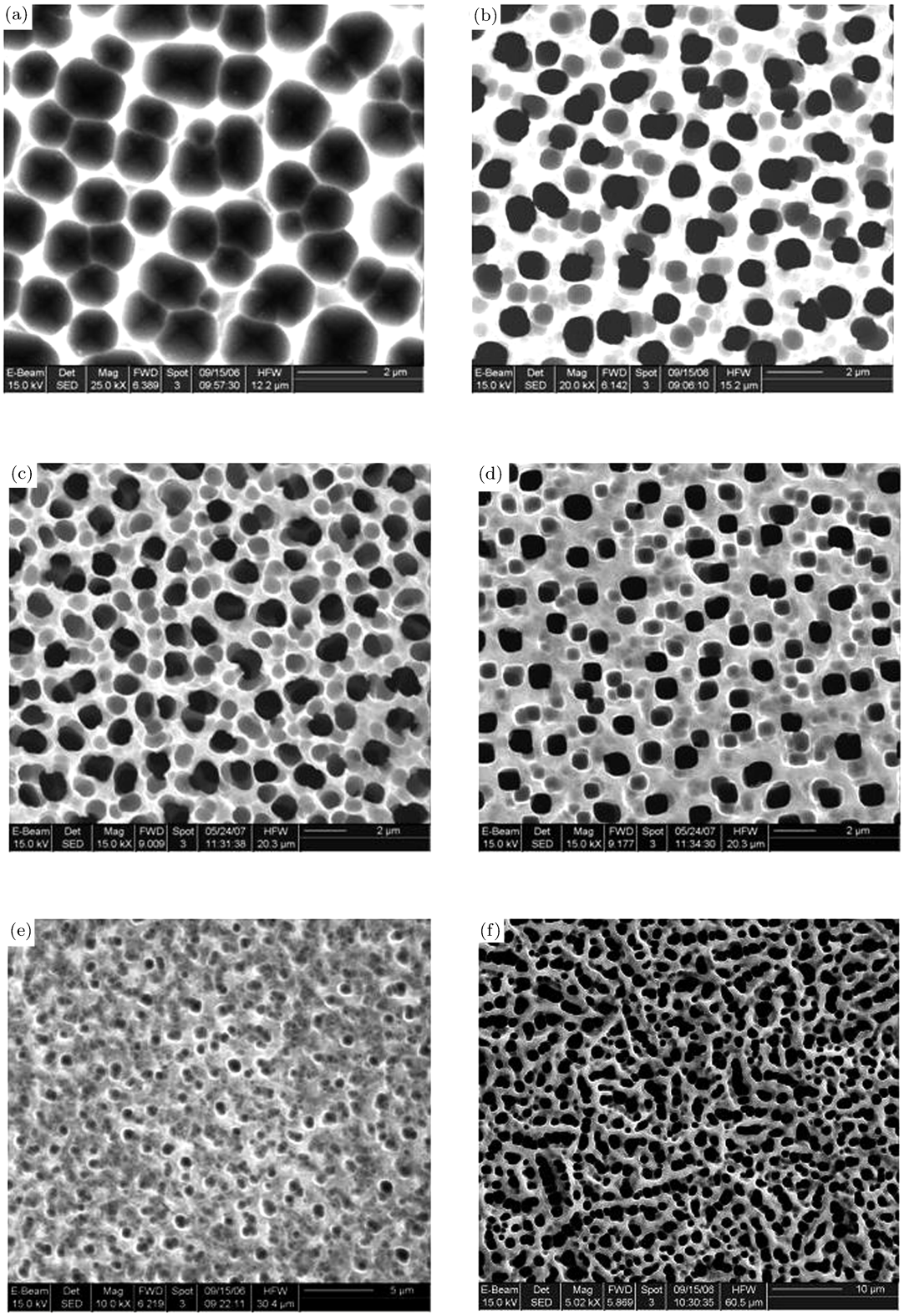



**Fig.4.** The surface morphologies of PS formed for Si substrates with resistivities of (a) 3, (b) 8, (c) 15, (d) 35 and (e) 100Ω·cm; (f) Si substrate with one side unpolished.

In order to control the growth velocity of PS by the present technique, the growth rates of silicon substrates with different resistivities are also investigated in detail. The growth rate information is also very critical especially when we need to control the anodization time and thickness of PS precisely. Figure 5 illustrates the relationship between the thickness of PS layer obtained and the anodization duration under a current density of 30mA/cm$^2$. It can be seen from Fig.5 that the growth velocity of porous silicon is approximately constant in growing PS layer. Furthermore, silicon wafers with different resistivities grow with different linear velocities. As shown in Fig.5, the silicon wafer with lower resistivity grows at a higher rate because it is highly doped and contains more carriers for anodization. The growth rates illustrated in Fig.5 can ensure a successful control of the anodization time and the thickness of PS in our substrate optimization technique.

Besides, the cross-section of the PS layer may suggest a chance to investigate the interface between the PS layer and the bulk silicon. Figure 6(a) shows the cross-section image of the grown PS layers while Fig.6(b) shows the high magnification image of a formed pore. This sample, with a resistivity of 15Ω·cm, was fabricated at 30mA/cm$^2$ current density for 200min. The regular pores grow vertically to the interface, which can be clearly observed in the SEM image of higher magnification. The interface formed is parallel to the two sides of the wafer. Figure 6 shows that the formation of PS can be successfully achieved under the above conditions, based on corresponding technical considerations.

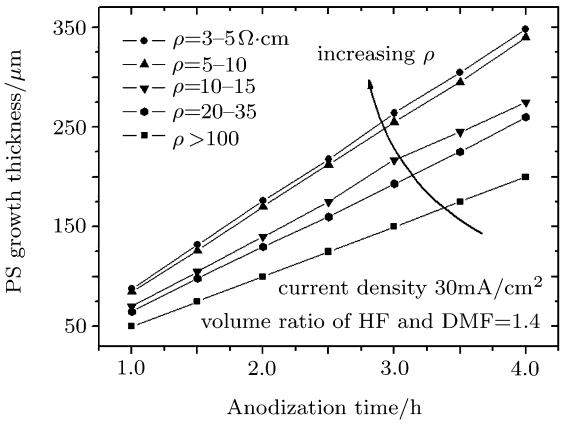



**Fig.5.** The growth rate versus anodization time for Si wafers with different resistivities.

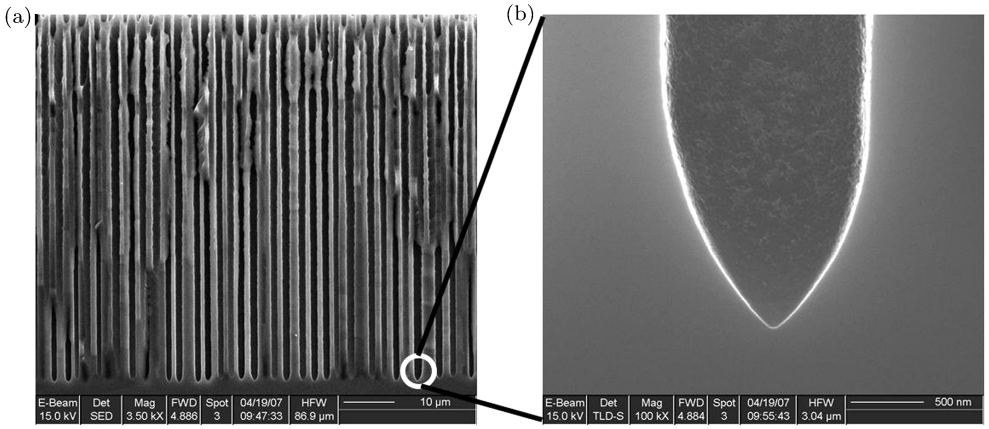



**Fig.6.** (a) The cross-section SEM image of the grown thick porous silicon sample and (b) a high-magnification pore.

## 4. Design and realization of substrate optimization technique for RF crosstalk isolation

The whole process for substrate optimization technique was realized in two steps. Firstly, the surface circuits and isolation structures were fabricated on silicon wafers using the standard CMOS process. Then, the performance of crosstalk isolation were improved using our post-CMOS SGPS technique.

Figure 7 shows the cross-section of the isolation structure in our work. In order to realize the controllable generation of electric field, 30 nm heavily doped poly-silicon was selectively deposited on p-type (001) silicon wafer with LPCVD after oxidation under the post-fabricated inductor area, which would be finally connected with the derivative elec-

trodes for anodization. Then 150 nm $SiO_2$ was deposited with plasma-enhanced chemical vapour deposition (PECVD). For the fabrication of surface circuits such as integrated inductors, the thicknesses of underpass metal (M1) and the top inductor winding metal (M2) were 70 nm/1$\mu$m Ti/Al and 70 nm/1.5$\mu$m Ti/Al, respectively. PECVD $SiO_2$ (700 nm thick) was deposited between these two metal layers. For isolation structures (70 nm/1$\mu$m Ti/Al metal) in typical G–S–G (ground-signal-ground) structure, the separation between noise-generating pad and noise-sensing pad was designed ranging from 100 to 200$\mu$m. The area of the pad was 80$\mu$m×80$\mu$m. Finally, the passivation layers were deposited to protect the fabricated chip.

The principle of SGPS technique is illustrated in Fig.7, in which Fig.7(a) shows the isolation structure fabricated with conventional 1 polysilicon 2 metal (1P2M) CMOS process. As shown in Fig.7(a), the two pads represent the noise-sensitive parts which need to be isolated under high frequency condition. The highly doped poly-Si layer, which is situated under the isolation area we are concerned with, is connected with the derivate electrodes through vias to generate the necessary electric field for the SGPS process. The selective growth of thick PS can be achieved due to the introduction of the special poly-Si layer. This selective growth of PS begins from the chip backside and grows erectly along the arrow direction as shown in Fig.7(b).

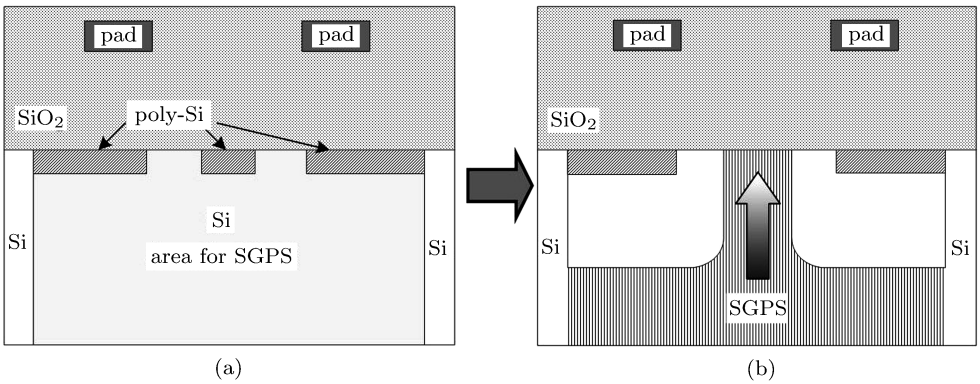



**Fig.7.** The schematic of isolation structure fabricated by SGPS technique. The cross-section of crosstalk isolation structure (a) before and (b) after the formation of SGPS trench.

In order to control the grown thickness of PS, precise DC current power (at least 1$\mu$A resolution was required) was introduced to generate constant electric field and thus to achieve constant growth velocity of SGPS.[11,12] The error of grown thickness could be controlled within 1$\mu$m. After the selective growth of thick PS, the thick PS trench could be formed between the two pads to suppress the high-frequency crosstalk and coupling. In this process, the poly-Si layer in the middle was separated from that on each side, as shown in Fig.7(b), and bias voltage was applied to derivate electrodes relevant to different poly-Si parts. Firstly, the positive voltage was applied to all poly-Si parts and PS grew under all of the poly-Si areas. When the growth of PS continued for a period of time, the bias voltage applied to the middle poly-Si part was kept on while the voltages on both sides were removed. The SGPS kept forming in the middle area until the required isolation structure was achieved as shown in Fig.7(b).

In this work, the thickness of silicon substrate was 400$\mu$m. Anodization was carried out with a current density of 30mA/cm$^2$ in a special mixed solution (40% HF in 99.7% ethanol solution with a volume ratio of 1:4) at room temperature. The growth rate was 1.5$\mu$m/min and the total anodization time was 265min. In our work, the resistivity and effective dielectric constant of the original silicon substrate were 2–5$\Omega$·cm and 11.9 respectively before SGPS process. After the formation of SGPS, the SGPS trench had much higher resistivity ($> 10^6\Omega$·cm) and lower effective dielectric constant $\varepsilon_{\mathrm{PS,eff}} = \varepsilon_{\mathrm{air}} \cdot p + \varepsilon_{\mathrm{Si}}(1-p) = 3.75$, with $p$=0.75 the porosity parameter of our PS layer.[12] These optimizations of substrate parameters resulted in the effective suppression of silicon substrate crosstalk.

Figure 8(a) shows the cross-section SEM image of the fabricated isolation structure after SGPS trench

formation. As shown in Fig.8(a), the distance between the two pads is 100$\mu$m and an about 50$\mu$m wide SGPS trench has been formed between the two pads. The inset at the upper-right shows the high magnification PS pores. Outside the SGPS region, about 50$\mu$m wide bulk silicon under each of the two pads is left, which protects the fabricated pads near silicon surface.

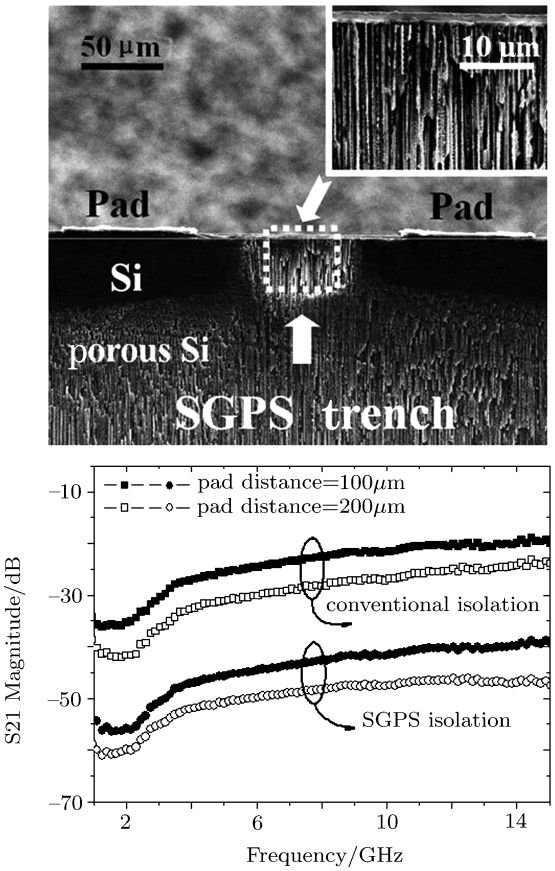



**Fig.8.** (a) The cross section SEM image of fabricated SGPS trench isolation structure and (b) the measured $S_{21}$ parameter of isolation structures.

Two port S-parameters were measured using Agilent E8362B Series network analyser up to 15 GHz. Pad de-embedding was performed using the measured 'open' structure, following the standard procedures. Figure 8(b) shows the typical $S_{21}$ results of isolation structure before and after SGPS process, in which the distances between the noise-generating pad and noise-sensing pad for the two measured results are 100 and 200$\mu$m, respectively. Although the distances between the pads are different, the variation trend of $S_{21}$ parameter is the same. After the thick SGPS trenches are formed, the values of $S_{21}$ are suppressed by at least 20dB. Whether before or after the SGPS process, about 2–5dB difference of $S_{21}$ for the two values of separation of pads is attributed to the strong dependence of the overall crosstalk on the Al pad separation.[7] The comparison between measured results for isolation structures before and after SGPS process further confirms the feasibility of the proposed SGPS technique for RF crosstalk isolation.

## 5. Conclusion

A CMOS-compatible silicon substrate optimization technique is proposed for RF crosstalk isolation. High-performance crosstalk isolation using post-CMOS selectively grown porous silicon technique has been demonstrated and verified. Three-dimension electro-magnetic simulator HFSS has been implemented to validate the obvious effect of the substrate optimization technique. The morphologies and growth condition of PS have been studied in detail to guarantee the feasibility of our technique. Furthermore, the thick SGPS trench for crosstalk isolation is formed after the isolation structures have been fabricated in the standard CMOS process. High-frequency crosstalk isolation can be improved by 20dB using our substrate optimization technique. This technique is of low cost, convenient to be realized and compatible with the standard CMOS process without modifying any step in the process. Besides, this post-CMOS SGPS technique can effectively avoid the contamination and supply a strong mechanical support. In a word, effective crosstalk isolation can be achieved for RF IC applications by using the proposed post-CMOS substrate optimization technique.

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