Vol 17 No 7, July 2008
1674-1056/2008/17(07)/2678-05

Chinese Physics B

© 2008 Chin. Phys. Soc.
and IOP Publishing Ltd

Carriers recombination processes in charge trapping memory cell by simulation

Song Yun-Cheng(宋云成), Liu Xiao-Yan(刘晓彦)†, Du Gang(杜 刚)
Kang Jin-Feng(康晋锋), and Han Ru-Qi(韩汝琦)

Institute of Microelectronics, Peking University, Beijing 100871, *China*

(Received 3 November 2007; revised manuscript received 16 February 2008)

We have evaluated the effects of recombination processes in a charge storage layer, either between trapped electrons and trapped holes or between trapped carriers and free carriers, on charge trapping memory cell's performances by numerical simulation. Recombination is an indispensable mechanism in charge trapping memory. It helps charge convert process between negative and positive charges in the charge storage layer during charge trapping memory programming/erasing operation. It can affect the speed of programming and erasing operations.

Keywords: recombination in insulator, charge trapping memory, programming/erasing characteristic
PACC: 7220J, 7220, 7960E, 7340R

1. Introduction

With the progress of non-volatile semiconductor memory, products featured of high density, high performance and low cost have been put to market. However, conventional non-volatile memory-floating gate flash memory encounters some barriers, either technological or physical.[1−4] The reliability issue is one of the most pressing problems preventing further scaling down of floating gate flash memory cell. As a promising candidate for the next generation of non-volatile semiconductor memory, charge trapping memory (CTM) is inherently immune form severe reliability issues accompanying good CMOS process compatibility.[5−8] Although an increasing integration density of CTM has been achieved in several works recently,[9,10] commercial use still needs great efforts to optimize device performance. To avoid increasing fabrication cost and process complexity, numerical simulation is a powerful tool for understanding the CTM program/erase procedure, its failure mechanism, reliability analysis, prediction, device design and optimization. Spatial distribution of trapped charges in charge storage layer is critical in determining CTM cell's performance. Conventionally, two aspects were considered as the main factors that affect CTM operation: (1) electrons and holes transport in the multiple dielectric layers, including direct/Fowler–Nordheim (F–N) tunnelling, and (2) carriers' trapping/de-trapping processes in charge storage layer, such as capture/thermal excitation, Poole–Frenkel effect (P–F), and thermally assisted tunnelling (ThAT). Several works[11−17] have dedicated to modelling tunnelling, trapping/de-trapping processes for electrons and holes in CTM. However, during the operations of CTM, both electrons and holes can tunnel across the multiple dielectric layers, and both negative and positive charges can be trapped/de-trapped in the charge storage layer. As a result, recombination is an indispensable mechanism which deals with the interaction between electrons and holes. However, few works are concerned with recombination processes in charge trapping memory. Here recombination processes, either between trapped electrons and trapped holes or between trapped carriers and free carriers, are implemented which accompany with other mechanisms in CTM cell to evaluate the effects of recombination mechanism on CTM cell's performance. By using the program we developed,[18,19] the performance of CTM is simulated. The influences of recombination on the programming/erasing operation with various recombination parameters are investigated.

†E-mail: xyliu@ime.pku.edu.cn

2. Model and simulation method

For CTM in NAND application, source bias is always equal to drain bias either in programming (P) or in erasing (E) operation. In other words, channel potential is uniform along the channel during P/E operation. Thus, numerical simulation could only be performed in the direction perpendicular to channel surface. Recombination processes, either between trapped electrons and trapped holes (trap–trap) or between trapped carriers and free carriers (trap–free), are considered. The recombination rate is modelled as a type of carrier capture. The difference between trap–trap recombination and charge trapping is that the former changes the density of both trapped electrons and trapped holes while keeps net trapped charge density fixed, and the latter changes either trapped electron density or trapped hole density. However, trap-free recombination changes the density of trapped charges which are opposite to free carriers while keeps identical trapped charge density fixed.

Figure 1 illustrates the recombination process between free electrons and trapped holes in programming operation. In general, programming operation starts from the condition under which most of the hole trap states occupy the charge storage layer. First, electrons tunnel through tunnelling oxide into charge storage layer (silicon nitride), then they are transported in conduction band. $J(X_n)$ and $J(X_{n+1})$ are the electron currents in silicon nitride layer at the positions X_n and X_{n+1}, respectively. When the electrons are transported in the interval between X_n and X_{n+1}, the electrons could either recombine with trapped holes ΔJ_{re} or be captured by electron traps ΔJ_{c}. The

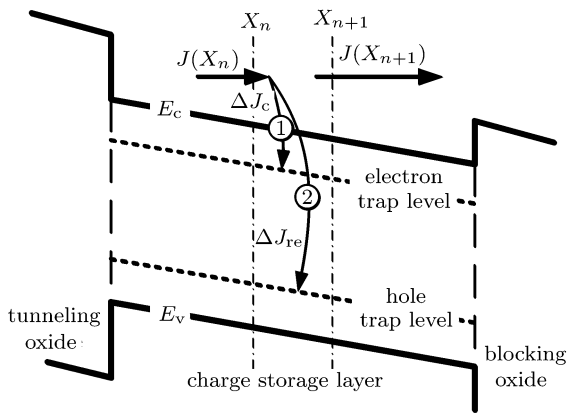


Fig.1. Schematic of trapping and recombination processes in programming operation. Electron current $J(X)$ could be either ①captured by electron traps or ②recombined with trapped holes.

model which could describe both capture and recombination processes can be written as

$$R = \sigma_{\mathrm{c}} v_{\mathrm{th}} n_{\mathrm{e}} (N_{\mathrm{t}} - n_{\mathrm{t}}), \tag{1}$$

where n_{e} is the free carrier density, $(N_{\mathrm{t}} - n_{\mathrm{t}})$ the unoccupied trap density, σ_{c} the effective capture cross-section, and ν_{th} the thermal velocity.

The capture current $\mathrm{d}J_{\mathrm{c}}(x)$ is obtained from Eq.(1)

$$\begin{aligned} \mathrm{d}J_{\mathrm{c}}(x) =& - J(x) \frac{\sigma_{\mathrm{c}} v_{\mathrm{th}} (N_{\mathrm{t}} - n_{\mathrm{t}})}{v} \mathrm{d}x \\ =& - J(x) C_{\mathrm{c}} \mathrm{d}x, \end{aligned} \tag{2}$$

where $C_{\mathrm{c}} = \dfrac{\sigma_{\mathrm{c}} v_{\mathrm{th}} (N_{\mathrm{t}} - n_{\mathrm{t}})}{v}$, $J(x)$ is local current density and ν is carrier drift velocity obtained from Monte Carlo simulator; $\mathrm{d}x$ is a small interval in the perpendicular direction to the channel surface. We assume that all values within $\mathrm{d}x$, such as trapped electron/hole density and carrier drift velocity, are constants. So, solving the differential equation above yields local current $J(x)$

$$J(x) = J(X_n) \exp\left[-C_{\mathrm{c}} (x - X_n)\right]. \tag{3}$$

The recombination rate in silicon nitride can be written as

$$R_{\mathrm{re}} = \sigma_{\mathrm{re}} v_{\mathrm{th}} n_{\mathrm{e}} h_{\mathrm{t}}, \tag{4}$$

where h_{t} is trapped hole density, σ_{re} is effective recombination cross-section.

The recombination current $\mathrm{d}J_{\mathrm{re}}(x)$ is:

$$\mathrm{d}J_{\mathrm{re}}(x) = -J(x) \frac{\sigma_{\mathrm{re}} v_{\mathrm{th}} h_{\mathrm{t}}}{v} \mathrm{d}x = -J(x) C_{\mathrm{re}} \mathrm{d}x, \tag{5}$$

where $C_{\mathrm{re}} = \dfrac{\sigma_{\mathrm{re}} v_{\mathrm{th}} h_{\mathrm{t}}}{v}$. When considering capture and recombination processes together, we have

$$\begin{aligned} \mathrm{d}J(x) =& - J(x) \left[\frac{\sigma_{\mathrm{e}} v_{\mathrm{th}} (N_{\mathrm{t}} - n_{\mathrm{t}})}{v} + \frac{\sigma_{\mathrm{re}} v_{\mathrm{th}} h_{\mathrm{t}}}{v} \right] \mathrm{d}x \\ =& - J(x) \left(C_{\mathrm{c}} + C_{\mathrm{re}}\right) \mathrm{d}x, \\ J(x) =& J(X_n) \exp[-(C_{\mathrm{c}} + C_{\mathrm{re}})(x - X_n)]. \end{aligned} \tag{6}$$

Thus, the recombination current part and the capture current part within an interval from X_n to X_{n+1} can be written as

$$\begin{aligned} \Delta J_{\mathrm{c}}(X) =& - \int_{X_n}^{X_{n+1}} J(x) C_{\mathrm{c}} \mathrm{d}x \\ =& \frac{C_{\mathrm{c}}}{C_{\mathrm{c}} + C_{\mathrm{re}}} \left[J(X_{n+1}) - J(X_n) \right], \\ \Delta J_{\mathrm{re}}(X) =& - \int_{X_n}^{X_{n+1}} J(x) C_{\mathrm{re}} \mathrm{d}x \\ =& \frac{C_{\mathrm{re}}}{C_{\mathrm{c}} + C_{\mathrm{re}}} \left[J(X_{n+1}) - J(X_n) \right] \end{aligned} \tag{7}$$

and the total capture current is

$$\Delta J(X_n) = J(X_{n+1}) - J(X_n). \tag{8}$$

When multiple capture mechanisms in the charge storage layer are included, the carrier selection rule is

$$\Delta J_i = \frac{C_i}{\sum\limits_j C_j} \Delta J. \tag{9}$$

3. Results and discussions

Recombination is an indispensable mechanism in charge trapping memory. It helps charge convert the process between negative and positive charges in charge storage layer during CTM P/E operation. Figure 2 shows the effects of recombination mechanism on programming characteristics. From the figure, it can be seen that the memory window is reduced since no charges were recombined. And the recombination mechanism can hardly influence the speed of programming. After erasing operation, most of the hole trap states are occupied, leaving empty electron trap states. Though these trapped holes could escape from trap states by means of de-trapping processes, high barriers formed by tunnelling oxide and blocking oxide will prevent de-trapped holes from escaping away from gate stack easily. So, without recombination mechanism, almost all trapped holes are untapped. The net charge density is lowered because these remaining trapped holes offset the trapped electron density. As a result, the memory window is reduced. With recombination mechanism, these trapped holes could recombine with electrons rapidly. In other words, the net charge density is larger than that without recombination mechanism. The maximum threshold voltage shift is also larger than that without recombination mechanism. So, recombination mechanism is important for CTM cell's programming window. Since the recombination model parameters such as recombination cross-sections can hardly be measured in the experiment, we simulate the programming characteristic of CTM cell with recombination cross-section $\sigma_{\rm re}$ changing from $10^{-30}{\rm cm}^2$ to $10^{-10}{\rm cm}^2$ to evaluate the influence of model parameter. Figure 3 plots the programming characteristics when $V_{\rm gs}$=18V with different recombination cross-sections. When recombination cross-section $\sigma_{\rm re}$ is smaller than $10^{-28}{\rm cm}^2$, recombination mechanism is hardly effective due to the rather low recombination rate. When recombination cross-section $\sigma_{\rm re}$ is larger than $10^{-20}{\rm cm}^2$, recombination becomes saturated. From the figure, it can be seen that the programming window reduces by about 3.08V when recombination cross-section $\sigma_{\rm re}$ decreases by 8 orders of magnitude, from $10^{-20}{\rm cm}^2$ to $10^{-28}{\rm cm}^2$.

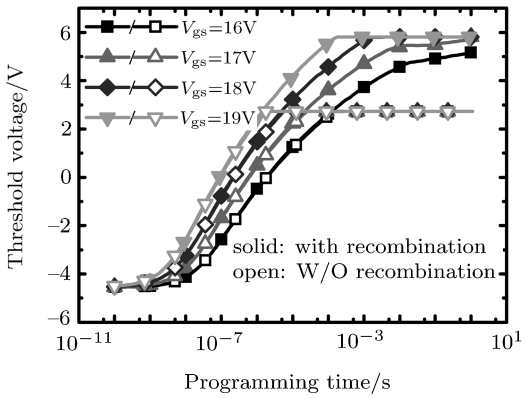


Fig.2. Programming characteristics with or without recombination mechanism at different programming voltages.

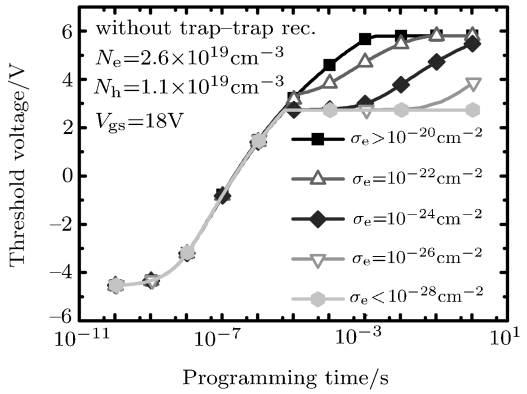


Fig.3. Programming characteristics for $V_{\rm gs}$=18V with different recombination cross-sections.

Effects of recombination on erasing characteristic are shown in Fig.4. Different from programming operation, recombination mechanism does not affect memory window in erasing operation, but can reduce the speed of erasing and change the shape of erasing curves. In consideration of recombination mechanism, trapped electrons could recombine with holes to lower the trapped electron density. The recombination and capture processes will co-exist until all trapped electrons are recombined. So, we obtain the normal erasing characteristics. While without consideration of recombination mechanism, de-trapping becomes the predominant mechanism for trapped electrons. After all the hole traps are occupied, the threshold voltage declines with another slope, as shown in Fig.4. This phenomenon could be understood as the shift of main

erasing mechanism from the hole trapping to the electron de-trapping. In erasing operation, de-trapped rate of trapped electrons is high due to the Poole–Frenkel effect under a high erasing electric field. In addition, electron barrier height is not as high as that of holes. So, in the erasing operation trapped electrons could escape from gate stack relatively easily. Figure 5 plots the erasing characteristics at V_{gs}=–18V for different recombination cross-sections. When recombination cross-section σ_{re} is smaller than 10^{-24}cm^2, recombination can be neglected. For recombination cross-section σ_{re} larger than 10^{-20}cm^2, recombination becomes a predominant mechanism. From the figure, it can be seen that the erasing time increases by about 3.5x when recombination cross-section σ_{re} increases 4 orders of magnitude from 10^{-24}cm^2 to 10^{-20}cm^2. So, recombination mechanism is an important mechanism in determining the CTM cell's erasing performance.

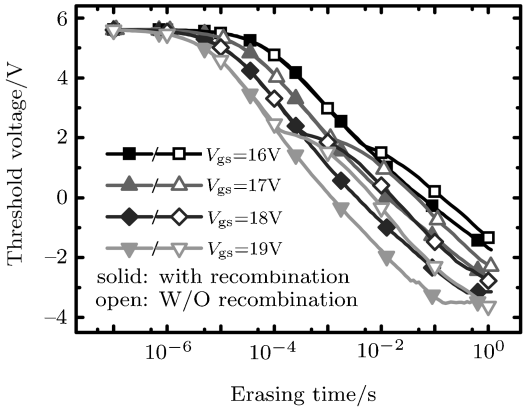


Fig.4. Erasing characteristics with or without recombination mechanism at different erasing voltages.

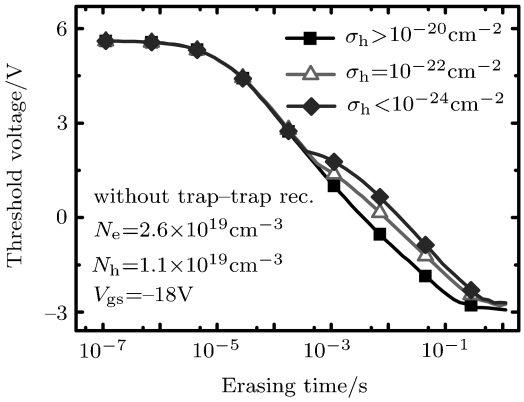


Fig.5. Erasing characteristics for V_{gs}=–18V with different recombination cross-sections.

4. Conclusion

Recombination processes, either between trapped electrons and trapped holes or between trapped carriers and free carriers, have been implemented, accompanied with other essential mechanisms in CTM to evaluate the effects of recombination mechanism on CTM cell's performance for the first time so far as we know. Simulation results reveal that recombination mechanism is important in determining CTM cell's programming/erasing performance. Furthermore, recombination processes are more important than capture process in programming window and erasing speed.

Acknowledgment

This work is supported by Samsung Electronics Co. Ltd and RFDP 20060001050.

References

[1] Belgal H P, Righos N, Kalastirsky I, Peterson J J, Shiner R and Mielke N 2002 *Proc. 40th IEEE-IRPS* p7

[2] Lam C, Sunaga T, Igarashi Y, Ichinose M, Kitamura K, Willets C, Johnson J, Mittl S, White F, Tang H and Chen T C 2000 *IEDM Tech. Dig.* p335

[3] Ielmini D, Spinelli A S, Lacaita A L and Modelli A 2002 *IEEE Electron Devices Lett.* **23** 40

[4] Kuhn P J, Hoefler A, Harp T and Hornung B 2001 *Proc. 39th IEEE-IRPS* p266

[5] Eitan B, Pavan P, Bloom I, Aloni E, Frommer A and Finzi D 2000 *IEEE Electron Device Lett.* **21** 543

[6] White M H 2000 *IEEE Circuits Devices Mag.* **16** 22

[7] Cho M K and Kim D M 2000 *IEEE Electron Device Lett.* **21** 399

[8] Wang T, Tsai W J, Gu S H, Chan C T, Yeh C C, Zous N K, Lu T C, Pan S and Lu C Y 2003 *IEDM Tech. Dig.*

p169

[9] Park Y, Choi J, Kang C, Lee C, Shin Y, Choi B, Kim J, Jeon S, Sel J, Park J, Choi K, Yoo J, Sim J and Kim K 2006 *Proc. IEDM* p29

[10] Kwak D, Park J, Kim K, Yim Y, Ahn S, Park Y, Kim J, Jeong W, Kim J, Park M, Yoo B, Song S, Kim H, Sim J, Kwon S, Hwang B, Park H, Kim S, Lee Y, Shin H, Yim N, Lee K, Kim M, Lee Y, Park J, Park S, Jung J and Kim K 2007 *Proc. Symp. on VLSI Tech. Dig.* p12

[11] McWhorter P J, Miller S L and Dellin T A 1990 *J. Appl. Phys.* **68** 1902

[12] Wang Y and Marvin H White 2005 *Solid-State Electronics* **49** 97

[13] Manzini S 1987 *J. Appl. Phys.* **52** 3278

[14] Parker G H and Mead C A 1969 *Appl. Phys. Lett.* **14** 21

[15] Wu J, Register L F and Rosenbaum E 1999 *Proc. IPRS* p298

[16] Andreas Schenk and Gernot Heiser 1997 *J. Appl. Phys.* **81** 7900

[17] Fitting H J, Cornet N, Touzin M, Goeuriot D, Guerret-Piecourt C and Treheux D 2007 *J. Euro. Ceram. Soc.* **27** 3977

[18] Song Y C, Xia Z L, Yang J F, Du G, Kang J F, Han R Q and Liu X Y 2006 *Proc. ICSICT* p772

[19] Song Y C, Du G, Yang J F, Jin R, Han R Q , Lee K H and Liu X Y 2007 *Proc. SISPAD* p345