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Fast-scale border collision bifurcation in SEPIC power factor pre-regulators

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In this paper we report a kind of fast-scale instability occurring in the single-ended primary inductance converter (SEPIC) power factor pre-regulator, which is designed to operate in discontinuous conduction mode. Main results are given by exact cycle-by-cycle computer simulations as well as theoretical analysis. It is found that the instability phenomenon manifests itself as a fast-scale bifurcation at the switching period, which implies the occurrence of border collision bifurcation, or is related to the transition of the regular operating mode of the SEPIC. According to the theoretical analysis and simulation results, the effects of parameters on system stability, and the locations of the bifurcation points are confirmed. Moreover, the effects of such an instability on power factor and switching stress are also discussed. Finally, the occurrence of the asymmetric bifurcation locations is investigated. The results show that this work provides a convenient means of predicting stability boundaries which can facilitate the selection of the practical parameters.

Keywords: fast-scale instability, border collision bifurcation, SEPIC power factor pre-regulator, discontinuous current mode

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1. Introduction

Recently, intensive investigations have been carried out on various kinds of bifurcation behaviours in switching power converters.[1−3] In DC–DC converters the input voltage is constant, so we need to consider only the variation in the duty ratio and the switching frequency.[4,5] In contrast, the input voltage of a power factor pre-regulator (PFP) is periodic with low frequency, and the nonlinear dynamics of the PFP depends not only on the duty ratio and the switching frequency, but also on the periodicity of the line voltage. Consequently, unlike DC–DC converters, the power factor pre-regulator is a kind of more complicated nonlinear system and various nonlinear behaviours may occur for improper choice of system parameters. In fact, nonlinear dynamics occurring in low-order power factor pre-regulators have been widely reported.[6−10] The research of such irregular behaviours can motivate the requirement for a deeper understanding of the corresponding dynamical behaviours and a further exploration of some new operation modes. Moreover, such knowledge would be used not only to improve system performances, but also to find new fields of application.[11,12]

Compared to the several known solutions to implementing a PFP, i.e. Boost and Flyback, the single-ended primary inductance converter (SEPIC) has the desirable features of its continuous input current, ripple current reduction, and wide output voltage range.[13] As a result, for low-power applications, the SEPIC working as a PFP in discontinuous current mode (DCM) is a cost-effective solution, which is widely used in power factor correction.[14−18] However, previous studies have mainly focused on the steady-state design and the control aspects of this kind of circuits. Unfortunately, based on simple linear techniques, the pioneering works have failed to predict essentially nonlinear phenomena. The detailed nonlinear dynamics, so far, have not been thoroughly pursued.

In this paper, we report the fast-scale border collision bifurcation observed in a single-phase SEPIC PFP operating in DCM. We will show that, with improper choice of system parameters, the converter can undergo fast-scale instability for some intervals of time during the line period. Specifically, power factor can be drastically degraded and switching stress

can be promptly increased when the instability phenomenon occurs. This is important in practice because it may seriously affect system performances or damage switching devices. Moreover, analytical equations and design curves will be given to facilitate the design of practical circuit parameters for maintaining stable operation.

2. System description

Figure 1 shows the SEPIC PFP, with the equivalent-series-resistance of the inductors included. As a DCM-PFP, the system just needs a voltage feedback loop. The controller uses a simple pulse width modulation (PWM) scheme, in which a control voltage $v_{\rm e}$ is compared with a periodic ramp signal to generate a PWM signal to drive switch S. The ramp signal is given by $V_{\rm ramp} = V_{\rm L} + (V_{\rm U} - V_{\rm L})\left(\dfrac{t}{T_{\rm s}} \bmod 1\right)$, where $V_{\rm L}$ and $V_{\rm U}$ are the lower and upper voltage limits of $V_{\rm ramp}$, and $T_{\rm s}$ is the switching period. As is common to all power electronic systems, the switching pre-regulator is a multi-structural system with its circuit topology varying according to the states of the switch. Normally, the switch S is turned on when $v_{\rm e} > V_{\rm ramp}$, and turned off otherwise. The control voltage $v_{\rm e}$ can be derived from the voltage feedback loop,

$$v_{\rm e} = K' V_{\rm ref} - K v_2, \tag{1}$$

where $V_{\rm ref}$ is the desired steady-state output voltage, $K = R_{\rm f}/R_x$ is the feedback gain of the controller, and $K' = 1 + R_{\rm f}(1/R_x + 1/R_y)$. The aim of the PFP is to operate as a voltage follower[19] to give a nearly constant output voltage. Meanwhile, the input current naturally tracks the input sinusoidal voltage profile, and hence the power factor is kept approximately unity.

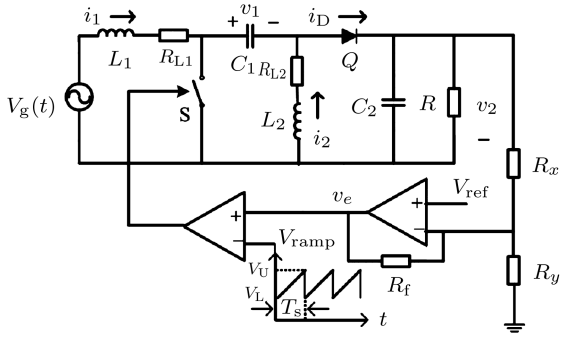


Fig.1. Schematic of SEPIC PFP with voltage control loop.

In Fig.1, there are three possible configurations, depending on the state of the switch S and the diode Q. The third configuration, where both S and Q are at their off-state (freewheeling stage), appears only when the sum of the two inductor currents $i_{\rm m}(i_{\rm m} = i_1 + i_2)$ reaches zero. In this case, the system is said to operate in a discontinuous current mode (DCM). Otherwise, if the condition $i_{\rm m} > 0$ always holds, only the first two configurations exist in a switching period. In that case, the system operates in a continuous current mode (CCM), and the diode Q always conducts whenever the switch S is turned off.

When the SEPIC PFP operates in DCM during a switching period, we denote the first two time durations of these three states by $t_{\rm n}$ and $t_{\rm d}$, respectively. Then, the exact state equation corresponding to each switch state can be given as follows:

$$\dot{\boldsymbol{x}} = \begin{cases} \boldsymbol{A}_1\boldsymbol{x} + \boldsymbol{B}_1 v_{\rm g}(t), & nT_{\rm s} \le t < nT_{\rm s} + t_{\rm n}; \\ \boldsymbol{A}_2\boldsymbol{x} + \boldsymbol{B}_2 v_{\rm g}(t), & nT_{\rm s} + t_{\rm n} \le t < nT_{\rm s} + t_{\rm n} + t_{\rm d}; \\ \boldsymbol{A}_3\boldsymbol{x} + \boldsymbol{B}_3 v_{\rm g}(t), & nT_{\rm s} + t_{\rm n} + t_{\rm d} \le t \le (n+1)T_{\rm s}, \end{cases} \tag{2}$$

where $\boldsymbol{x} = [i_1, i_2, v_1, v_2]^{\rm T}$, $v_{\rm g}(t) = V_{\rm g}\,|\sin(\omega t)|$ is the input sinusoidal voltage, $V_{\rm g}$ is the input line peak voltage, ω is the line angular frequency, and the system matrices are

$$\boldsymbol{A}_1 = \begin{bmatrix} -\dfrac{R_{L1}}{L_1} & 0 & 0 & 0 \\ 0 & -\dfrac{R_{L2}}{L_2} & \dfrac{1}{L_2} & 0 \\ 0 & -\dfrac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\dfrac{1}{RC_2} \end{bmatrix}, \quad \boldsymbol{A}_2 = \begin{bmatrix} -\dfrac{R_{L1}}{L_1} & 0 & -\dfrac{1}{L_1} & -\dfrac{1}{L_1} \\ 0 & -\dfrac{R_{L2}}{L_2} & 0 & -\dfrac{1}{L_2} \\ \dfrac{1}{C_1} & 0 & 0 & 0 \\ \dfrac{1}{C_2} & \dfrac{1}{C_2} & 0 & -\dfrac{1}{RC_2} \end{bmatrix}, \quad \boldsymbol{A}_3 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \dfrac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\dfrac{1}{RC_2} \end{bmatrix},$$

$$\boldsymbol{B}_1 = \boldsymbol{B}_2 = \left[\begin{array}{cccc} \dfrac{1}{L_1} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}}, \quad \boldsymbol{B}_3 = \left[\begin{array}{cccc} 0 & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}}.$$

Based on the design criterion presented in Ref.[19], to operate in DCM, inequality $L_{\mathrm{e}} < RT_{\mathrm{s}}/(4M^2)$ must hold, where $L_{\mathrm{e}} = L_1L_2/(L_1 + L_2)$, $M = v_2/V_{\mathrm{g}}$. Moreover, to avoid the input current oscillations at every half-line period and to guarantee almost a constant voltage during a switching period, the design criterion of C_1 is also given as $\omega_{\mathrm{s}} > \omega_{\mathrm{r}} > \omega$, where $\omega_{\mathrm{r}} = 1/\sqrt{C_1(L_1 + L_2)}$ and $\omega_{\mathrm{s}} = 2\pi/T_{\mathrm{s}}$.[19]

3. Bifurcation behaviour from circuit simulations

Here, based on the exact state equations, we will carry out a series of computer simulations to make an initial evaluation of the possible bifurcation phenomena. We follow the above mentioned design criteria to choose the circuit parameters. Meanwhile, we restrict our attention to the case when the load R varies, while the other parameters are fixed. Essentially, for each set of parameters, cycle-by-cycle time-domain waveforms are generated by solving the appropriate linear equation in a sub-interval of time, according to different switching states.[10] After the transient period, we capture the steady-state time-domain waveforms of the system. Since the waveforms are repeated for every $[k\pi, (k + 1)\pi]$ interval, for all integers k, we shall henceforth restrict our analysis within a half-line period. Moreover, the phase portrait is constructed between the input current and the intermediate capacitor voltage to explain the stability from nonlinear viewpoint. The parameters used in the simulations are: $V_{\mathrm{g}} = 180\,\mathrm{V}$, $L_1 = 6.4\,\mathrm{mH}$, $L_2 = 206\,\mu\mathrm{H}$, $R_{\mathrm{L1}} = 2.2\,\Omega$, $R_{\mathrm{L2}} = 1.2\,\Omega$, $C_1 = 0.4\,\mu\mathrm{F}$, $C_2 = 100\,\mu\mathrm{F}$, $V_{\mathrm{ref}} = 1.6\,\mathrm{V}$, $V_{\mathrm{L}} = 0\,\mathrm{V}$, $V_{\mathrm{U}} = 3\,\mathrm{V}$, $K = 0.016$, $K' = 1.4$, $T_{\mathrm{s}} = 25\,\mu\mathrm{s}$ and $\omega = 314\,\mathrm{rad/s}$.

3.1. Normal operation

When the value of R is relatively large, e.g. $140\,\Omega$, the SEPIC PFP can work in normal operation. Simulation results are shown in Fig.2. We clearly see that in a half-line period, the fundamental input current i_1 naturally follows the input voltage, the intermediate capacitor voltage v_1 follows the input voltage profile, and the output voltage v_2 is approximately a constant. The time-domain waveform of the current i_{m} clearly illustrates that the operating mode of the system is a DCM operation within a half-line period. To observe the change clearly in dynamical behaviour, we collect the sampled peak values of i_1 and the corresponding values of v_1 during each switching period in the steady state. Figure 2(f) shows the phase portrait of the peak values of i_1 and v_1. Moreover, the switch duty ratio D_1 and the diode duty ratio D_2 are also shown in Fig.2(g), where D_1 remains nearly a constant while D_2 varies with ωt in a half-line period. From Fig.2(g), we can clearly see that $D_1 + D_2 < 1$ always holds for a half-line period.

3.2. Onset of fast-scale border collision bifurcation

We now gradually decrease the load R. When the resistor is adjusted to $78\,\Omega$, normal operation is no longer possible, and the system begins to exhibit a kind of fast-scale instability at the switching period. In Figs.3(a)–3(d) the time-domain waveforms of i_1, i_2, v_1 and v_2 are shown separately, where the distorted response can be seen. In order to see the operating mode of the system, the time-domain waveform of i_{m} is given in Fig.3(e). We can observe that the system stops operating globally in DCM within a half-line period, i.e., when there are some switching periods during which the current i_{m} no longer reaches zero value, that is, the system operates in CCM during these switching periods. After that, the system works in DCM again and this operating mode lasts to the end of the half-line period. Thus, we say that the system undergoes a DCM–CCM–DCM transitions within a half-line period. Essentially, these transitions of operating mode, such as DCM to CCM and CCM to DCM, are related to the change of topological sequence. In Ref.[20], based on symbolic method, Tse *et al* have pointed out that the change of topological sequence indicates the border collision bifurcation. According to that, we know that the system here suffers from a nonsmooth border collision bifurcation. Figure 3(f) shows the phase portrait of the peak values of i_1 and

v_1. In order to see the critical bifurcation points more clearly, the switch duty ratio D_1 and the diode duty ratio D_2 are shown in Fig.3(g), where the two critical points, namely θ_1 and θ_2, are located. Between the two points, we can see that the condition $D_1 + D_2 = 1$ holds.

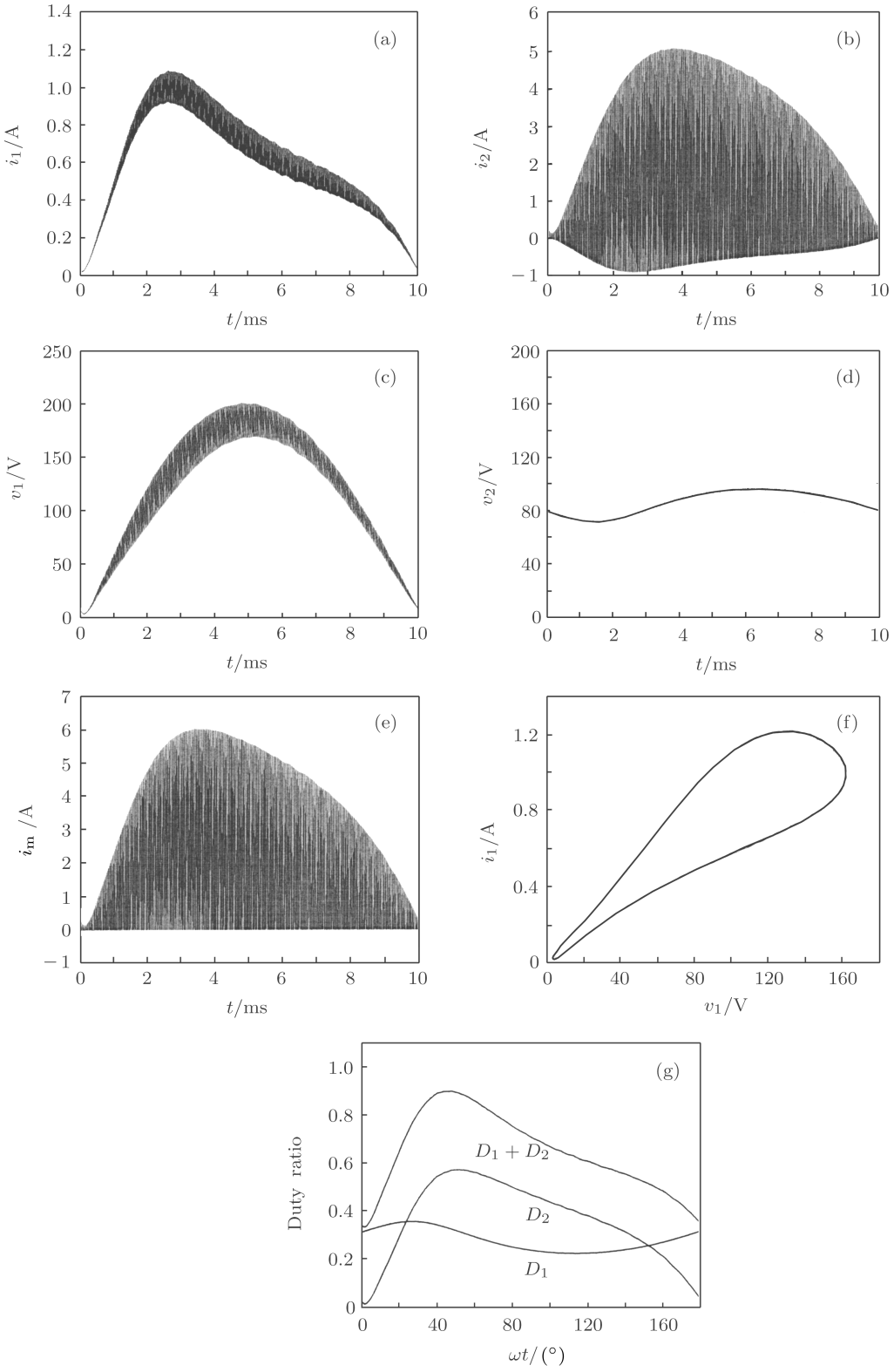


Fig.2. Simulations for $R = 140\,\Omega$. (a)–(e) Time-domain waveforms of i_1, i_2, v_1, v_2 and i_m; (f) phase portrait of the peak values of i_1 and v_1; (g) waveforms of D_1, D_2, $D_1 + D_2$.

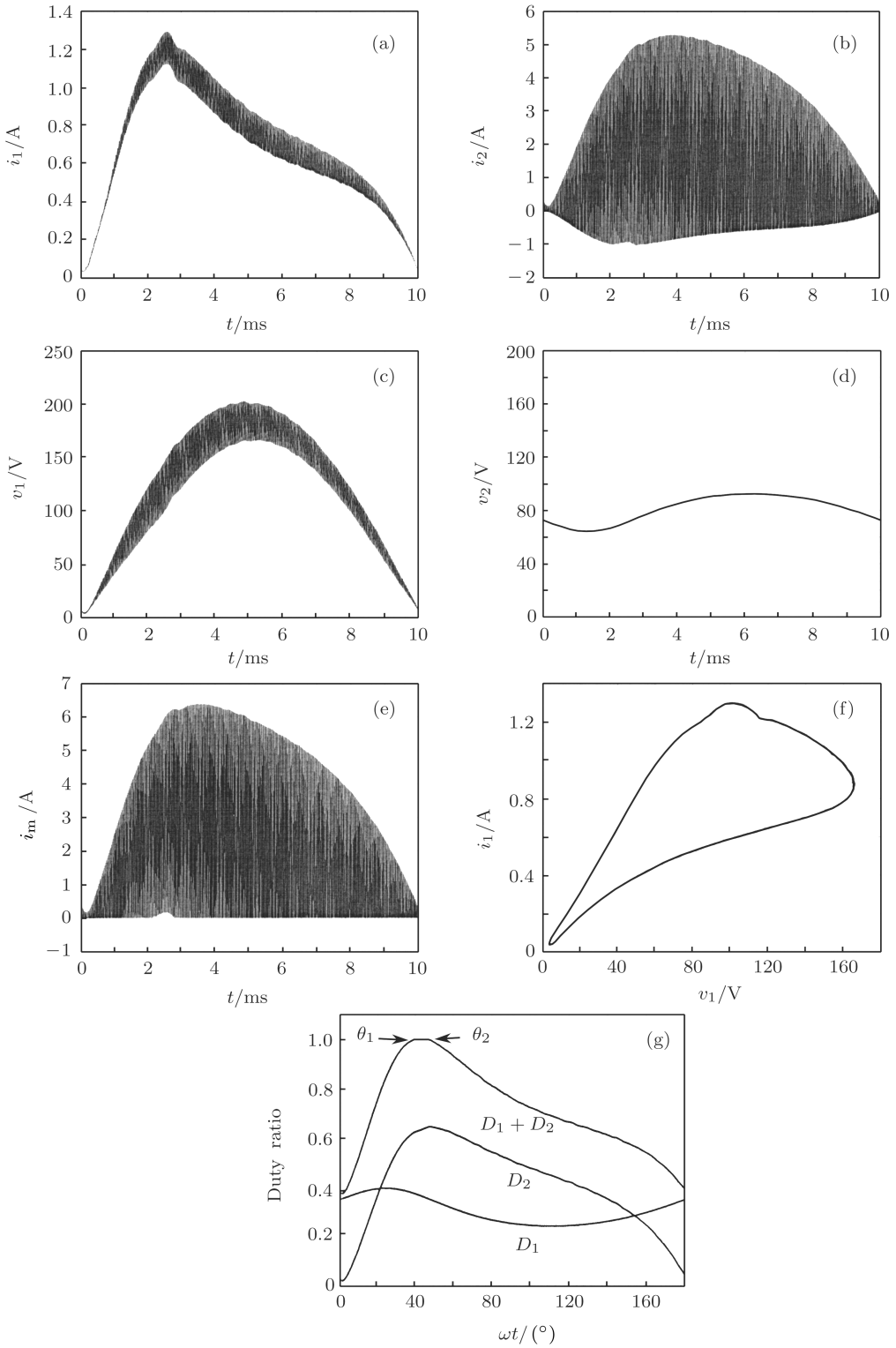


Fig.3. Simulations for $R = 78\,\Omega$. (a)–(e) Time-domain waveforms of i_1, i_2, v_1, v_2 and i_m; (f) phase portrait of the peak values of i_1 and v_1; (g) waveforms of D_1, D_2, $D_1 + D_2$.

3.3. 'Deep' fast-scale border collision bifurcation

When R is decreased to $60\,\Omega$, the fast-scale instability becomes more serious. As shown in Figs.4(a)–4(d), we can observe that the time-domain waveforms of i_1, i_2, v_1 and v_2 are distorted seriously. The time-domain waveform of i_m in a half-line period is also given in Fig.4(e). We can clearly see that the system stops operating globally in DCM and suffers from a

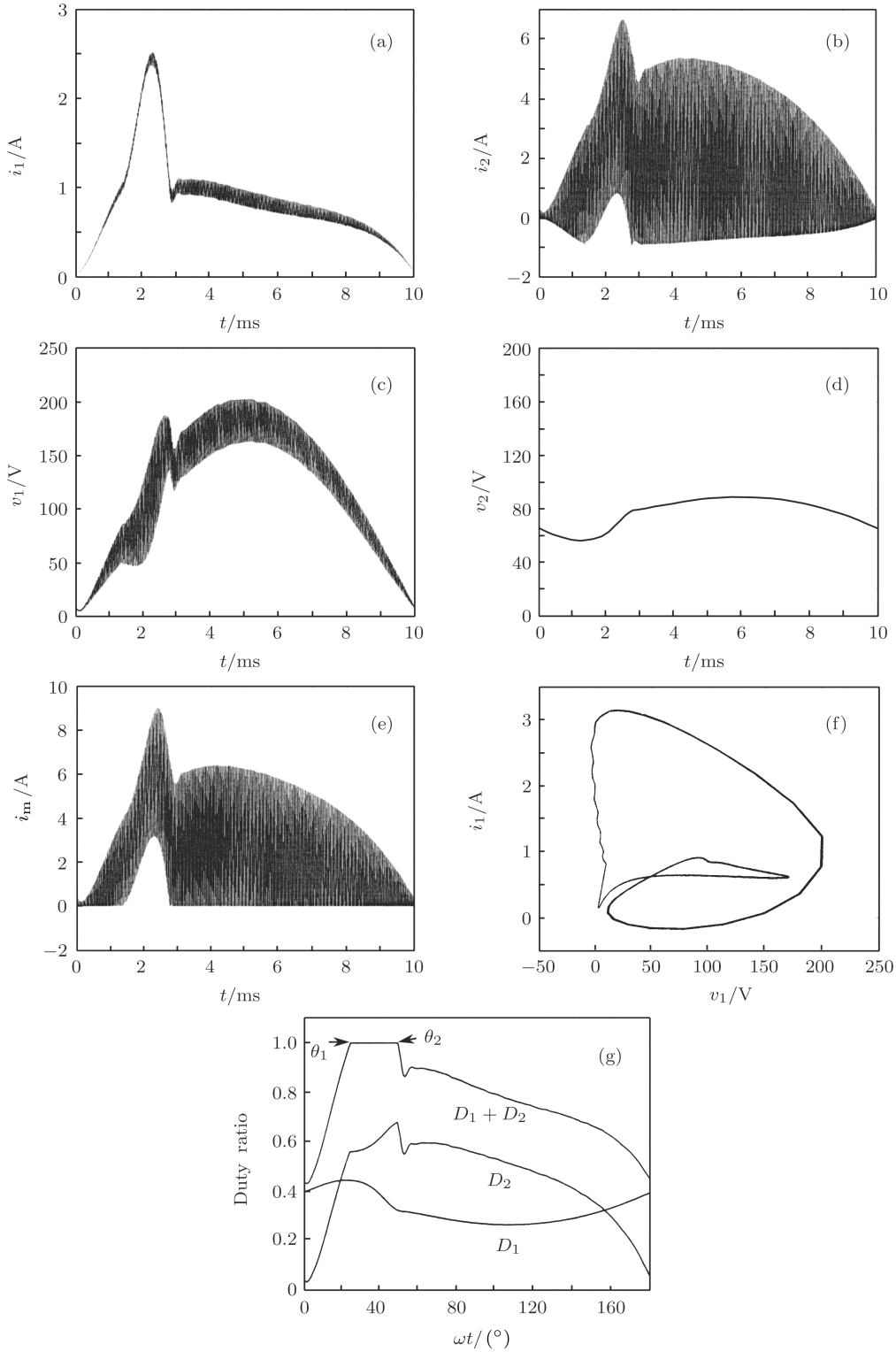


Fig.4. Simulations for $R = 60\,\Omega$. (a)–(e) Time-domain waveforms of i_1, i_2, v_1, v_2 and i_m; (f) phase portrait of the peak values of i_1 and v_1; (g) waveforms of D_1, D_2, $D_1 + D_2$.

DCM–CCM–DCM transitions in a half-line period. Figure 4(f) shows the phase portrait of the peak values of i_1 and v_1. Obviously, we see that the phase portraits under this condition are rather unlike the results shown in Fig.2(f). Finally, the switch duty ratio D_1 and the diode duty ratio D_2 are also shown in Fig.4(g). From Fig.4(g), we can see that between the critical points θ_1 and θ_2, the condition $D_1+D_2 = 1$ al-

ways holds. Moreover, we can observe that the SEPIC PFP keeps the expected DCM operation in intervals corresponding to $\omega t < \theta_1$ and $\omega t > \theta_2$.

3.4. Effects of fast-scale border collision bifurcation on power factor and switching stress

In this subsection, we will discuss the effects of fast-scale border collision bifurcation on power factor (PF) and switching stress. Figure 5 shows the change of the PF as R decreases. When the system works in normal operation (Fig.2), we can derive PF = 0.93, which is adequate for most practical applications. Detailed simulations show that under normal operation the PF always keeps PF > 0.86. However, the fast-scale border collision bifurcation appears and the system fails to maintain the expected normal operation as R further decreases. When the system starts to undergo border collision bifurcation (Fig.3), the PF remains quite large (about 0.86). Meanwhile, the operating mode is changed from globally DCM to DCM–CCM–DCM. After that, the PF falls drastically from 0.86 to 0.65 as R decreases from 78 to 60 Ω. It is clearly seen here that the change of operating mode can cause fast-scale border collision bifurcation which will lead to drastically degradation of power factor correction (PFC) performance.

Likewise, Fig.6 shows the current stress imposing on the switch S. We can see that the fast-scale instability problem imposes higher current stress on the switching device. In practice, we should make efforts to avoid such instability.

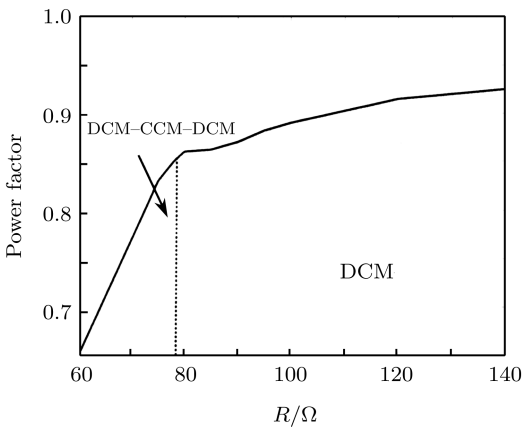


Fig.5. Power factor of the SEPIC PFP as R varies.

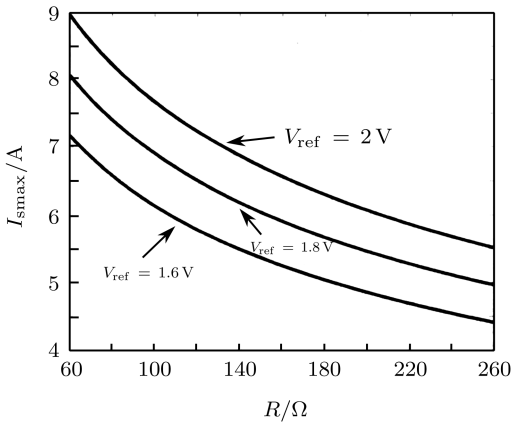


Fig.6. Current stress on power switch versus R.

4. Analysis of bifurcation behaviour

In this section we will confirm the above simulation findings by analysing the bifurcation behaviour of the SEPIC PFP.

4.1. Derivation of the duty ratio

The SEPIC PFP has more than one stable equilibrium point in a half-line period, since the input voltage in PFP is continuously changing at the line frequency. In this case, the quasi-static analysis approach[21] can be used to discuss the dynamics involved. Under the quasi-static approximation condition, we denote the input voltage in the ith switching period by a constant E. To simplify our analysis, we ignore the effects of the equivalent-series-resistance of the inductors and assume almost a constant voltage v_1 in a switching period. According to the operating mechanism of the SEPIC PFP, when the system operates in DCM in the ith switching period, we have

$$\Delta I_{\rm m} = \frac{E}{L_1} D_1 T_{\rm s} + \frac{v_1}{L_2} D_1 T_{\rm s}, \tag{3}$$

where $\Delta I_{\rm m}$ and D_1 are the peak-to-average ripple of the current $i_{\rm m}$ and the switch duty ratio in the ith switching period for a half-line period, respectively. Assuming very low ripple in the intermediate capacitor C_1 and by taking average value over one switching period, we have $v_1 = E$. Hence, Eq.(3) becomes

$$\Delta I_{\rm m} = \frac{E}{L_{\rm e}} D_1 T_{\rm s}. \tag{4}$$

On the other hand, the average current $I_{\rm m}$ and I_D can be expressed respectively as

$$I_{\rm m} = \frac{1}{2}\Delta I_{\rm m}, \tag{5}$$

and

$$I_{\rm D} = D_2 I_{\rm m} = \frac{v_2}{r}, \tag{6}$$

where D_2 is the diode duty ratio, and r is the equivalent load 'seen' by the converter. Assuming unity input PF and 100% efficiency, the following equation relating r and R within a line period is immediately clear,[22]

$$r = \frac{R}{2\sin^2(\omega t)}. \tag{7}$$

From Eqs.(4)–(7) we can obtain the following expression

$$D_1 = M\sqrt{\tau}, \tag{8}$$

where $\tau = \dfrac{4L_{\rm e}}{RT_{\rm s}}$. Fixing the parameters related to Eq.(8), we realize that the switch duty ratio D_1 in the ith switching period is essentially independent of the value of ωt and remains a constant. Thus, the switch duty ratio maintains constant in a half-line period, and is also denoted by D_1. Furthermore, applying volt-second balance[23] to the DCM SEPIC PFP, we can readily obtain

$$D_2 = \frac{|\sin(\omega t)|}{M} D_1 = \sqrt{\tau}\,|\sin(\omega t)|\,. \tag{9}$$

From Eq.(9), we know D_2 is characterized by a slowly varying sinusoidal function in each half-line period. In order to make a distinction, when the SEPIC PFP operates in CCM, the switch duty ratio is denoted by D. It is easy to obtain $\dfrac{E}{L_1}DT_{\rm s} = \dfrac{v_2}{L_1}(1-D)T_{\rm s}$ and $v_2 = \dfrac{M}{|\sin(\omega t)|}E$. Solution for D yields

$$D = \frac{M}{M + |\sin(\omega t)|}. \tag{10}$$

From the above analysis, we can see clearly that when the SEPIC PFP operates in CCM, the switch duty ratio D varies continuously with ωt in each half-line period. In contrast, when the system works in DCM, in each half-line period the switch duty ratio D_1 remains constant and D_2 varies in a sinusoidal fashion. Meanwhile, D_1 is proportional to the inverse square root of the load resistance R while the other parameters are given as constants.

4.2. Critical condition for operating in DCM

It is known that a PWM DC–DC converter operates in DCM when $D_1 + D_2 < 1$ and the boundary between CCM and DCM is defined as $D_1 + D_2 = 1$.[24] Likewise, when the SEPIC PFP operates globally in DCM, the following inequality must always hold for a half-line period

$$D_1 + D_2 < 1. \tag{11}$$

On the other hand, from Eq.(8) we know D_1 keeps constant during each half-line period. Then, according to the operating mechanism of the SEPIC PFP, the control voltage $v_{\rm e}$ satisfies

$$v_{\rm e} = D_1(V_{\rm U} - V_{\rm L}) = D_1 V_{\rm M}. \tag{12}$$

Thus, the dc voltage conversion ratio M can be calculated by equating Eq.(1) and Eq.(12). And the resulting output voltage of the closed-loop system is of the form

$$v_2 = \frac{K' V_{\rm ref}}{KV_{\rm g} + V_{\rm M}\sqrt{\tau}} V_{\rm g}. \tag{13}$$

Solution for R from Eqs.(8)–(9), (11) and (13), noting that $\sin(\omega t) \le 1$, yields the critical condition for the load resistance

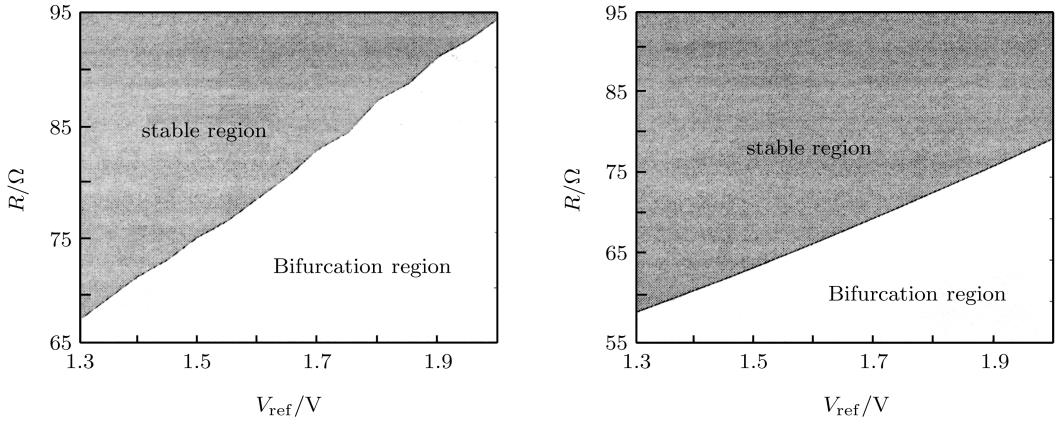
$$R_{\rm m} = \frac{2L_{\rm e}f_{\rm s}}{(KV_{\rm g})^2}\left[2KV_{\rm g}V_{\rm M} + a\left(a + \sqrt{a^2 + 4KV_{\rm g}V_{\rm M}}\right)\right], \tag{14}$$

where $a = KV_{\rm g} - V_{\rm M} + K'V_{\rm ref}$. Hence, if R satisfies $R > R_{\rm m}$, the DCM operation can be guaranteed for all ωt. For example, in the prototype of Fig.1, choosing the same parameters as used in Section 3, we can obtain $R_{\rm m} \approx 67\,\Omega$.

However, the theoretical condition (14) is considerably different from the simulation results where $R_{\rm m} \approx 78\,\Omega$. To answer this question, we will come back to the preconditions for obtaining Eq.(14). In the foregoing subsection, in order to derive the switch duty ratio D_1 and the diode duty ratio D_2, we have assumed that the SEPIC PFP is under ideal conditions, that is, unity input PF and 100% efficiency. This means that the effects of the equivalent-series-resistance of the inductors on system performance are ignored in theoretical analysis. However, system performance degradations are inevitable in practice. In addition, using the quasi-static method to simulate the operation of the PFP may lead to unavoidable errors. Essentially, we can emulate the 'real' operating

modes of the PFP in terms of cycle-by-cycle time-domain simulations. Subsequently, the simulation results can be more accurate.

Of engineering importance is the stable region of the system. From the foregoing simulation results, we know that the stability of the system is always maintained during globally DCM operation. However, for a certain parameter, such as the reference voltage $V_{\rm ref}$, there exists a critical value of load resistance R, below which the system exhibits the fast-scale border collision bifurcation and above which the system maintains itself in a stable state. Consequently, the critical parameter values define a stability boundary dividing the parameter spaces of R and $V_{\rm ref}$ in order to facilitate the practical design, as shown in Fig.7(a). In addition, based on the formula (14) the theoretical stability boundary in parameter space of $V_{\rm ref}$ versus R is also presented in Fig.7(b). Compared to the theoretical result, the simulation result has less stable operation range. This is because we have ignored the effects of the equivalent-series-resistance of the inductors in the above theoretical analysis.



(a) simulation result (b) theoretical result

Fig.7. Stability boundary in the parameter space of R versus $V_{\rm ref}$.

From these two figures we see clearly that when R decreases or $V_{\rm ref}$ increases, the fast-scale border collision bifurcations are more likely to occur.

4.3. Location of the critical bifurcation points

As the simulation results indicate, the system starts with DCM operating mode at the beginning of each half-line period and stops suddenly at some switching period when the condition

$$D_1 + D_2 = 1 \tag{15}$$

satisfies. Crossing the boundary of the stable region, the system bifurcates into a new regime of dynamical behaviour. Therefore, by inspecting the boundary between CCM and DCM at which the fast-scale border collision bifurcations occur, the critical phase angles can be found from Eq.(15) as

$$\theta_{\rm m} = \sin^{-1} x, \quad \theta_{\rm m}{}' = 180^\circ - \theta_{\rm m}, \tag{16}$$

where x is given by $x = \dfrac{KT_{\rm s}V_{\rm g} - 2a\sqrt{L_{\rm e}RT_{\rm s}}}{4L_{\rm e}V_{\rm M}}$, and $\theta_{\rm m}$ is restricted to the range $0 < \theta_{\rm m} \leq 90^\circ$. It is necessary to point out that Eq.(16) is only valid in a limited load range.

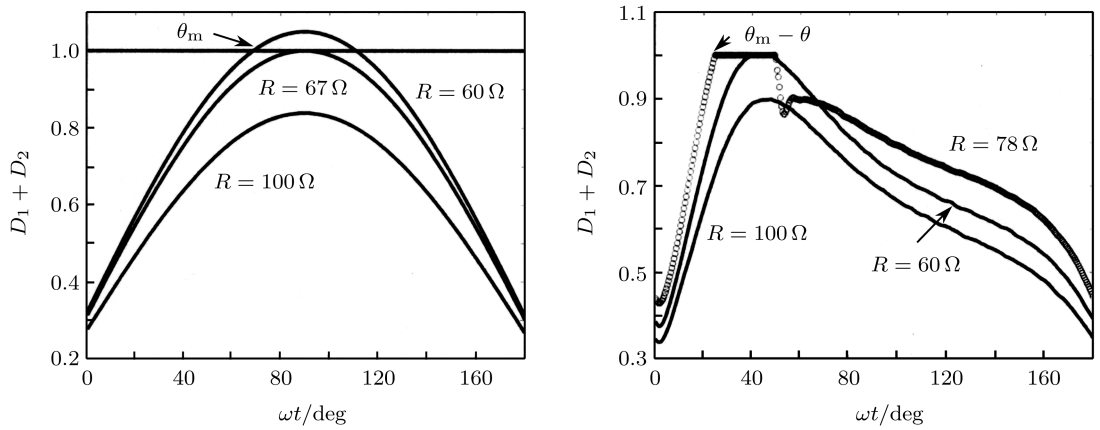
Using Eq.(16), we now readily arrive at some useful conclusion concerning the behaviour of the system under different load resistances R. Figure 8(a) shows three typical curves corresponding to the normal DCM operation ($R = 100\,\Omega$), critical DCM operation ($R = 67\,\Omega$, onset of border collision bifurcation) and CCM operation ($R = 60\,\Omega$, 'deep' border collision bifurcation), respectively. Hence, the border collision bifurcation can be characterized by the presence of the critical phase angle $\theta_{\rm m}$ in each quarter of the line period. When $\theta_{\rm m}$ reaches its maximum value, the SEPIC PFP then operates in CCM at $\omega t = 90^\circ$, which implies the onset of the fast-scale instability.

From Fig.8(a), we know that the two phase angles are completely symmetrical with respect to $\omega t = 90^\circ$ and achieve the maximum value. Obviously, this does not agree with the simulation result shown in Fig.8(b). Such discrepancy is due to the fact that we calculate

the critical phase angle $\theta_{\rm m}$ in the case of the unit PF. However, in practice the PF is always below 1. Now let $\theta = \cos^{-1}(\mathrm{PF})$, $\theta_{\rm m} \in [0, 90^\circ]$, we can derive the modified condition

$$\theta_{\rm m} - \theta < \omega t < 180^\circ - \theta_{\rm m} - \theta, \qquad (17)$$

which defines the boundaries of the bifurcation regions, as shown in Fig.8(b). As $\theta_{\rm m}-\theta$ and $180^\circ-\theta_{\rm m}-\theta$ get closer to each other, the unstable interval diminishes. Using Eq.(17), we can understand thoroughly the fact that the foregoing simulated bifurcation points are asymmetric with respect to $\omega t = 90^\circ$.



(a) theoretical result (b) simulation result

Fig.8. Critical phase angles for border collision bifurcation.

5. Conclusion

In this paper, the nonlinear dynamics of the DCM SEPIC PFP have been studied. We have reported the results from exact cycle-by-cycle circuit simulations, and revealed a kind of fast-scale instability at the switching period. Our focus is put on the effects of variation of a few chosen system parameters. Essentially, the occurrence of the phenomena is due to border collision bifurcation. It is further shown that when such an instability occurs, the system may inevitably undergo DCM–CCM–DCM transitions in a half-line period. Moreover, the occurrence of asymmetric bifurcation locations, and the effects of parameters on system stabilities are investigated. It is necessary to point out that the instability phenomena occurring in SEPIC PFP are completely different from those of low-order power factor pre-regulators. Finally, the effects of the instability on power factor and switching stress are discussed. Since the instability phenomena may greatly affect the system performances, the results obtained here are useful for engineers to diagnose the causes of such instability when it occurs in the circuits.

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