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Influence of spacer layer thickness on the current-voltage characteristics of pseudomorphic AlAs/$In_{0.53}Ga_{0.47}As$/InAs resonant tunnelling diodes

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This paper investigates the dependence of current–voltage characteristics of AlAs/$In_{0.53}Ga_{0.47}As$/InAs resonant tunnelling diodes (RTDs) on spacer layer thickness. It finds that the peak and the valley current density J in the negative differential resistance (NDR) region depends strongly on the thickness of the spacer layer. The measured peak to valley current ratio of RTDs studied here is shown to improve while the current density through RTDs decreases with increasing spacer layer thickness below a critical value.

Keywords: resonant tunnelling diode, molecular beam epitaxy
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1. Introduction

Since Tsu and Esaki[1] first proposed resonant tunnelling diode (RTD) structures in 1973, many researches have been done to improve the negative differential resistance (NDR) characteristics of GaAs/$Al_xGa_{1-x}As$ structures,[2] AlAs/GaAs structures[3,4] grown on GaAs and InAlAs/InGaAs structures[5] lattice-matched to InP. InP-based resonant tunnelling devices have the potential to be key devices in the near future and have been intensively studied in recent years, because their unique NDR feature makes it possible to reduce the complexity and increase the operating speed of integrated circuits.[6,7] A pseudomorphic AlAs/$In_{0.53}Ga_{0.47}As$/InAs RTD structure with an InAs sub-well in the InGaAs well layer has been proposed for reducing and controlling the energy level without degrading NDR characteristics. This structure has been used in the fabrication of monolithically integrated circuits.[8,9] In this work, we report on the effect of increasing spacer layer thickness in the current–voltage ($I-V$) characteristics of AlAs/$In_{0.53}Ga_{0.47}As$/InAs RTDs based InP substrates grown by molecular beam epitaxy (MBE).

2. Experiments

The RTDs were grown in a Vecoo GENII MBE system. Polished (100) Fe-doped semi-insulating 2-inch InP substrates were used in this work. The symmetric RTD structure used in this work consists of a 300 nm n^+-InGaAs emitter-contact layer ($5\times10^{18}\,cm^{-3}$ Si), a 100 nm n-InGaAs emitter layer ($2\times10^{17}\,cm^{-3}$ Si), a variable i-InGaAs spacer (L_N), an undoped double-barrier structure with a 1.2-nm InGaAs/1.2 nm InAs/1.2 nm InGaAs strained well sandwiched by 2.83 nm AlAs barriers, a variable i-InGaAs spacer, a 100 nm n-InGaAs collector layer ($2\times10^{17}\,cm^{-3}$ Si), a 100 nm n^+-InGaAs collector-contact layer ($5\times10^{18}\,cm^{-3}$ Si) (Fig.1). Thin, undoped InGaAs spacer layers were introduced on both sides of barriers to examine the effect of Si doping profile on $I-V$ characteristics of RTD structure. The thickness of spacer layer was varied from 0 nm to 5 nm. The details of material growth and device fabrication have been described elsewhere.[10,11]RTD devices with contact areas (emitter) ranging from $2\mu m\times3\mu m$ to $10\mu m\times10\mu m$ were fabricated by conventional wet-etching and lift-off processes. Nonalloyed ohmic contacts were made by using Cr/Au for the top and bot-

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tom contacts.

100 nm n^+ $In_{0.53}Ga_{0.47}As$ collector contact
100 nm $In_{0.53}Ga_{0.47}As$ collector
variable $In_{0.53}Ga_{0.47}As$ -spacer
2.83 nm AlAs
1.2 nm $In_{0.53}Ga_{0.47}As$
11.2 nm InAs
1.2 nm $In_{0.53}Ga_{0.47}As$
2.83 nm AlAs
variable $In_{0.53}Ga_{0.47}As$ -spacer
100 nm $In_{0.53}Ga_{0.47}As$ emitter
300 nm n^+ $In_{0.53}Ga_{0.47}As$ emitter contact
semi-insulating InP substrate

Fig.1. Schematic cross section of an $In_{0.53}Ga_{0.47}As$/AlAs/InAs RTD.

3. Results and discussion

With L_N=3 nm a peak current density (J_p) of 4 kA/cm^2 and a good peak-to-valley current ratio (PVCR) of 20 were obtained for one diode at room temperature. Fig.2 shows the PVCR (J_p/J_v) of RTDs measured at room temperature as a function of the thickness L_N of the spacer layer. Here, positive (negative) bias means that the surface electrode is positively (negatively) biased with respect to the substrate electrode and electrons flow from the substrate to the surface (from the surface to the substrate) through resonant tunnelling barrier (RTB) structure. In the positive bias case, the PVCR drastically improved with increasing thickness L_N, while in the negative bias case improvement was less remarkable. When L_N is in excess of

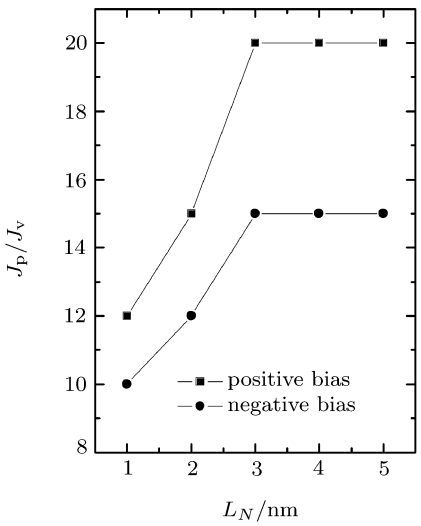


Fig.2. PVCR J_p/J_v in the NDR region of RTDs as a function of spacer layer thickness L_N.

3 nm, the PVCR at the positive and negative bias is inclined to saturation. Fig.3 shows the L_N dependence of the peak current density (J_p) and the valley current density (J_v). J_p and J_v decrease drastically with increasing L_N at the positive bias.

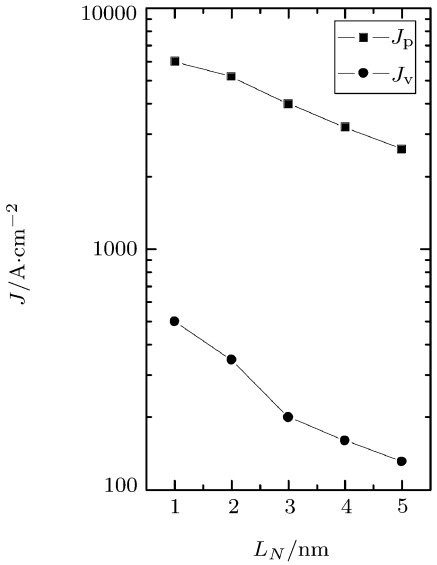


Fig.3. Peak and valley current densities J of RTDs as a function of spacer layer thickness L_N.

Increasing the spacer layer thickness results in higher series resistance which shifts to the peak and valley voltage (V_p, V_v) to higher values. The smaller PVCR in the 1 nm spacer RTDs is believed to be due to ionized impurity scattering from the emitter and collector regions. Such scattering decreases the peak transmission probability and broadens the resonance energy, thus lowering the PVCR.[12] Another possible cause for the smaller PVCR is that high current density implies a high concentration of electrons accumulated in the quantum well of RTDs, which reduces the PVCR due to the higher probability of electron–electron scattering and larger amount of band bending within RTB. A thick spacer layer requires a two step electron transport process. The first step is thermionic emission and/or tunnelling across the emitter spacer layer, followed by tunnelling through the rest of the double-barrier structure as the second step. With the increase of the spacer layer width, thermionic emission over the emitter spacer layer barrier becomes the rate-limiting transport process leading to suppression of the resonant tunnelling current and leak current (thermionic emission electron over the double-barrier and photon assisted electron tunnelling across the double-barrier). The experiments show that with the increase of the spacer width J_p and J_v are largely

suppressed below a critical spacer width. Above the critical spacer width the PVCRs with different spacer width are comparable. This implies that increasing spacer thickness in excess of the critical value PVCR of RTDs has not been improved. The exact design of the optimum spacer layer thickness for maximum PVCR is complicated by the compromise between improved performance due to the reduction in impurity scattering and decreased performance through suppression of the tunnelling current due to the spacer barrier.

4. Conclusion

In summary, we have investigated the effect of a InGaAs spacer layer on the $I-V$ characteristics of an AlAs/$In_{0.53}Ga_{0.47}As$/InAs RTDs. We have found that both J_p and J_v in the NDR region can be controlled by changing the spacer thickness. By adjusting the spacer layer thickness properly, we obtained a high PVCR of 20 at room temperature.

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