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Formation of high density TiN nanocrystals and its application in non-volatile memories

Li Xue-Lin(李学林)[a)c)†], Feng Shun-Shan(冯顺山)[b)], and Chen Guo-Guang(陈国光)[a)]

[a)] *North University of China, Taiyuan* 030051, *China*
[b)] *Beijing Institute of Technology, Beijing* 100081, *China*
[c)] *Shandong Machinery (Group) Co. Ltd, Zibo* 255201, *China*

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Non-volatile memory based on TiN nanocrystal (TiN–NC) charge storage nodes embedded in SiO_2 has been fabricated and its electrical properties have been measured. It was found that the density and size distribution of TiN–NCs can be controlled by annealing temperature. The formation of well separated crystalline TiN nano-dots with an average size of 5 nm is confirmed by transmission electron microscopy and x-ray diffraction. x-ray photoelectron spectroscopy confirms the existence of a transition layer of TiN_xO_y/SiON oxide between TiN–NC and SiO_2, which reduces the barrier height of tunnel oxide and thereby enhances programming/erasing speed. The memory device shows a memory window of 2.5 V and an endurance cycle throughout 10^5. Its charging mechanism, which is interpreted from the analysis of programming speed (dV_{th}/dt) and the gate leakage versus voltage characteristics (I_g vs V_g), has been explained by direct tunnelling for tunnel oxide and Fowler–Nordheim tunnelling for control oxide at programming voltages lower than 9V, and by Fowler–Nordheim tunnelling for both the oxides at programming voltages higher than 9 V.

Keywords: TiN nanocrystal, size, density, non-volatile memory application
PACC: 6146, 7220, 7340L, 7340Q

1. Introduction

The needs for high-density and high-performance nonvolatile memory are rapidly increasing in the application of mobile information devices. Discrete nanocrystals (NCs) embedded in SiO_2-based nonvolatile memory (NVM) devices have received considerable attention due to the suppression of lateral migration of electrons along the floating gate.[1−4] Devices could be less vulnerable from the local oxide defects compared with conventional continuous floating gate nonvolatile memories and thus have advantages in retention, reliability, and scalability. To achieve a fast programming/erasing (P/E) speed and an extended duration of data retention, it is desirable to engineer NVM gate stacks, that is, to meet both the requirements of a large barrier height in the retention mode and a small barrier height in the P/E mode. This trade off can be made possible by the work function engineering of the metal-NCs.[3] Titanium nitride (TiN) material is a promising metal–NC candidate because of its midgap work function (4.6 eV) which makes a deeper quantum well compared with the electron affinity of Si or Ge. Moreover, titanium nitride (TiN) belongs to the family of refractory transition metal nitrides having the physical properties of high melting point, thermodynamic stability, high hardness, and high electrical conductivity.[5] In complementary metal–oxide–semiconductor (CMOS) technology, a TiN diffusion barrier has been employed between the metal electrode and the gate oxide due to its excellent electrical properties and structural stability. Particularly, it shows good adhesion to SiO_2, as implied by Gibb's free energy change ($\Delta_f G^0$) of formation for Ti–O (−883.2 kJ/mol).[6] Moreover, TiN metal in the form of NC embedded in dielectric is thermodynamically stable up to 1000 °C and is unlikely to cause unwanted contamination upon integration into NVM devices.[7] In the CMOS process, TiN is used as a barrier for plug material and interconnect metal, but it forms a continuous layer because of large thickness (10–50 nm) and low temperature treatment (usually < 800 °C). More uniform and smaller sized dot formation is made possible by controlling the wetted layer thickness of metal up to the size which is the same as or smaller than the nucleation site spacing. Beyond this critical thickness, interlocked islands between NCs are formed after rapid thermal annealing

†E-mail: mrc017@hotmail.com

(RTA).[3] However, the mechanism of NC formation is unknown for determining nanocrystal size, density, and uniformity, which are responsible for data retention and memory window.

This article addresses the fabrication of NVM MOSFET (metal oxide semiconductor field effect transistor) devices with TiN–NCs embedded in SiO_2 in high-density and good electrical performances. We have developed the process to form the high-density TiN–NCs using an e-beam evaporator, and investigated the properties of TiN–NCs on SiO_2. Furthermore, the bulk material properties and interfacial properties of NCs have been studied to understand the charging /discharging properties of NVM devices.

2. Formation of TiN–NCs

A 2.8 nm thick SiO_2 (used as a tunnel oxide in NVM device) was first thermally grown at 875 °C on a p-type (100) silicon wafer. Subsequently, a 2 nm thick TiN layer was deposited on SiO_2 by e-beam evaporation using a TiN target and annealed at different temperatures to study their effects on the shape and density of NCs. Annealing was performed in vacuum for 10 s in the temperature range from 800 to 900 °C. TiN–NCs were then capped with a 9 nm thick SiO_2 (used as a control oxide in NVM device) formed by low-pressure chemical vapour deposition (LPCVD) at 600°C using a tetraethoxysilane (TEOS, $Si(OC_2H_5)_4$) precursor. Thicknesses of the tunnel and control oxides were determined by an elliposometer.

The TiN–NCs embedded in SiO_2 has been confirmed by atomic force microscopy (AFM), high-resolution transmission electron microscopy (HRTEM) and x-ray diffraction (XRD) analysis. The estimated average density and size of NCs are shown in Fig.1. The strong dependence of nanocrystal size and density on the annealing temperature has been observed for uncapped TiN–NCs from the AFM analysis. The as-deposited TiN film at room temperature appears as a continuous layer even after annealing at 800°C, while the NC formation is hardly observed. It is believed that the thermal energy provided for the nucleation of TiN is insufficient. The size and density of the NCs are increased when the annealing temperature increases from 800 to 900°C. The average height and density of NCs are found to be 5 nm and $1.5\times10^{12}\,cm^{-2}$ at an annealing temperature of 850°C, and 4.4 nm and $1.3\times10^{11}\,cm^{-2}$ at 800°C. It is understood that, at 850 °C stress built in the TiN layer during the deposition is relaxed compared with that when annealing at 800°C.[2,3] However, at 900 °C the increase of the average size of NCs leading to agglomeration is observed. That is to say, the growing NCs are merged with adjacent ones (known as Oswald ripening). As a result, NC density deceases.

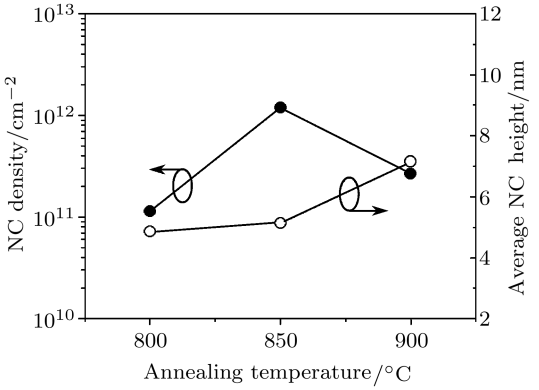


Fig.1. The density and average height of TiN–NCs observed from AFM surface morphology in SiO_2 as functions of annealing temperature.

A cross-sectional TEM picture for TiN–NCs annealed at 850°C for 10 s demonstrates the well separated NC islands. Nanostructures shown from the dark image with lattice fringes (indicated by empty circles) have the crystalline phases embedded in an amorphous matrix. NCs have various orientations and are slightly different in size and shape. The NC density estimated from the NC mean size of 5 nm and the distance between adjacent NCs of 3–4 nm match well with the result obtained from AFM. In the NC memory device, high NC density is required to increase $\Delta V_{\rm th}$ and reduce the fail probability. However, increased NC density leads to reduced distances between NCs and thereby to lowered immunity to stress-induced leakage current (SILC). Recently, Gusmeroli *et al*[8] proposed that an optimum NC density to meet the requirements of 65 nm NAND NCs memory device was $\sim 10^{12}\,cm^{-2}$, based on their simulation results using the 3D Monte Carlo method which took into account of the trade off between the uniformity of NCs and the SILC immunity. Since our result obtained under the condition of 850 °C annealing for 2 nm thick TiN is close to the proposed optimum NC density, it is chosen as the baseline condition for the fabrication of our test memory devices.

The XRD analysis was performed on the SiO_2/TiN–NCs/SiO_2/Si stacked structure, as shown in Fig.2. It is found from this result that the major

peaks detected at 2θ = 36°C, 42°C, 63.5°C, 76.5 °C originate from the reflections from the (111), (200),

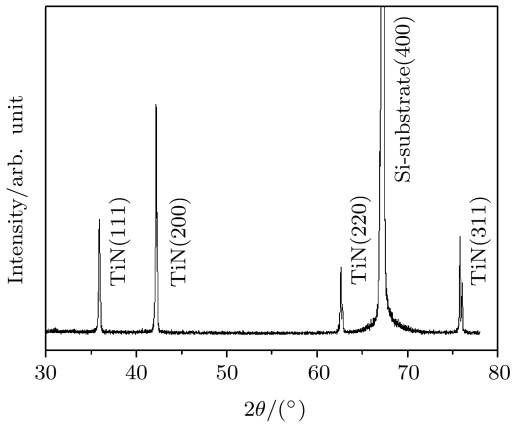


Fig.2. XRD results of TiN–NCs embedded in SiO_2. The presence of TiN–NCs is demonstrated.

(220) and (311) planes of TiN–NCs, respectively. This result indicates that TiN exists as pure NCs and exhibits the polycrystalline property which corresponds to the TEM results. The orientation [200] of TiN–NCs is the preferred orientation. It is understood that TiN–NCs are highly textured along the [100] growth direction of Si, from which the (200) peak intensity is stronger compared with the other peaks. The overall energy of the film, which is transferred during deposition, is the summation of the strain energy and the surface energy. The surface energy is $4.0 \times 10^{-4}\,\mathrm{J\cdot cm^{-2}}$ for (111), $2.6 \times 10^{-4}\,\mathrm{J\cdot cm^{-2}}$ for (110) and $2.3 \times 10^{-4}\,\mathrm{J\cdot cm^{-2}}$ for (100).[9] That is, the lowest surface energy plane is (200), while the lowest strain energy plane is (111). In this experiment, most NCs align in the [200] preferred orientation on the lowest surface energy plane with the NaCl-type structure.[10]

In order to investigate the chemical property of materials in the TiN–NCs/SiO_2/Si stack, XPS surface profiling for Ti 2p, N 1s, O 1s, and Si 2p peaks was performed, the results of which are shown in Fig.3. The Ti 2p spectra are characterized by the doublets of Ti $2p_{1/2}$ and Ti $2p_{3/2}$, resulting from spin-orbit coupling. In this work, considering that the integrated intensity of the Ti $2p_{1/2}$ peak relative to that of the Ti $2p_{3/2}$ peak is equal to the spin-orbit multiplicity of 0.5 and the spin-orbit splitting is assumed to be ∼5.9 eV for all of the states; we can deconvolute the Ti 2p spectra into Ti–N and Ti–N–O bonds. The deconvoluted results of Ti 2p spectra are also shown in Fig.3(a), where the Ti $2p_{3/2}$ peaks are observed at 455.6 and

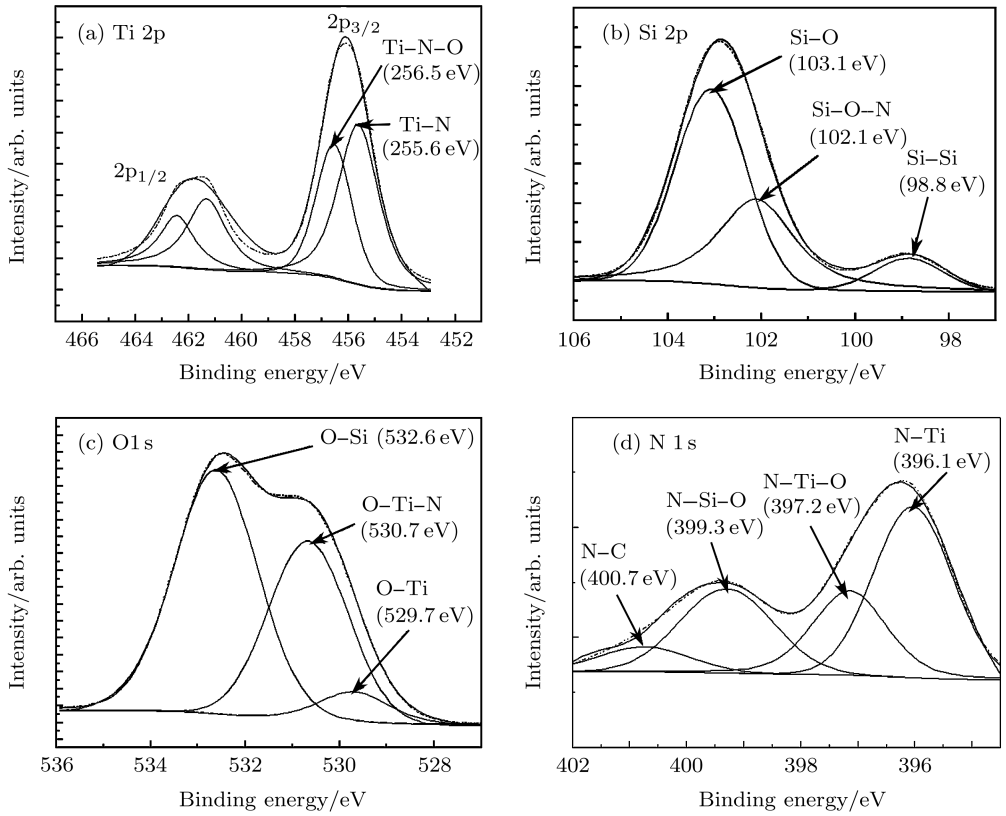


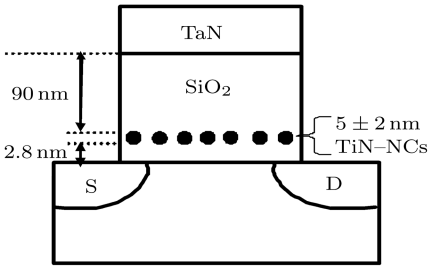
Fig.3. XPS spectra showing (a) Ti 2p, (b) Si 2p, (c) O 1s and (d) N 1s of TiN–NCs in SiO_2. Deconvolution results confirm the formation of TiON/SiON transition layer between TiN-NC and SiO_2 dielectric.

456.5 eV due to Ti–N and Ti–N–O bonds which correspond to TiN and TiN_xO_y, respectively. This can be attributed to the chemical reaction between the TiN layer and the SiO_2 layer due to the low free energy change of oxidation for Ti–O or attributed to the oxygen traps at the TiN grain boundary due to the availability of many dangling bonds at grain boundaries.[11] Based on the results of XRD, TEM and XPS, it can be considered that TiN_xO_y layer has been formed at the interface of TiN–NCs. According to the deconvolution for Si 2p spectra in Fig.3(b), the peaks at binding energies of 103.1, 102.1 and 98.8 eV for the binding states of Si–O, Si–O–N and Si–Si can be obtained. Deconvoluted O 1s spectra in Fig.3(c) indicate the presence of O–Si (532.6 eV), O–Ti–N (530.7 eV) and O–Ti (529.7 eV) peaks which originate from SiO_2, TiN_xO_y and TiO_2, respectively. However, the area under the TiO_2 peak is very small compared with other peaks. The Gibb's free energy change ($\Delta_f G^0$) of TiN is -308.1 kJ/mole whereas that of SiO_2 is -849.8 kJ/mole,[6] indicating that SiO_2 is thermodynamically more stable. TiN is oxidized upon the exposure to the oxygen and air during the experiment. The reaction, $TiN+O_2 \rightarrow TiO_2 + 1/2N_2$, is thermodynamically favourable: $\Delta_f G^0 = -581.9$ kJ/mole.[12]

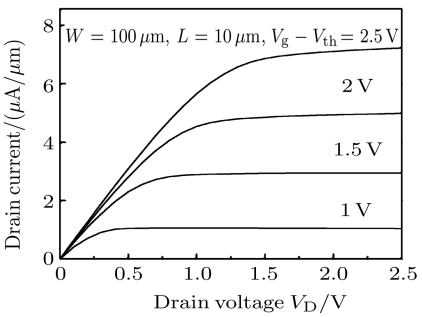
The major peaks in N 1s spectra (396.1 eV for N–Ti bond and 397.2 eV for N–Ti–O bond) are attributed to TiN and TiN_xO_y, respectively, as shown in Fig.3(d). In addition, the N–Si–O bonds at 399.3 eV and the N–C bonds at 400.7 eV are also detected. The result for the N–Si–O bonds is also consistent with that from the Si 2p spectra in Fig.3(b), and this confirms the presence of SiO_xN_y transition layer at the interface of the SiO_2 and NCs. In this process of NCs formation on SiO_2, a transition layer of TiON/SiON has been formed between TiN–NC and SiO_2 matrix. This transition layer can be beneficial to the memory window and P/E speed, which can be explained from the model proposed by Joo *et al.*[13] It is expected that the barrier height of tunnel oxide is reduced during the erasing operation due to the transition layer, resulting in the improvement of erasing speed. The barrier height of the control oxide is also reduced, but the decrease of programming speed may be little since the thickness of the control oxide is much larger than that of tunnel oxide. On the other hand, back tunnelling of electrons from trapping nodes to control gate can be reduced due to the deeper quantum well formed by midgap work function of TiN–NC compared with that of Si–NC, and the thicker control oxide. As a result, the improvement of programming speed is anticipated in our fabricated NVM device.

3. NVM device fabrication using TiN–NCs

N-MOSFET devices with the TaN/SiO_2/TiN–NCs/SiO_2/p-Si stacked structure have been fabricated to demonstrate NVM performance using the NCs formation method, as shown in Fig.4(a). TaN layer was deposited by sputtering using a Ta target in an Ar+N_2 ambient, and patterned as a gate electrode, followed by ion implantation (As^+, 1×10^{15} cm^{-2}, 70 keV), RTP activation annealing at 950°C for 30 s to form the source/drain regions and, finally forming gas annealing at 400°C. Tantalum nitride (TaN) is selected as the gate material, instead of n^+ polysilicon, because the midgap work function of TaN has been reported to contribute to an enlarged memory window by reducing electron injection from the gate through the control oxide during erasing operation.[14] Moreover, it is well known that the TaN metal has an excellent thermal stability, which can be maintained over 1000°C, and a strong resistance against oxidation. The well behaved $I_d - V_d$ characteristics of n-MOS transistor with TiN–NCs embedded in SiO_2 are shown in Fig.4(b). A



(a)



(b)

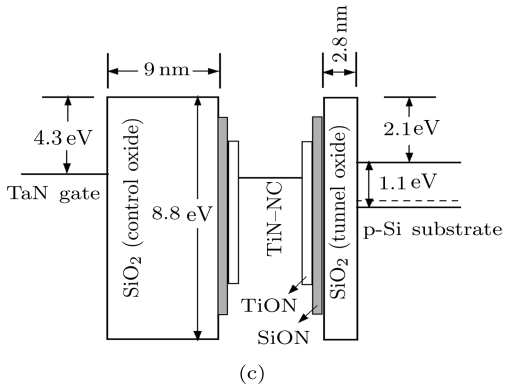


Fig.4. (a) Schematic diagram for the cross-section of the memory device structure, (b) the well behaved $I_d - V_d$ characteristics and (c) energy band diagram at flat band condition of n-MOS transistor memory device with TiN–NCs embedded in SiO_2.

possible energy band diagram at flat band condition is drawn by taking into consideration the transition layers, as shown in Fig.4(c). Control device was fabricated under the same process condition without TiN layer, for comparison with the memory device so as to confirm the effect of TiN–NCs used as charge storage nodes.

4. Programming and erasing efficiency of TiN–NCs based NVM device

The programming/erasing (P/E) properties of the fabricated 100 μm/10 μm n-MOSFET devices with and without TiN–NCs using the Fowler–Nordheim (F–N) method are shown in Fig.5 for various applied voltages (0 to $\pm$12 V) and pulse duration (10^{-6} to 1 s). The threshold voltage change increases with increasing programming or erasing voltage in TiN–NCs based devices, as shown in Fig.5(a). In contrast, without NCs no shift is observed in n-MOSFET devices in the entire range of P/E applied voltage. Therefore, it is clearly proven that TiN–NCs and peripheral Ti-based oxide are the charge storage media in the memory device.

Programming and erasing transient characteristics of the memory device is shown in Fig.5(b). The memory window is found to be 2.6 V from the P/E voltage of $\pm$12 V which is close to the International Technology Roadmap for Semiconductors (ITRS) 2006 requirement of memory window ($\sim$ 3 V).[15] The programming speed determined by dV_{th}/dt, is found to be about the same value $\sim$0.3 V/s for all the programming voltages. However, the starting point to attain the maximum programming speed is clearly observed at about 1 ms for programming voltages of 5–9 V, while it is at about 1 μs for programming voltages of 10–12 V. Saturation starts between 10–100 ms for the programming voltage range

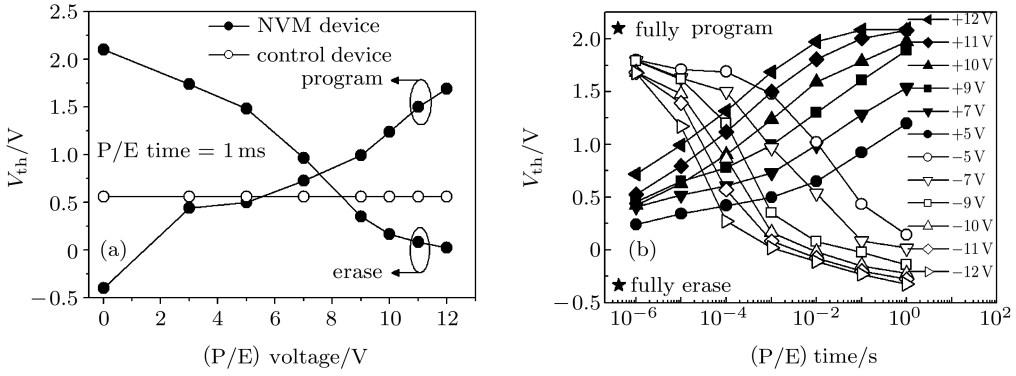


Fig.5. (a) Threshold voltage shift of the TiN–NC memory (NVM) device as a function of P/E voltages for 1 ms, compared with the control device. Nanocrystals and peripheral Ti-based oxide play the key role for charge storage in the memory device. (b) Transient P/E characteristics.

of 10–12 V. This suggests that the charge tunnelling mechanisms are different between low and high voltage programming modes. The programming current versus the programming voltage characteristic of the memory and control devices shown in Fig.6(a) supports the change in the tunnelling mechanism. A plot of $\ln(J/E^2)$ vs E^{-1}, as shown in Fig.6(b), confirms that the F–N tunnelling (current density, $J_{\mathrm{F-N}} = \alpha E^2 \exp(-\beta/E)$, where E is the applied electric field, $\alpha = 1.5 \times 10^{-6}(m_{\mathrm{e}}/m_{\mathrm{o}})(1/\varphi_{\mathrm{b}})/$ $(\mathrm{A/V^2})$, $\beta = 6.8 \times 10^7 (m_{\mathrm{o}}/m_{\mathrm{e}})^{1/2} \varphi_{\mathrm{b}}^{3/2}/(\mathrm{V/cm})$[16]) is the dominant mechanism in both the devices during programming at a higher field (> 9 V) applied to the tunnel and control oxides. The barrier height (φ_{b}) in the SiO_2/Si interface derived from the slope of the F–N plot for positive applied field is found to be 2.5 eV for the memory device and 3.0 eV for control device, when the effective mass of electron (m_{e}) in SiO_2 is assumed to be $0.39\,m_0$, whereas the barrier height calculated from the gate current of the control device (3.0 eV) is comparable to the reported result.[16] It is understood that the discrepancy in the barrier heights for memory device estimated by the electrical measurement originates from the transition layer.

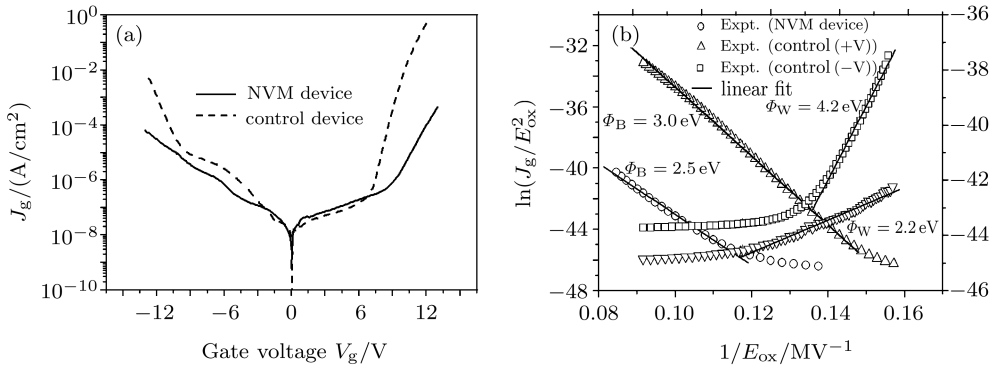


Fig.6. (a) Programming current versus programming voltage and (b) $\ln(J/E^2)$ vs E^{-1} for both the TiN–NC memory (NVM) and control devices.

According to the model proposed by Compagnoni *et al*[17] on P/E dynamics in the flash memory devices employing Si–NC embedded in SiO_2, the F–N tunnelling for both tunnel oxide and control oxide is the main mechanism for programming at high voltage, and this is similar to the observation using our device. However, a large saturated V_{th} is obtained from high voltage programming in our experiment. This is due to the electron storage in a deeper energy level resulting from the higher work function of TiN–NCs and the electron trapping at the NC interface (TiON), which are not taken into account in the model in Ref.[17]. Therefore, in our device the tunnelling probability to gate via conduction band is low and in turn more charges can be retained in NCs. This requires a higher electric potential of NCs to reach the saturation. According to the model in Ref.[17], charging mechanism can be explained by direct tunnelling for tunnel oxide and F–N tunnelling for control oxide at low programming voltage (≤9 V). The control gate coupling ratio of our device is estimated to be 0.24 [here, coupling ratio = $C_{\mathrm{controloxide}}/(C_{\mathrm{tunnel\ oxide}} + C_{\mathrm{control\ oxide}})$, by neglecting the contribution of capacitance of floating-gate to source and drain since the device gate length is large. The electric field in the control oxide calculated for gate voltages of 7 to 9 V is in the range of 5.9 to 7.6 MV/cm. As the electric field in this range is large (onset of F–N tunnelling is ∼6 MV/cm[18,19]), the F–N tunnelling of the carriers through control oxide is expected to be the main mechanism at low programming field. Meanwhile, injection current through the 2.8 nm oxide can be considered to be generated by direct tunnelling, the same as the Compagnoni *et al*'s [17] model. This allows a large amount of charges in NCs due to well-separated oxide field at low programming voltages. In addition, the charges trapped at the interfacial TiON layer need to be taken into account in that explanation. Therefore, it is believed that the electron transition from tunnelling levels to trap levels of the interfacial layer is slower, resulting in the long induction time to attain the maximum programming speed from low voltage programming.

The erasing speed, which is determined by the same equation as that for programming speed, increases with increasing applied voltage. Erasing speeds are found to be 0.5 V/s for −5 V, 0.6 V/s for −9 V, and 0.7 V/s for −12 V, and the point to reach the maximum programming speed is similar to that

at an erasing time of $\sim 10\,\mu$s. This indicates that the same tunnelling mechanism is responsible for erasing which is reflected in the erasing current versus the erasing voltage characteristic (see Fig.5(b)), and the erasing speed increases with increasing electric field applied to the floating-gate. Work function of the gate material TaN in the control device is found to be 4.2 eV from the slope of the $\ln(J/E^2)$ vs E^{-1} plot for a negative applied field, being close to the reported value (4.3–4.7 eV).[20] Whereas, in the memory device, the estimated work function of 2.2 eV, indicating that F–N tunnelling is not responsible for the entire erasing voltage range. Electron tunnelling may occur by the combination of trap-assisted tunnelling and direct tunnelling, although this has not been proven yet. Under-erase problem is observed under the low voltage erasing mode. This is because charges cannot be removed fully from deep quantum well to the channel at such a low electric field. Fully erasing of the memory device is observed at a higher electric field.

5. Retention and endurance properties

The endurance characteristics of the memory device demonstrate the ability of the TiN–NCs to capture and release electrons without significant degradation of $V_{\rm th}$ window, even after 10^5 cycles of P/E operation, as shown in Fig.7(a). With a higher voltage for P/E pulses ($\pm$12 V for 1 ms), endurance performance is better up to 10^5 P/E cycles. This indicates that the quality of TEOS-deposited control oxide is as good as that of tunnel oxide grown from silicon surface. At a

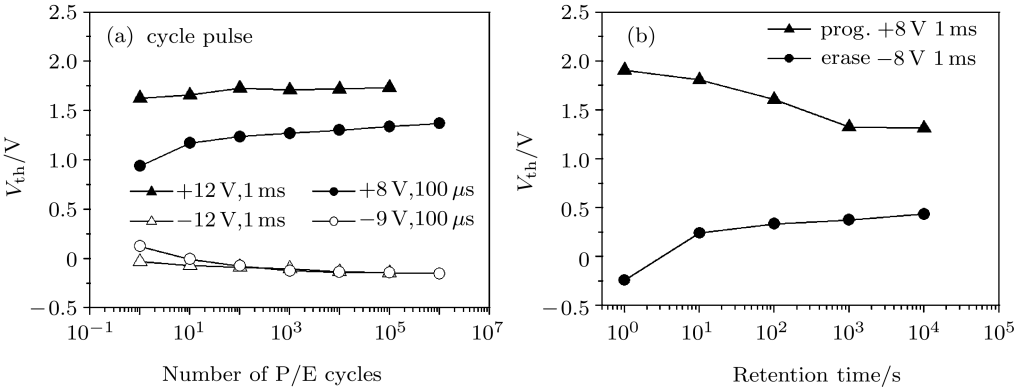


Fig.7. (a) Endurance characteristics of the TiN–NC memory device for two different P/E conditions. No significant degradation is observed even after 10^5 P/E cycles. (b) Retention characteristics of the TiN–NC memory (NVM) device at room temperature (100 μm/10 μm n-MOSFET).

low voltage of P/E pulses (+8/−9 V for 100 μs), a slight initial enlargement in $V_{\rm th}$ window is observed, followed by a negligible change. The slower and reversible electron transition from the tunnelling levels down to the trap levels in the interfacial TiON layer during the initial operation cycles may be responsible for the change in $V_{\rm th}$. In Fig.7(b) the data retention characteristics of the high speed programmed/erased ($\pm$8 V, 1 ms) memory device are demonstrated. The $V_{\rm th}$ decay is fast and $V_{\rm th}$ becomes saturated at 10^3 s. Interfacial charge decay from shallow trap levels of TiON may be faster. It is expected that the decay can be controlled by optimizing the tunnel oxide thickness as well as transition layer thickness. After 10^3 s, good retention property is observed due to the formation of deep quantum well from the high density and mid gap work function of TiN–NCs.

6. Conclusions

High density TiN–NCs as charge trapping media in NVM devices have been successfully fabricated by means of the advanced e-beam evaporation using thin TiN pre-deposition on SiO_2 followed by vacuum annealing. The annealing temperature is an important parameter in the formation of uniform, well-distributed, and small sized NCs. TiN–NCs with a number density of $\sim 10^{12}\,{\rm cm}^{-2}$ and a diameter of 5$\pm$2 nm have been obtained at an annealing temperature 850°C. TiN–NCs exhibit the polycrystalline properties mainly with the [200] orienta-

tion. XPS analysis confirms that the transition layer of TiON/SiON has been formed between TiN–NC and SiO_2 matrix from the NC formation on SiO_2, and the barrier height is reduced as a result. While the memory effects due to charge trapping in NCs have been demonstrated by attaining a large threshold voltage shift of ∼2.5 V from the fabricated TiN–NCs memory device. The large amount of charges in NCs is due to the direct tunnelling through the tunnel oxide, and the F–N tunnelling through the control oxide at low programming voltages, whereas for both the oxides at high programming voltages the charges are due to the F–N tunnelling. For low voltage P/E (±5V), good retention and excellent cycle endurance (10^6 P/E cycles) characteristics suggest that TiN–NCs can be the promising charge storage nodes for future NVM devices.

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