Vol 17 No 2, February 2008
1674-1056/2008/17(02)/0685-05

Chinese Physics B

© 2008 Chin. Phys. Soc.
and IOP Publishing Ltd

A novel 10-nm physical gate length double-gate junction field effect transistor*

Hou Xiao-Yu(侯晓宇)[a], Huang Ru(黄 如)[a]†, Chen Gang(陈 刚)[a], Liu Sheng(刘 晟)[a], Zhang Xing(张 兴)[a], Yu Bin(俞 滨)[b], and Wang Yang-Yuan(王阳元)[a]

[a] *Institute of Microelectronics, Peking University, Beijing* 100871, *China*

[b] *NASA Ames Research Center, Moffett Field, CA* 94035, *USA*

(Received 24 May 2007; revised manuscript received 2 July 2007)

A novel double-gate (DG) junction field effect transistor (JFET) with depletion operation mode is proposed in this paper. Compared with the conventional DG MOSFET, the novel DG JFET can achieve excellent performance with square body design, which relaxes the requirement on silicon film thickness of DG devices. Moreover, due to the structural symmetry, both p-type and n-type devices can be realized on exactly the same structure, which greatly simplifies integration. It can reduce the delay by about 60% in comparison with the conventional DG MOSFETs.

Keywords: MOSFET, double-gate MOSFET, depletion operation mode
PACC: 7280C, 7340R, 7360J

1. Introduction

As the device size is scaled down, many critical challenges such as reduction of leakage current, suppression of short-channel effect, and the compatibility of technology integrations have occurred.[1−3] Many novel structures, such as grooved gate MOSFETs, UTB MOSFET, FinFET, and Ω-gate MOSFET etc, are proposed to alleviate these problems.[4−8] Although these newly proposed device structures can obtain improved electric characteristics due to strong gate controllability over channel, they still have some disadvantages, such as increased fabrication complexity and critical requirement of Si film thickness.[9−12] In this paper, a novel double-gate (DG) depletion-mode junction field effect transistor (JFET) is proposed to provide a potential solution. Two-dimensional simulation is performed with device simulator-ISE8.0. The obtained results demonstrate that in comparison with conventional DG MOSFETs, the proposed DG JFET can achieve higher on-off current ratio due to the strong controllability of the junction gates. Moreover, due to the structural symmetry, both p-type and n-type devices can be realized on exactly the same structure, which can greatly simplify the integration.

2. Device structure and simulation

Figure 1 shows the structural comparison of conventional DG MOSFET and the proposed DG JFET. Unlike the conventional DG MOSFET where the device structure is based on metal-oxide-semiconductor structure, in the proposed DG JFET the gates are realized by the homogenous junctions. The electric

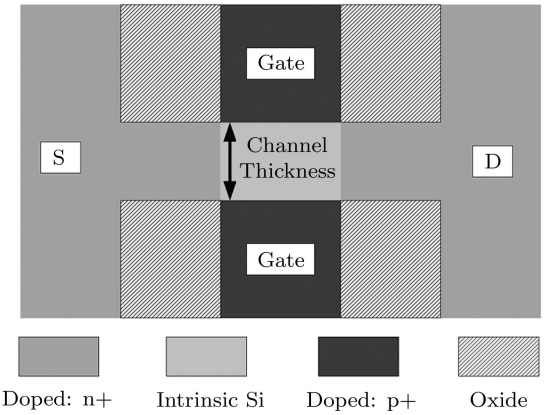


Fig.1. The schematic view of the proposed DG JFETs.

characteristics of the devices is investigated by adopting suitable transport model. The density gradient

*Project supported by the National Natural Science Foundation of China (Grant No 60625403), by the Special Funds for Major State Basic Research (973) Projects and NCET program.
†E-mail: huangr@ime.pku.edu.cn

model is adopted to take account of quantum effect and the hydrodynamic model is included to consider the small dimension. The gate length of simulated DG JFET is 10 nm, with the silicon film thickness of 10 nm. The doping of the gate and source/drain is the same and we use a typical value of 2×10^{20} for most simulation.

Due to the structural difference from the conventional DG MOSFET, the proposed DG JFET can perform as a depletion-mode device as showed in Fig.2. In comparison with the conventional DG MOSFETs where the depletion widths are broadened when the device changes from the off-state to the on-state, the proposed DG JFET, on the contrary, shows the narrowed depletion widths in this case. Since DG JFETs operate in a depletion mode, the carriers are confined to the centre of the channel in the on-state as showed in Fig.3. Thus the carriers do not suffer from scattering caused by surface roughness, resulting in higher carrier mobility. In the off-state, due to the p-n junction depletion, the channel is nearly depleted.

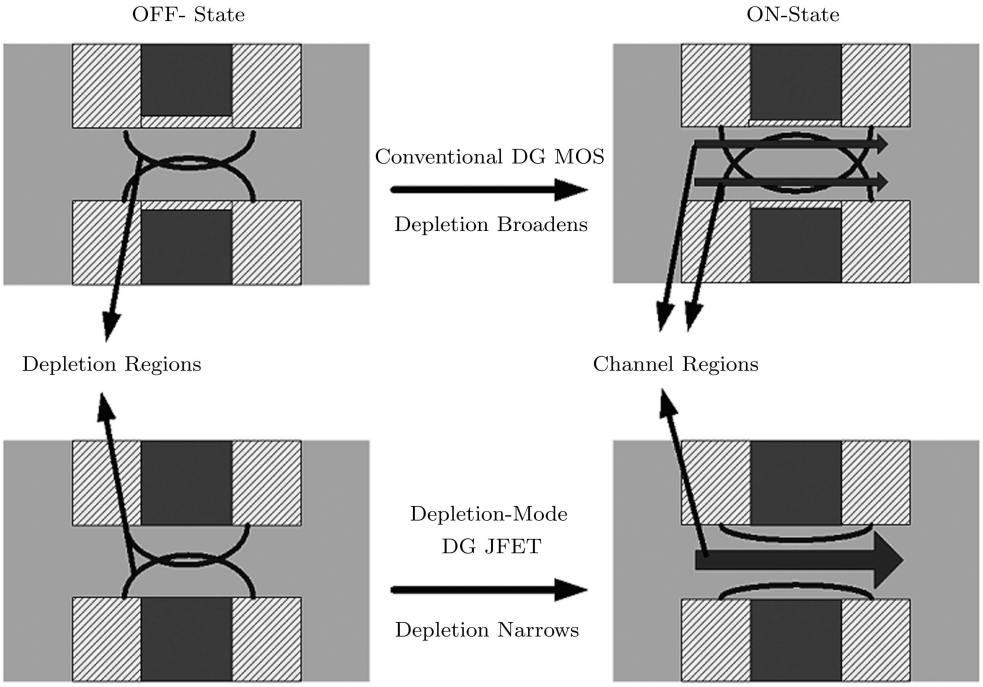


Fig.2. Operation of the proposed depletion mode DG JFETs with its channel in the centre as opposed to a conventional surface channel DG MOSFETs.

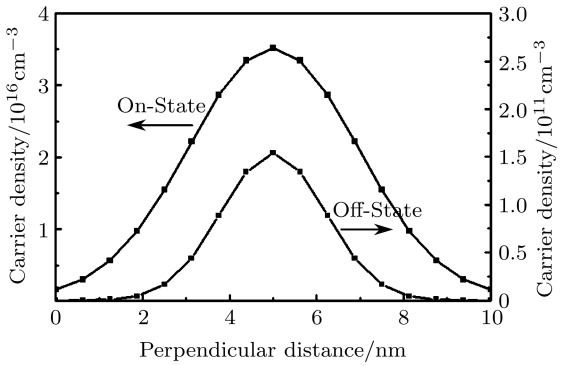


Fig.3. The carrier distributions perpendicular to the channel of DG JFETs.

3. Results and discussions

Since the gates are realized by p-n junction, the gate leakage is a crucial issue. Due to the effective control of the p-n junction gates, the proposed DG JFET greatly relaxes the stringent requirements on the body thickness scaling which is the critical problem in a conventional DG MOSFET. For the conventional DG MOSFET, the body thickness must be smaller than the channel length in order to effectively suppress the leakage current.[13] However, the DG JFET with body thickness equal to channel length can still achieve good performance. Table 1 shows the comparison between

the DG JFET and conventional DG MOSFETs of the same square body design with gate length of 10 nm. The gate workfunction of conventional DG MOSFETs is adjusted to reach the same leakage current of the DG JFET. Since the junction gates can control the channel more effectively, the proposed DG JFET exhibits much higher drive current with the same leakage current of conventional DG MOSFET. The supplied voltage $V_{\rm dd}$ is adopted as 0.75 V to satisfy the requirement on the gate leakage of ITRS 2006, as shown in Fig.4.

Table 1. Device structure parameters and extracted characteristics parameters of DG JFETs and DG MOSFETs with square body design.

	DG JFET		Conventional DG MOSFET	
	NMOS	PMOS	NMOS	PMOS
Channel length L_g/nm	10	10	10	10
Gate Oxide $T_{\rm ox}$/nm	1	1	—	—
Silicon film thickness $T_{\rm si}$/nm	10	10	10	10
Channel doping/cm^{-3}	1×10^{15}	1×10^{15}	1×10^{15}	1×10^{15}
$V_{\rm dd}$/V	0.75	0.75	0.75	0.75
Leakage current $I_{\rm off}$/(A/μm)	1.4×10^{-8}	1.1×10^{-9}	1.4×10^{-8}	1.1×10^{-9}
Drive current $I_{\rm on}$/(A/μm)	5.0×10^{-4}	1.8×10^{-4}	2.5×10^{-5}	1.8×10^{-5}
Ratio of $I_{\rm on}$ to $I_{\rm off}$	3.6×10^{4}	1.6×10^{5}	1.8×10^{3}	1.6×10^{4}

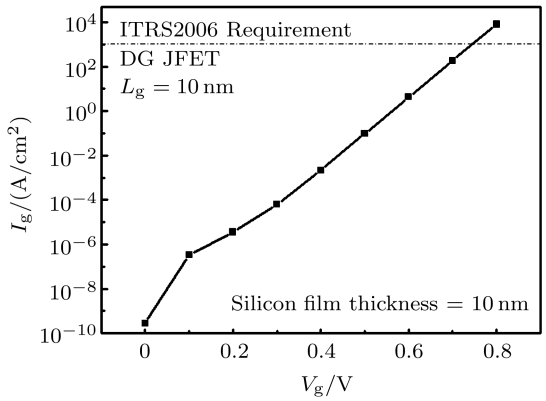


Fig.4. Gate leakage of the DG JFETs of square body design.

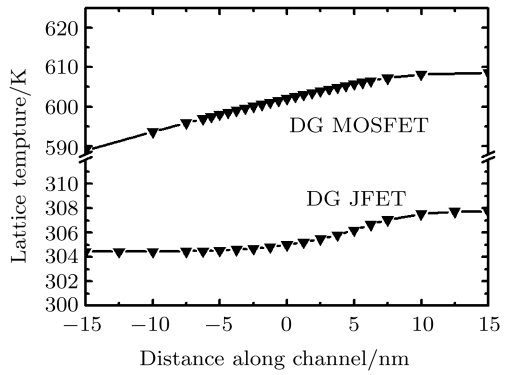


Fig.5. Comparison of the lattice temperatures between the conventional DG MOSFET and the proposed DG JFET of the square body design.

In the DG JFET, as the gates are directly connected to the channel without the gate oxide, the heat dissipation can be greatly improved. As shown in Fig.5, in comparison with the conventional DG MOSFET, the lattice temperature in the proposed DG JFET can be significantly reduced, which is very attractive for high-density integrated circuits. And due to the better heat dissipation and less surface scattering, the mobility of the DG JFET is higher than that of the conventional DG MOSFET, as shown in Fig.6.

Since the design of the channel can be a 'square' shape, the DG JFET of 10 nm gate length has a symmetrical structure. An n-type DG JFET can be easily transformed into a p-type DG JFET only through exchanging the gate and the source/drain contacts.

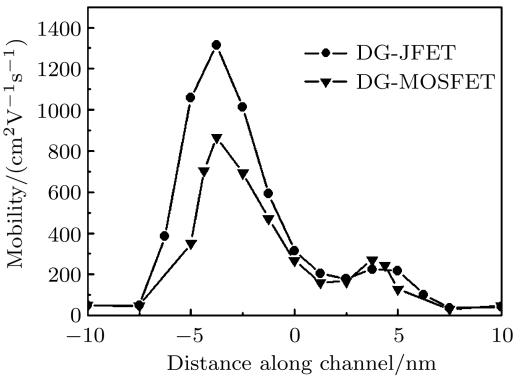


Fig.6. Comparison of carrier mobility in the channel of DG JFETs and conventional DG MOSFETs.

Figure 7 gives the schematic view to illustrate this unique feature. It can bring great simplicity in device fabrication and process integration, since it implies that the same device structure can be used as either n-type or p-type DG JFET only through exchanging interconnection designs. Figure 8 shows the comparison of the delay metric $C_{\mathrm{T}}V_{\mathrm{dd}}/I_{\mathrm{on}}$ between DG JFET and the conventional DG MOSFET with different gate/source/drain doping concentration. It can be seen that the proposed DG JFET can reduce the delay by about 60% in comparison with the conventional DG MOSFET at the doping of 2×10^{20}.

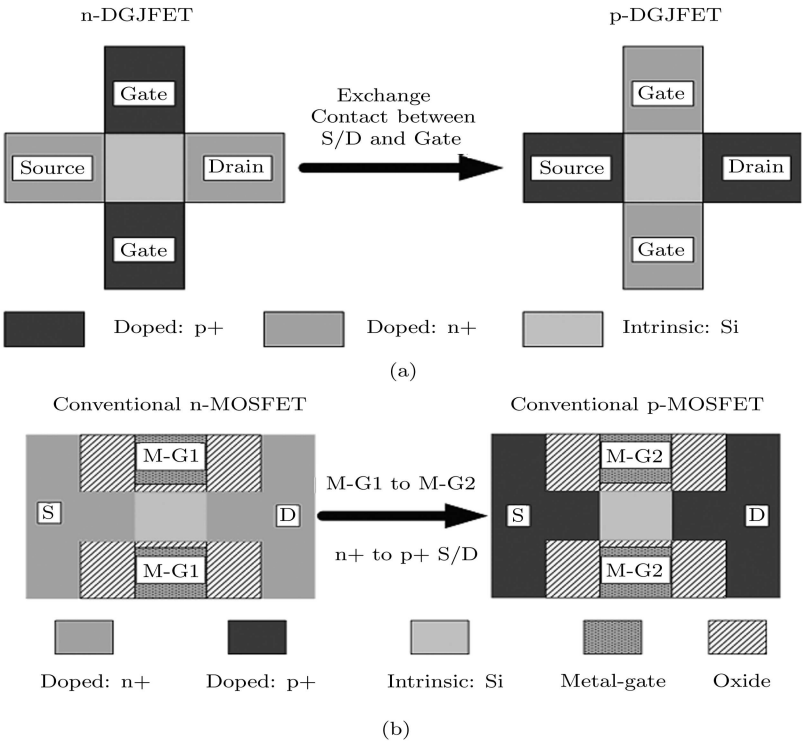


Fig.7. Comparison between the proposed DG JFETs with square body design and the conventional DG MOSFETs when transferring n-type device to p-type one.

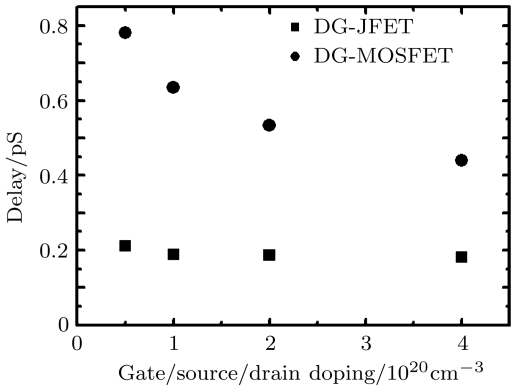


Fig.8. Comparison of the delays between the proposed DG JFETs and DG MOSFETs of square body design with different gate/source/drain doping concentrations.

4. Conclusions

A novel DG JFET with depletion operation mode is proposed and investigated in this paper. In comparison with the conventional DG MOSFETs, the novel DG JFET can achieve excellent performance with a square body and thus greatly relax the stringent requirements on silicon film thickness. Moreover, due to the strong controllability of the junction gates, the novel DG-JFET can obtain much higher drive current I_{on} than that of the conventional DG MOSFETs under the same leakage current . Compared with conventional DG MOSFET, the intrinsic delay is reduced by about 60%. Moreover, for the DG-JFET with a square body design, which has exactly symmetrical structure, both n-type and p-type DG-JFET can be realized simultaneously based on exactly the same DG-JFET only through exchanging contacts of source/drain and gates, it greatly simplifies the fabrication process.

References

[1] Huang X, Lee W C, Kuo C, Hisamoto D, Chang L, Kedzierski J, Anderson E, Takeuchi H, Choi Y K, Asano K, Subramanian V, King T J, Bokor J and Hu C 2001 *Electron Devices* **48** 880

[2] Choi Y K, Lindert N, Xuan P, Tang S, Ha D, Anderson E, King T J, Bokor J and Hu C 2001 *IEDM Tech. Dig.* 421

[3] Yu B, Chang L, Ahmed S, Wang H, Bell S, Yang C Y, Tabery C, Ho C, Xiang Q, King T J, Bokor J, Hu C, Lin M R and Kyser D 2002 *IEDM Tech. Dig.* 251

[4] Zheng Z S, Liu Z L, Zhang G Q, Li N, Fan K, Zhang E X, Yi W B, Chen M and Wang X 2005 *Chin. Phys.* **14** 565.

[5] Tong J N, Zou X C and Shen X B 2003 *Acta Phys. Sin.* **53** 2905 (in Chinese)

[6] Xiong S and Bokor J 2003 *Electron Devices* **50** 2255

[7] Krishnamohan T, Jungemann C and Saraswat K C 2003 *IEDM Tech. Dig.* 687

[8] Taur Y 2001 *Electron Devices* **48** 2861

[9] Wong H P, Frank D J, Solomon P M, Wann C H J and Welser J J 1999 *Proc. IEEE* **87** 537

[10] Huang X, Lee W C, Kuo C, Hisamoto D, Chang L, Kedzierski J, Anderson E, Takeuchi H, Choi Y K, Asano K, Subramanian V, King T J, Bokor J and Hu C 1999 *IEDM Tech. Dig.* 67

[11] Hisamoto D, Lee W C, Kedzierski J, Anderson E, Takeuchi H, Asano K, King T J, Bokor J and Hu C 1998 *IEDM Tech. Dig.* 1032

[12] Kedzierski J, Fried D M, Nowak E J, Kanarsky T, Rankin J H, Hanafi H, Natzle W, Boyd D, Zhang Y, Roy R A, Newbury J, Yu C, Yang Q, Saunders P, Willets C P, Johnson A, Cole S P, Young H E, Carpenter N, Rakowski D, Rainey B A, Cottrell P E, Ieong M and Wong H P 2001 *IEDM Tech. Dig.* 437

[13] Ieong M, Wong H P, Nowak E, Kedzierski J and Jones E C 2002 *Proc. Symp. Quality Electronic Design* 492