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Study on the dose rate upset effect of partially depleted silicon-on-insulator static random access memory

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This paper implements the study on the Dose Rate Upset effect of PDSOI SRAM (Partially Depleted Silicon-On-Insulator Static Random Access Memory) with the Qiangguang-I accelerator in Northwest Institute of Nuclear Technology. The SRAM (Static Random Access Memory) chips are developed by the Institute of Microelectronics of Chinese Academy of Sciences. It uses the full address test mode to determine the upset mechanisms. A specified address test is taken in the same time. The test results indicate that the upset threshold of the PDSOI SRAM is about 1×10^8 Gy(Si)/s. However, there are a few bits upset when the dose rate reaches up to 1.58×10^9 Gy(Si)/s. The SRAM circuit can still work after the high level γ ray pulse. Finally, the upset mechanism is determined to be the rail span collapse by comparing the critical charge with the collected charge after γ ray pulse. The physical locations of upset cells are plotted in the layout of the SRAM to investigate the layout defect. Then, some layout optimizations are made to improve the dose rate hardened performance of the PDSOI SRAM.

Keywords: dose rate, PDSOI, SRAMs, upset
PACC: 6180, 0250, 8140

1. Introduction

SOI (Silicon-On-Insulator) technologies are used to harden devices in the environment of dose rate irradiation thanks to their hardness properties (immunity to latch-up, reduced sensitive volume). Dose rate irradiations present some similarities with single event upset (SEU) since they both imply a transient irradiation which induces a parasitic current mainly generated by the silicon regions of the device. Like for SEU, dose rate irradiations are susceptible to activate the parasitic bipolar transistor inherent to the PDSOI MOS (metal–oxide–semiconductor) structure. The upsets caused by dose rate irradiation can be due to either local capacitive effects induced by the cell own photocurrent, or the rail span collapse (resistive effect) at lower dose rate. Moreover, the capacitive failure mode appears when the photocurrent generated by each cell is high enough to reach the critical charge at higher dose rate. On the other hand, the resistive failure mechanism appears when the photocurrent generated in a single cell is not high enough to induce its own local upset. The sum of all the elementary photocurrents is necessary to induce a global collapse of the supplying voltage.[1] The two mechanisms are shown in Fig. 1. Below D'_0, cells are not able to generate enough photocurrent to induce their own upset. However, a global upset can though be observed, if the resistance of the supplying rails is high enough to induce a rail span collapse. This resistive effect is observed if the sum of all the elementary photocurrents of the N off-state transistors is high enough to induce a voltage drop in the resistive supplying rails (resistance R), higher than the retention voltage margin ($V_{\rm dd}-V_{\rm retention}$) of the circuit:

$$RNI_{\rm ph}=V_{\rm dd}-V_{\rm retention}. \tag{1}$$

If the dose rate is low (far from D'_0), the voltage margin ($V_{\rm dd}-V_{\rm retention}$) is constant and does not depend on dose rate. If the dose rate is higher, close to D'_0 (or

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if the pulse duration is close to T_0), the memory cells are weakened by their own photocurrent generation, and the voltage margin is lowered. The SRAM may upset. Thus, the resistance value of supplying rails is the key point of the whole IC (Integrated Circuit) design for radiation hardening.

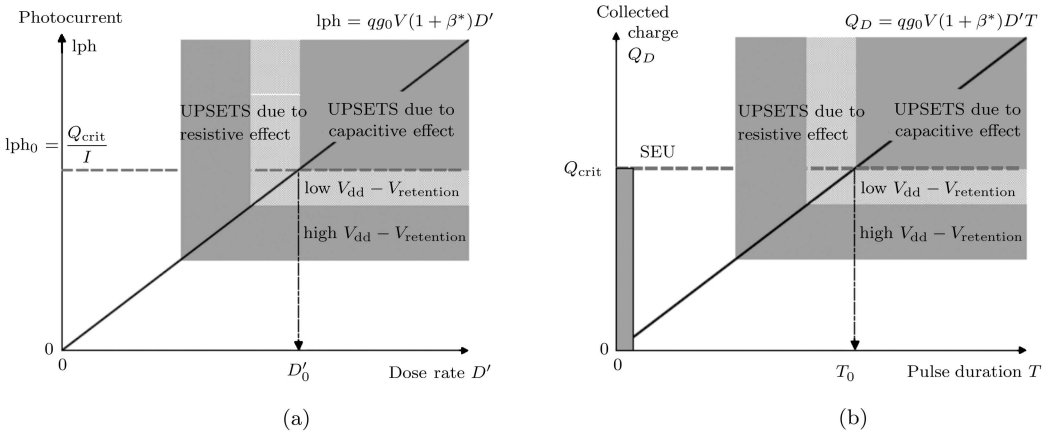


Fig.1. Representation of the regions of upsets due to capacitive and resistive effects: (a) the photocurrent versus dose rate; (b) the collected charge versus pulse duration.[1]

Therefore, if the capacitive mechanism takes effect, the memory IC will lost almost all its information. Consequently, catastrophic failure of system will occur. However, if the resistive mechanism takes effect, certain local cells will be upset. Thus the information corrupted may be rebuilt by some error correcting method.

2. Device under test description

The SRAM circuits are fabricated on SIMOX (Separation by implanted oxygen) material with a $0.2\,\mu$m Si film on a $0.4\,\mu$m Buried Oxide (BOX). The source/drain implants are driven to the BOX interface so that the depletion region (charge collection region) is only at the drain/body interface beneath the gate. The body nodes of all transistors, except the pass transistors, are connected to the associated source node by body-tied-to-source (BTS) straps, as shown in Fig.2(a). For the n-channel transistor, the body tie is a p^+ source/drain diffusion that contacts the p^- body region. The silicide process then connects the p^+ body tie to the n^+ source. Pass gates, such as the access transistors in the memory cell, have the body node connected to supplying voltage (V_{ss} for n-channel, V_{dd} for p-channel) by a connection at the edge, as shown in Fig.2(b). These body contacts help to reduce parasitic bipolar effects, but do not completely eliminate them because of distributed resistance from the contact to portions of the body node. However, the improvement factor compared to register without body ties is greater than 6.[1] The memory cell is typical six transistors cell with no feedback delay element. Two metal layers with one poly layer are used to perform the interconnections.

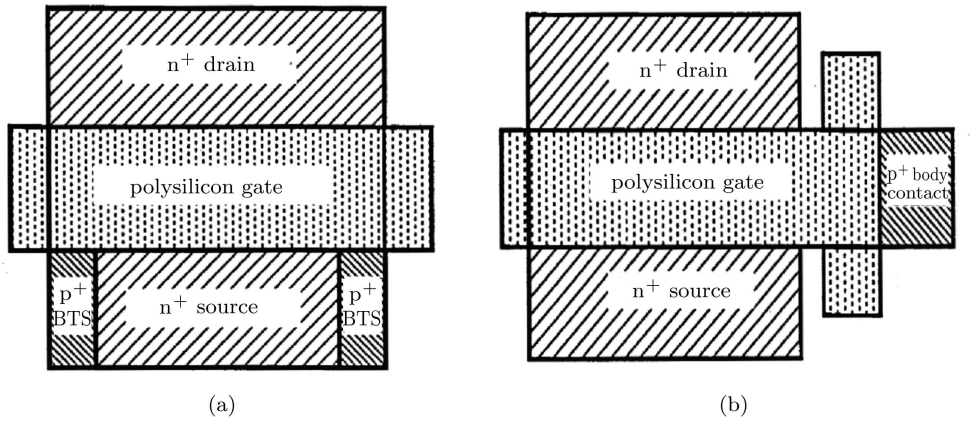


Fig.2. (a) Body-Tied-to-Source (BTS) straps; (b) Body contact to supplying voltage.[2]

3. Experimental description

Experiments are implemented with the Qiangguang-I accelerator in Northwest Institute of Nuclear Technology. Device under test is placed in the socket on test board. The whole board is sealed in a metal box. Pins connected by coaxial cables are linked to the test equipment and oscilloscopes. The experimental set-up is presented in Fig.3.

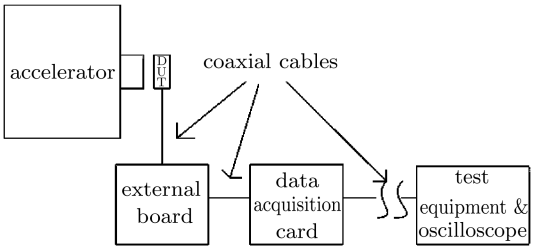


Fig.3. The experimental set-up diagram.

The accelerator has γ ray pulse with dose rate range from 1×10^8 Gy(Si)/s to 1×10^{10} Gy(Si)/s, duration range from 20 ns to 50 ns. In the experiments, three kinds of γ ray pulse are used. The detailed parameters are list in Table 1. Prior to these experiments total dose failure level was measured for the tested SRAM circuits and found to be $> 1 \times 10^4$ Gy(Si) in Northwest Institute of Nuclear Technology by Co–60 source. If each test sample accumulate a total dose of not more than 10^3 Gy(Si), the total dose effects are not taken into account.[3−6] In the dose rate effect experiment the accumulated dose is about 6×10^1 Gy(Si). Then the impact of total dose is ignored. Test pattern '01010101' is written to the SRAM cells before each radiation pulse. During the pulse, the SRAM circuit is in read mode with specified address '1555H'. The waves of eight output pins are collected by the oscilloscopes in the same time. After each radiation pulse all memory cells are read and compared with the original pattern. If there is any error, the cell address and data will be recorded. Afterwards, the error map will be drawn.

Table 1. Experimental parameters of γ ray pulse.

No.	Dose rate/ (Gy(Si)/s)	Pulse width/ns	Total dose/(Gy(Si))
1	2.42×10^8	33.3	8.06
2	8.80×10^8	25.0	2.20×10^1
3	1.58×10^9	20.1	3.18×10^1

4. Experimental result and discussion

4.1. Dose rate threshold determination

The results of upset are listed in Table2. From this table, the numbers of 0 to 1 upset and 1 to 0 upset will almost be equal as the rising of the dose rate. Thus it can be predicted that the upset trend will be 'inversion'.[7,8] According to Refs.[7] and [8], the number of upsets vs. dose rate dependence range is wide-up to three decades of dose rate magnitude. The accelerator in Northwest Institute of Nuclear Technology is hard to achieve that high dose rate to investigate the 'inversion' effect. Therefore, the simulation of dose rate by laser test may be expected to study the upset number vs. dose rate. The dose rate of pulse No.2 is about four times higher than No.1, but the upset number of No.2 is less than No.1. Then it can be decided that the dose rate threshold is about 1×10^8 Gy(Si)/s magnitude for the upset number should increase with the dose rate when it is somewhat higher than the threshold.

Table 2. Information of Upsets.

Pulse No.	Byte upset number	Bit upset number	Upset number 0 to 1	Upset number 1 to 0
1	18	62	15	47
2	8	34	10	24
3	44	114	49	65

4.2. Main mechanism determination

Capacitive and resistive failure mechanisms discussed before are usually used to explain the upsets effect. In order to determine which mechanism caused the upset of the PDSOI SRAM, the critical charge of the SRAM must be calculated and compared with the collected charge.

Firstly, some parameters of the PDSOI SRAM are illustrated below. The threshold value of the SEU is ranged from $59\,\mathrm{MeV\cdot cm^2/mg}$ to $84.4\,\mathrm{MeV\cdot cm^2/mg}$, which is acquired through the experiments on HI-13 Tandem Accelerator in China Institute of Atomic Energy. The value of β^* is simulated using the ISE-TCAD tools,[9] and its maximum value is 1.7 which is comparable to the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) with body ties in Ref.[10]. Besides, in view of the total dose radiation resistance of the SRAM (Static Random Access Memory) up to $1\times10^4\,\mathrm{Gy(Si)}$, the body ties is very effective. Therefore the simulation result of β^* is reasonable.

Secondly, according to the Ref.[1], the critical charge can be calculated through the threshold value of the SEU.

By using the equivalence $1\,\mathrm{MeV\cdot cm^2/mg}\approx 0.01\,\mathrm{pC}/\mu\mathrm{m}$ in silicon, the corresponding critical charge necessary to induce a cell upset is equal to

$$\begin{aligned} Q_{\mathrm{cirt}} &= Q_{\mathrm{LET}}L \\ &= 59(84.4)\times 0.01\,\mathrm{pC}/\mu\mathrm{m}\times 0.2\,\mu m \\ &= 0.118\,\mathrm{pC\ to\ }0.1688\,\mathrm{pC}, \end{aligned} \tag{2}$$

where Q_{cirt} is the critical charge, Q_{LET} is the charge created by the heavy ion strike in the silicon, L is the trace length of the heavy ion (In PDSOI case, the L is thickness of the silicon film for active devices on the BOX layer).

The collected charge is given by

$$Q_{\mathrm{coll}} = qg_0V(1+\beta^*)D't, \tag{3}$$

where q is the elementary charge ($q=1.6\times10^{-19}\,\mathrm{C}$), g_0 is the generation rate in silicon ($g_0\approx 4\times10^{15}$ electron-hole pairs $\mathrm{Gy^{-1}cm^{-3}}$), D' is the dose rate (Gy(Si)/s), t is the pulse duration, β^* is the gain of the parasitic transistor and V is the sensitive volume (In SOI, the sensitive volume is clearly defined by the body volume under the gate: $V=LWt_{\mathrm{Si}}$, where L is the gate length, W is the gate width, and t_{Si} is the silicon film thickness.). By calculations, the collected charge of a MOSFET is 0.01 pC to 0.05 pC during radiation.

Finally, comparing Q_{cirt} with Q_{coll}, we find that the Q_{coll} is smaller, which means that the photocurrent generated in a single cell is not high enough to induce its own local upset. Thus it can be concluded that the upset is caused mainly by resistive failure mechanism.

4.3. Upsets analysis and method for radiation hardened

Error map is plotted in Fig.4. The points in the map are the corresponding physical locations of upset cells in layout. Assisting with the design layout (Fig.5), we can see that the upsets are located at the edge of each block of memory. From Fig.5(a), the power supply bus which is shown as white line, is around the die with horizontal 'finger' supplying power to the individual memory cells. The whole power supply bus finally makes comb shape with the end in middle of die. The GND (ground) bus is same as power bus but with main bus in the middle of die, shown in Fig.5(b). When dose rate level is low as test No.1, the upsets mainly locate at the end of power bus. With dose rate level going higher, the upsets occur at the end of GND bus, just like test No.2 and No.3. Because the density of GND bus is higher than the power bus, the rail span collapse in power bus is more serious than in GND bus. That is why the upset happens first at the end of power bus. The waves of the output pins are also shown in Fig.6. In the figure, it can be seen that the cell with address of '1555H' and data of '55H' does not upset even with some interruption.

From the upset map, it can be seen that the design of this layout of PDSOI SRAM is not perfect that the supplying bus is too long and not wide enough. To make improvement simple, pads are added on the corners of memory IC die and connected to the supplying pin of package. The relative length of the supplying bus is shorted, thus the rail span collapse may be mitigated. Further radiation test will then be taken to verify the improvement.

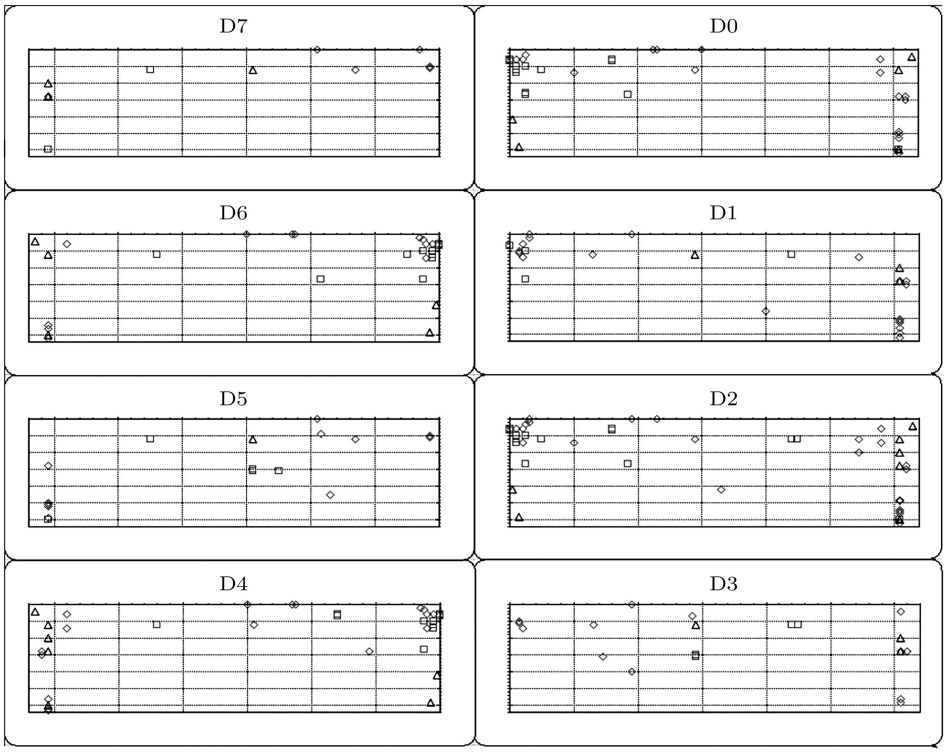
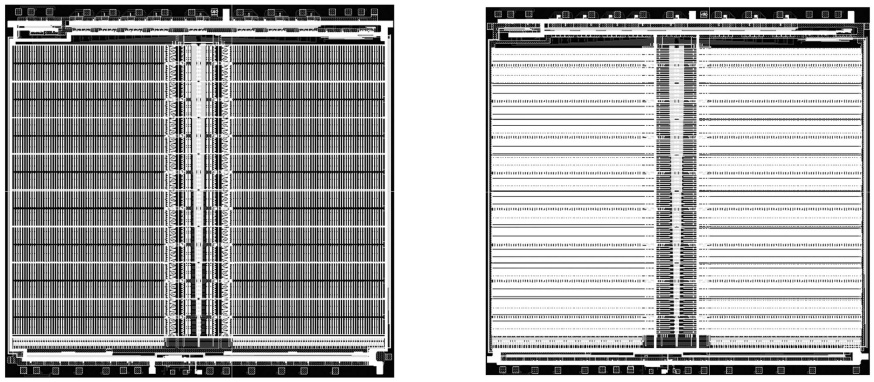
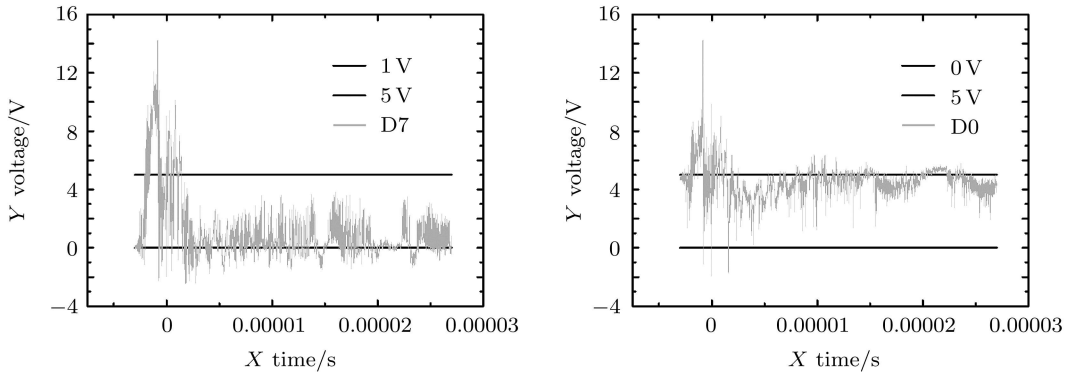


Fig.4. Error map with dose rate of □: 2.42×10^8 Gy(Si)/s; △: 8.80×10^8 Gy(Si)/s; ♢: 1.58×10^9 Gy(Si)/s.



(a) The white lines are power supply bus. (b) The white lines are GND supply bus.

Fig.5. Supplying bus distribution in design layout.



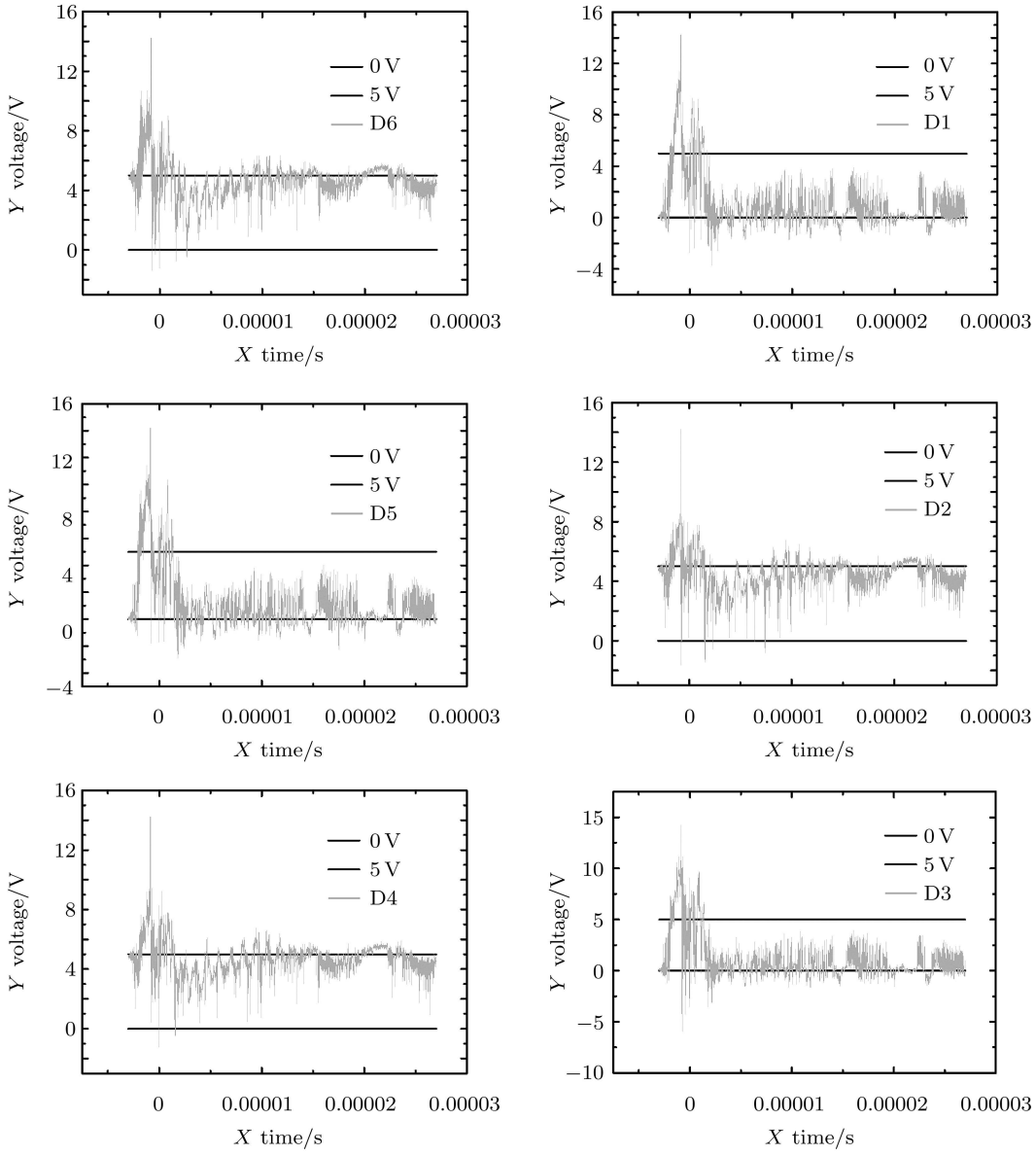


Fig.6. Waves of output pins of the PDSOI SRAM during the γ ray pulse.

5. Conclusions

According to the experimental results, the threshold dose rate of the PDSOI SRAM circuit is about 1×10^8 Gy(Si)/s, and the main mechanism of upset is rail span collapse. Therefore, in order to make the PDSOI SRAM resistant to dose rate irradiation, some additional pads are added on the corners of memory IC die to separate the power and GND path to several parts. In the result, the resistance decrease with the length of the supply lines. Consequently, the voltage collapse on supply lines may be mitigated. Further radiation test is expected.

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