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Performance and analytical modelling of halo-doped surrounding gate MOSFETs*

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Halo structure is added to sub-100 nm surrounding-gate metal–oxide–semiconductor field- effect-transistors (MOSFETs) to suppress short channel effect. This paper develops the analytical surface potential and threshold voltage models based on the solution of Poisson's equation in fully depleted condition for symmetric halo-doped cylindrical surrounding gate MOSFETs. The performance of the halo-doped device is studied and the validity of the analytical models is verified by comparing the analytical results with the simulated data by three dimensional numerical device simulator Davinci. It shows that the halo doping profile exhibits better performance in suppressing threshold voltage roll-off and drain-induced barrier lowering, and increasing carrier transport efficiency. The derived analytical models are in good agreement with Davinci.

Keywords: MOSFET, surrounding gate, compact model, halo
PACC: 7340Q, 1240Q, 7360J

1. Introduction

For extending the scalability of CMOS technology, multiple-gate metal–oxide–semiconductor field-effect-transistors (MOSFETs) such as double-gate,[1,2] triple-gate,[3] and surrounding-gate MOSFETs[4−8] are becoming intense research subjects because of their better gate control capacity and scaling potential. Among these advanced structures, the surrounding-gate MOSFETs are considered to be the most attractive device, which gains intensive control of the potential in the channel.[9−13] When the gate length scales down to sub-100 nm, short channel effect (SCE) such as threshold voltage roll-off and drain induced barrier lowering (DIBL) will be difficult to control in surrounding-gate MOSFETs. To reduce threshold voltage roll-off and DIBL, channel doping has to be increased. However, higher channel doping results in lower carrier mobility and therefore lower current.[14,15] Halo doping profile has been used to optimize the on-state current, off-state leakage current and SCE in planar MOSFETs.[16−23]

In the present work, the performance of surrounding gate MOSFETs with symmetric halo doping profile is studied in suppressing SCE and improving current driving capacity. Analytical two-dimensional models for surface potential, electric field and threshold voltage are developed by solving the Poisson's equation in fully depleted cylindrical surrounding gate MOSFETs. The validity of the models is verified by the close proximity of the analytical results and the simulated data of the three dimensional (3D) device simulator Davinci of Synopsys.

2. Analytical model

The schematic cross-section of the halo doped cylindrical surrounding-gate MOSFET (HSG) is shown in Fig.1. The halo doping concentration $N_{\rm h}$ is higher than the doping concentration $N_{\rm c}$ in the rest of the channel. The channel in HSG can be divided into three regions.

The coordinate system consists of a radial direction r, a vertical direction z, and an angular component θ (not shown in the figure) in the plane vertical to the direction z. The symmetry of the structure ensures that the potential and, hence, the electric field have no variation in the θ direction. Thus a two-dimensional (2D) analysis is sufficient.

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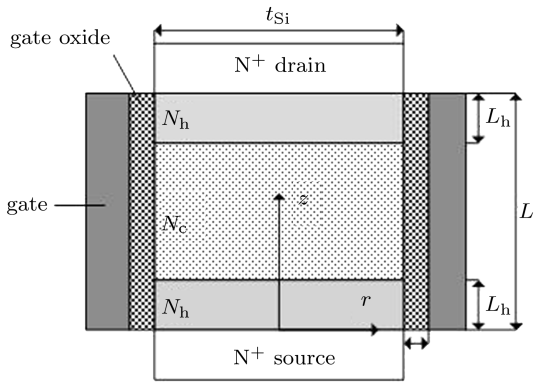


Fig.1. Schematic cross-section of halo doped surrounding-gate MOSFET.

The surface potential and electric field distribution can be derived by solving the Poisson equation in the silicon pillar. Assuming that the influence of the charge carriers and fixed oxide charges on the electrostatics of the channel can be neglected, before the onset of strong inversion, we can write the 2D Poisson equation of potential distribution in the silicon pillar[24] as

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi_j(r,z)}{\partial r}\right)+\frac{\partial^2\phi_j(r,z)}{\partial z^2}=\frac{qN_j}{\varepsilon_{Si}}$$
$$(L_{j-1}\le z\le L_j,\ 0\le r\le t_{Si}/2\ , j=1,2,3), \quad (1)$$

where ε_{Si} is the dielectric constant of silicon film, $N_1=N_h$, $N_2=N_c$, $N_3=N_h$, $L_0=0$, $L_1=L_h$, $L_2=L-L_h$, $L_3=L$, $\phi_j(r,z)$ $(j=1,2,3)$ is the potential distribution in region j.

The potential profile in the radial direction, i.e., the r-dependence of $\phi_j(r,z)$, can be approximated by a simple parabolic function for the fully depleted surrounding-gate MOSFET as

$$\phi_j(r,z)=c_{j0}(z)+c_{j1}(z)r+c_{j2}(z)r^2$$
$$(L_{j-1}\le z\le L_j,\ 0\le r\le t_{Si}/2, j=1,2,3). \quad (2)$$

The electric field in the centre of the silicon pillar is zero by symmetry,[25] so we have

$$\frac{\partial\phi_j(r,z)}{\partial r}|_{r=0}=0=c_{j1}(z)$$
$$(L_{j-1}\le z\le L_j,\ j=1,2,3). \quad (3)$$

The channel surface potential $\varphi_{sj}(z)$ is

$$\varphi_{sj}(z)=\phi(t_{Si}/2,z)=c_{j0}(z)+c_{j2}(z)t_{Si}^2/4. \quad (4)$$

The electric flux at the oxide–silicon interface is continuous, so we have

$$\frac{\partial\phi_j(r,z)}{\partial r}\Big|_{r=t_{Si}/2}$$
$$=\frac{C_f}{\varepsilon_{Si}}(V_{gs}-V_{FBj}-\varphi_{sj}(z))=c_{j2}(z)t_{Si}$$
$$(j=1,\ 2,\ 3), \quad (5)$$

where $C_f=2\varepsilon_{ox}/[t_{Si}\ln(1+2t_{ox}/t_{Si})]$, ε_{ox} is the dielectric constant of the gate oxide, t_{ox} is the thickness of gate oxide, V_{gs} is the gate-to-source bias voltage and V_{FBj} is the channel flat band voltage of region j.

From Eqs.(1) to (5), we can obtain the differential equation of the surface potential $\varphi_{sj}(z)$ as follows:

$$\frac{d^2\varphi_{sj}(z)}{dz^2}-\lambda^2\varphi_{sj}(z)=\beta_j \quad (j=1,\ 2,\ 3), \quad (6)$$

where $\lambda=\sqrt{4C_f/(\varepsilon_{Si}t_{Si})}$ and $\beta_j=qN_i/\varepsilon_{Si}-\lambda^2(V_{gs}-V_{FBj})$.

Equation (6) is a second-order differential equation with constant coefficients and the general solution for the surface potential is of the form:

$$\varphi_{sj}(z)=A_je^{-\lambda z}+B_je^{\lambda z}-\frac{\beta_j}{\lambda^2}$$
$$(L_{j-1}\le z\le L_j,\quad j=1,2,3). \quad (7)$$

The coefficients A_j and B_j can be determined by the boundary conditions. The potential at the source end is

$$\phi_1(t_{Si}/2,0)=\varphi_{s1}(0)=V_b, \quad (8)$$

where V_b is the built-in potential drop across the source–body junction.

The potential at the drain end is

$$\phi_3(t_{Si}/2,L_3)=\varphi_{s3}(L_3)=V_b+V_{ds}, \quad (9)$$

where V_{ds} is the applied drain source bias voltage.

The surface potential and electric flux at the interfaces between regions 1, 2 and 3 are continuous, so we have

$$\phi_j(t_{Si}/2,L_j)=\phi_{j+1}(t_{Si}/2,L_j) \quad (j=1,2), \quad (10)$$

$$\frac{\partial\phi_j\,(t_{Si}/2,z)}{\partial z}\Big|_{z=L_j}=\frac{\partial\phi_{j+1}\,(t_{Si}/2,z)}{\partial z}\Big|_{z=L_j}$$
$$(j=1,2). \quad (11)$$

Using Eqs.(8) to (11), we can obtain constants A_j

and B_j as follows:

$$A_1 = \Big[(V_{b1} + (1 - e^{\lambda L)})V_{gs}\Big] \Big/ 2\sinh(\lambda L), \quad (12a)$$

$$B_1 = \big[(V_{b2} + (e^{-\lambda L} - 1)V_{gs}\big]/2\sinh(\lambda L), \quad (12b)$$

$$A_2 = \Big[(V_{b1} + (1 - e^{\lambda L)})V_{gs}\Big] \Big/ 2\sinh(\lambda L) - e^{\lambda L_h}(U_1 - U_2)/2, \quad (12c)$$

$$A_3 = \Big[(V_{b1} + (1 - e^{\lambda L)})V_{gs}\Big] \Big/ 2\sinh(\lambda L) - e^{\lambda L_h}(U_1 - U_2)/2 - e^{\lambda(L-L_h)}(U_2 - U_3)/2, \quad (12d)$$

$$B_2 = \big[(V_{b2} + (e^{-\lambda L} - 1)V_{gs}\big]/2\sinh(\lambda L) - e^{-\lambda L_h}(U_1 - U_2)/2, \quad (12e)$$

$$B_3 = \big[(V_{b2} + (e^{-\lambda L} - 1)V_{gs}\big]/2\sinh(\lambda L) - e^{-\lambda L_h}(U_1 - U_2)/2 - e^{-\lambda(L-L_h)}(U_2 - U_3)/2, \quad (12f)$$

where $V_{b1} = (V_b+U_1)e^{\lambda L} - (V_b+V_{ds}+U_3) - \cosh[\lambda(L - L_h)](U_1 - U_2) - \cosh(\lambda L_h)(U_2 - U_3)$, $V_{b2} = V_b + V_{ds} + U_3 + \cosh[\lambda(L - L_1)](U_1 - U_2) + \cosh(\lambda L_h)(U_2 - U_3) - (V_b - U_1)e^{-\lambda L}$, $U_1 = \dfrac{qN_h}{\lambda^2\varepsilon_{Si}} + V_{FB1}$, $U_2 = \dfrac{qN_c}{\lambda^2\varepsilon_{Si}} + V_{FB2}$, and $U_3 = \dfrac{qN_h}{\lambda^2\varepsilon_{Si}} + V_{FB1}$.

The electric field pattern along the channel determines the electron transport velocity through the channel. Differentiating $\varphi_{sj}(z)$ $(j = 1, 2, 3)$ with respect to z, we get the electric field component $E(z)$ in the z direction as follows:

$$E(z) = -A_j\lambda e^{-\lambda z} + B_j\lambda e^{\lambda z} \quad (L_{j-1} \le z \le L_j, j = 1, 2, 3\ ). \quad (13)$$

When the halo doping concentration N_h is greater than N_c, the minimum surface potential $\varphi_{s\,min}$ lies in the halo near the source. Let the differentiation of $\varphi_{s1}(z)$ be equal to zero, $\varphi_{s\,min}$ can be obtained as

$$\varphi_{s\,min} = 2\sqrt{A_1B_1} - \beta_1/\lambda^2. \quad (14)$$

Threshold voltage V_{th} is the value of the gate voltage V_{gs} at which a conducting channel is induced at the surface of the MOSFET. Therefore, the threshold voltage is taken to be that value of V_{gs} at which $\varphi_{s\,min} = 2\varphi_F$, where φ_F is the difference between the extrinsic Fermi level in the silicon pillar and the intrinsic Fermi level. From Eqs.(12) and (14), we have

$$V_{th} = \frac{-\eta + \sqrt{\eta^2 - 4\sigma\xi}}{2\sigma}, \quad (15)$$

where $\sigma = 2\cosh(\lambda L) - 2 - \sinh^2(\lambda L)$, $\eta = V_{b1}(e^{-\lambda L} - 1) + V_{b2}(1 - e^{\lambda L}) + 2\sinh^2(\lambda L)(2\varphi_F + U_1)$, $\xi = V_{b1}V_{b2} - \sinh^2(\lambda L)(2\varphi_F + U_1)^2$.

Subthreshold slope S is a very important parameter characterizing the subthreshold region and is defined as

$$S = \frac{\partial V_{gs}}{\partial(\log I_d)} = \frac{kT\ln(10)}{q} \Big/ \frac{\partial\varphi_{s\,min}}{\partial V_{gs}}. \quad (16)$$

Using Eqs.(12) and (14), we can obtain S as

$$S = \frac{kT\ln(10)}{q} \frac{2\sinh(\lambda L)\sqrt{A_1B_1}}{B_1(1 - e^{\lambda L}) + A_1(e^{-\lambda L} - 1) + 2\sinh(\lambda L)\sqrt{A_1B_1}}. \quad (17)$$

3. Results and discussion

Now we will study the performance of HSG in threshold voltage roll-off, DIBL and carrier transport efficiency, compare it with uniformly doped surrounding-gate MOSFETs (USG) which is the special case of HSG when $N_h = N_c$, and verify the analytical models by comparing analytical results with the simulated data of Davinci. In all figures, symbols represent the simulated data by Davinci, and lines represent the analytical results. Unless otherwise noted, drain and source doping concentration $N_D = 10^{20}\,cm^{-3}$, $N_h = 3 \times 10^{17}\,cm^{-3}$, $N_c = 6 \times 10^{16}\,cm^{-3}$, $t_{ox} = 4\,nm$, $t_{Si} = 50\,nm$, $L_h = 20\,nm$, $L = 100\,nm$.

The surface potential in the channel of HSG and USG is plotted in Fig.2. It can be seen from the figure that the minimum surface potential occurs in the halo region near the source for HSG. The minimum surface potential $\varphi_{s\,min}$ in HSG almost keeps unchanged when V_{ds} is increased from 0.05 V to 1.3 V, whereas the increase of $\varphi_{s\,min}$ in USG is evident. Therefore the gate has more effective control of channel in HSG than that

in USG.

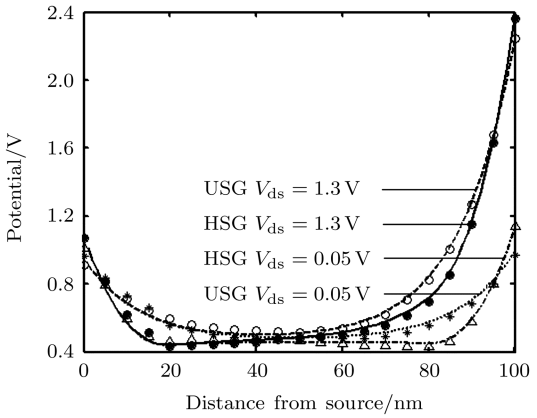


Fig.2. Surface potential along the channel under different V_{ds}(V_{gs} = 0.2 V).

The surface electric field in the channel is shown in Fig.3. It could be found that there is an electric field peak near the halo boundary in HSG. Because the electric field peak is close to the source, carriers will be accelerated earlier and travel more quickly through the channel in HSG than in USG. Carrier transport efficiency and therefore current driving capacity are increased in HSG. But the electric field near the drain in HSG is higher than that in USG, which is not favourable for hot carrier effect. Figure 4 shows the surface electric field of HSG with different halo doping concentration and length. It is indicated in the figure that increasing halo length makes the electric field peak to move away from the source, delaying the speeding-up of carriers. Increasing doping concentration increases the electric field peak, enhances the speeding-up of carriers. But higher halo doping concentration also increases the electric field near the drain, worsens hot carrier effect. So tradeoff needs to be made between carrier transport efficiency and hot carrier effect.

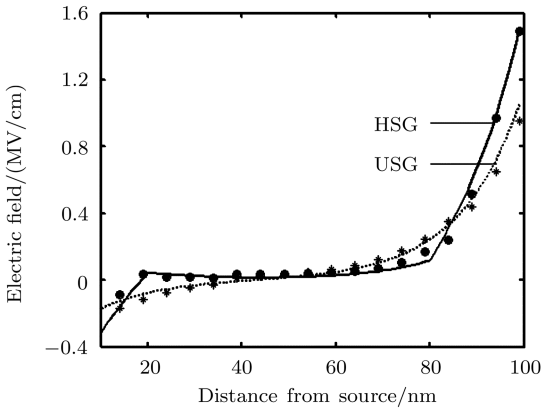


Fig.3. Surface electric field along the channel (V_{ds} = 0.8 V, V_{gs} = 0.2 V).

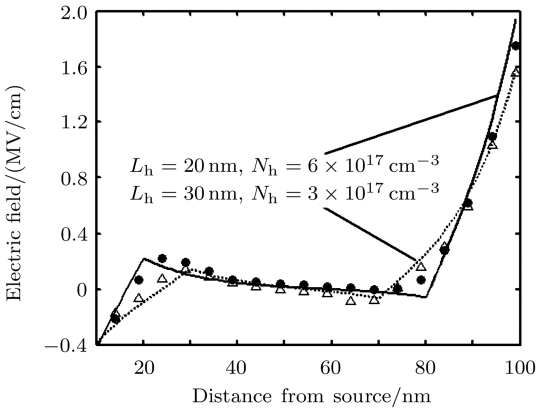


Fig.4. Surface electric field of HSG with different halo structures (V_{ds} = 0.8 V, V_{gs} = 0.2 V).

Figure 5 presents threshold voltage roll-off with gate length of HSG and USG, where V_{th0} is the V_{th} value with a gate length of 200 nm. It shows that the threshold voltage decreases rather faster in USG than in HSG when the gate length is below 80 nm, which indicates that HSG has better suppression of threshold voltage roll-off than USG in sub-100 nm region.

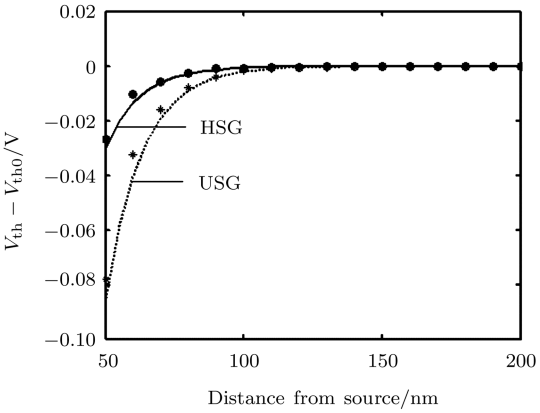


Fig.5. Threshold voltage roll off with gate length (L_h = 20 nm).

Figure 6 shows threshold voltage roll-off of HSG with different halo doping concentration versus gate length. It is shown that the suppression capacity of threshold voltage roll-off is enhanced when the halo doping concentration is increased. The analytical model and numerical simulation indicate that halo length has no evident influence on threshold voltage roll-off.

DIBL can be expressed by $\Delta V_{th}/\Delta V_{ds}$. DIBL variation of HSG and USG with gate length is presented in Fig.7, where $\Delta V_{th} = V_{th}|_{V_{ds}=0} - V_{th}|_{V_{ds}=2}$ and ΔV_{ds} = 2 V. It is evident from the figure that HSG exhibits better suppression of DIBL than USG and higher halo doping concentration can increase DIBL

suppression capacity. Analytical and numerical studies indicate that halo length does not have evident influence on DIBL.

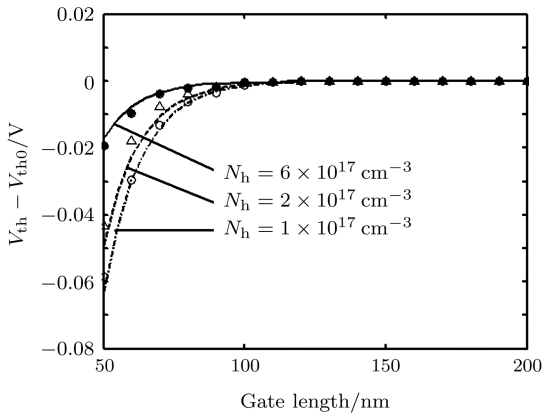


Fig.6. Voltage roll off of HSG with different halo doping concentration ($L_h = 20\,{\rm nm}$).

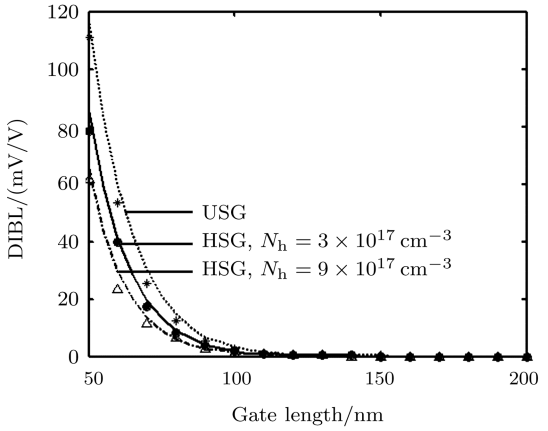


Fig.7. DIBL variation with gate length ($L_h = 20\,{\rm nm}$).

The subthreshold slope variation with gate length is plotted in Fig.8. The subthreshold slope of HSG is a little higher than USG when the gate length is over 100 nm because of the higher halo doping concentration. But it is evident from the figure that HSG has almost the identical subthreshold slope with USG when the gate length is below 100 nm.

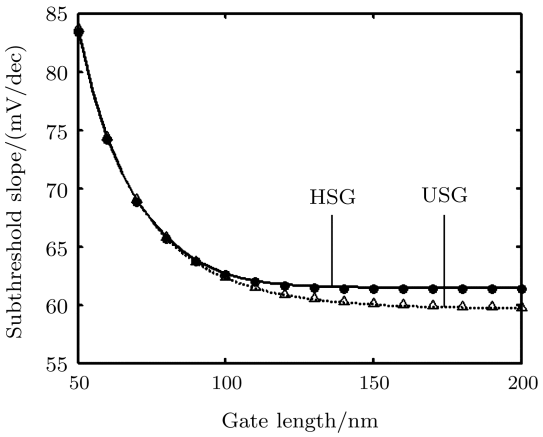


Fig.8. Subthreshold slope variation with gate length.

Figures 2 to 8 show that the analytical models are in good agreement with Davinci.

4. Conclusion

Halo doping profile is used in the sub-100 nm surrounding gate MOSFET to improve scalability. By assuming parabolic potential variation in the radical direction, the Poisson's equation in cylindrical coordinates is solved analytically in the three regions of the fully depleted silicon pillar. 2D analytical surface potential and threshold voltage models are developed for the symmetric halo doped surrounding gate MOSFET. The halo doped device shows better performance in suppressing threshold voltage roll-off and DIBL, and increasing carrier transport efficiency. Higher halo doping concentration is better for improving the performance. The analytical models agree well with the 3D device simulator Davinci of Synopsys.

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