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All-optical error-bit amplitude monitor based on NOT and AND gates in cascaded semiconductor optical amplifiers*

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This paper proposes and simulates a novel all-optical error-bit amplitude monitor based on cross-gain modulation and four-wave mixing in cascaded semiconductor optical amplifiers (SOAs), which function as logic NOT and logic AND, respectively. The proposed scheme is successfully simulated for 40 Gb/s return-to-zero (RZ) signal with different duty cycles. In the first stage, the SOA is followed by a detuning filter to accelerate the gain recovery as well as improve the extinction ratio. A clock probe signal is used to avoid the edge pulse-pairs in the output waveform. Among these RZ formats, 33% RZ format is preferred to obtain the largest eye opening. The normalized error amplitude, defined as error bit amplitude over the standard mark amplitude, has a dynamic range from 0.1 to 0.65 for all RZ formats. The simulations show small input power dynamic range because of the nonlinear gain variation in the first stage. This scheme is competent for nonreturn-to-zero format at 10Gb/s as well.

Keywords: semiconductor optical amplifier, nonlinear optics, optical communications devices
PACC: 4281W, 4265, 4280S

1. Introduction

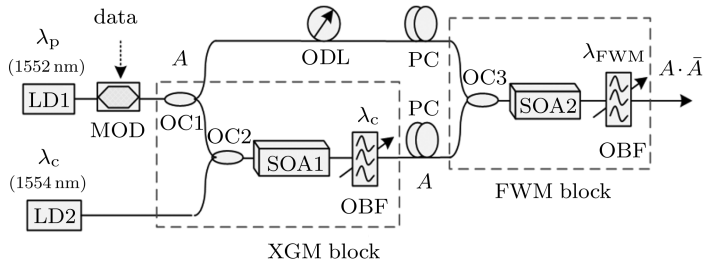
In high capacity optical transport and access networks, the bit-error monitoring is indispensable for optical layer protection and eye monitoring.[1] However, the traditional bit-error monitoring system (BEMS) requires complex optical-electrical-optical conversion.[2] All-optical BEMS is useful in future high speed optical networks since the detected optical error signals can be forwarded to the corresponding network node for processing without optical-electrical conversion. Chan *et al* first demonstrated all-optical error-bit amplitude monitor at 10Gb/s based on two injection-locked Fabry-Pérot laser diodes (FP-LD).[3] This monitor is realized by cascaded logic NOT and NOR functions and two threshold levels determine the error bits. However, the steady injection-locking condition experiences rather long time due to the limited carrier dynamics. In order to realize high speed monitoring, the FP-LD should be replaced by the multiple quantum-well FP-LD. Currently semiconductor optical amplifiers (SOAs) have been well developed to achieve high speed optical signal processing due to the mature semiconductor manufacturing techniques. It is possible to achieve 640 Gb/s wavelength conversion by nonlinear polarization rotation.[4] or by transient cross phase modulation.[5] in the SOA. Inspired by the proposal of Ref.[3], this paper proposes and simulates a novel all-optical error-bit amplitude monitor using two cascaded SOAs, which implement logic NOT based on cross-gain modulation (XGM) and logic AND based on four-wave mixing (FWM), respectively. The operation speed is as high as 40 Gb/s for return-to-zero (RZ) signal monitoring. Although the SOA has slow recovery time with XGM,[6] a detuning filter can compensate the slow recovery time. Moreover, the incident wavelength can be freely adjusted in the wide gain bandwidth of SOA. The dynamic range of the input power and the error bit amplitude are analysed. The monitor for 10 Gb/s nonreturn-to-zero (NRZ) signal is also discussed.

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2. Operation principle and experimental setup

Figure 1(a) shows the operation principle, which consists of two stages of all-optical logic functions. The first stage is logic NOT based on XGM in SOA1, which gets an inverted copy ($\bar{A}$) of the incoming data signal (A). The second stage is logic AND based on FWM in SOA2, which implements the logic AND function ($A \cdot \bar{A}$) of the incoming data and its inverted copy. Therefore only the error bits can be detected by the logic function $A \cdot \bar{A}$. Figure 1(b) shows the truth table of the logic functions. "E" denotes the error bit, $0 < E < 1$. Note that in the first stage, the logic NOT signal is converted to the probe wavelength λ_c, and in the second stage, the logic AND signal is converted to the conjugated wavelength λ_{FWM}, and $\lambda_{FWM} = 2\lambda_c - \lambda_p$, where λ_p is the input data wavelength.



(a)

A	$\bar{A}$	$A \cdot \bar{A}$
	XGM	FWM
1	0	0
E	E	1
0	1	0

(b)

Fig.1. (a) Experimental setup for the BEMS, (b) Truth tables for the logic NOT and AND functions based on cascaded SOAs. PC: polarization controller; MOD: modulator; OC: optical coupler; OBF: optical bandpass filter; ODL: optical delay line. E: error bit, $0 < E < 1$.

It should be noted that, our scheme only serves as the bit-error amplitude detection in optical domain. As for an integral BEMS, one may use an optically controlled switch and an optical logic to count the error bits, or one may use a high speed detector to complete the optical-to-electrical conversion, and a digital logic to count the error bits. The all-optical method is preferred so that the optical advantages with huge bandwidth capacity and immunity to electromagnetic interference can be utilized. There are also some other effects resulting in the bit errors, such as timing jitter and cross talk.

The experimental setup is described in Fig.1(a). The data signal to be monitored is generated by the laser diode (LD1) and modulator (MOD). The data signal is split to two beams. One beam is combined with the continuous wave (CW) probe signal generated by LD2, and launched into SOA1 to experience XGM. The optical bandpass filter (OBF) is used to select the probe wavelength, but proper OBF detuning is necessary to enhance the SOA modulation speed. The output signal is logic NOT of input data signal. Another beam and the logic NOT signal are injected into SOA2 to experience FWM. The following OBF is used to filter out the conjugate light, which is able to monitor the error bits of input data streams.

3. Results and discussions

Two stages of SOAs are simulated with ultrafast gain dynamic model[7] and FWM model.[8] respectively, since different SOA nonlinearities are concerned in each stage. When the ultrafast gain dynamics of SOA followed by an OBF is simulated, the influence of intra-band dynamics, such as spectrum hole burning (SHB) and carrier heating (CH), should be considered.[7,9,10] The influence of intra-band dynamics is modelled by a nonlinear gain suppression factor $\varepsilon = \varepsilon_{CH} + \varepsilon_{SHB}$ associated with SHB and CH effect. Then the material gain can be expressed as $\bar{g} = g_l/(1 + \varepsilon P_{tot})$, where P_{tot} is the input total power coupled into the SOA, g_l is the linear material gain coefficient.

In the simulation, both SOAs have the bias current of 200 mA and the cavity length of 0.35 mm. The input data signal is set as RZ format at first. Some important parameters are set as following. $\lambda_c = 1554$nm, $\lambda_p = 1552$ nm, $\lambda_{FWM} = 1556$ nm, $P_c = 1$ mW and $P_p = 4$ mW for SOA1, $P_c = 5$mW and $P_p = 8$ mW for SOA2, where λ and P denote the wavelength and peak power respectively. Subscript c, p and FWM denote probe light, data light and conjugated light, respectively. Both filters have a bandwidth of 0.4 nm. $\varepsilon_{CH} = 0.3\,W^{-1}$, and $\varepsilon_{SHB} = 0.1\,W^{-1}$.[11] Other parameters can be found in Refs.[7] and [8].

Assume that the RZ signal is modulated at 40 Gb/s with duty cycle of 33%, and the error bits have half amplitude of correct bits '1'. The input data signal is plotted in Fig.2(a). Employing the XGM model for SOA1, we calculate the converted waveform with inverted polarity. However, the SOA1 has a typical recovery time of about 100 ps, therefore the converted waveform has serious pattern effect as well as low extinction ratio. An effective solution uses detuning filter to accelerate the gain recovery.[12] When the filter has a detuning of –0.32 nm (blue shifted), the converted waveform shows good performance, as shown in Fig.2(b). We can see that the converted signal is logic NOT of the input data signal. The converted error bits are located at middle amplitude between bit '0' and bit '1'. According to the FWM model of SOA2, the output waveform at conjugate light λ_{FWM} is calculated in Fig.2(c). All the error bits in the original signals now appear as '1' bits, marked as solid arrow. Note that there are some narrow pulse-pairs in the bit edges, marked as a dashed arrow. These pulse-pairs are caused by the FWM effect of the original signal and its inverted copy in edge durations. In fact, the bit-error monitoring is immune to these pulse-pairs since the pulse-pairs only appear in the edge duration, but not in the middle duration. One can use a synchronized optical clock to sample the signal at middle duration.

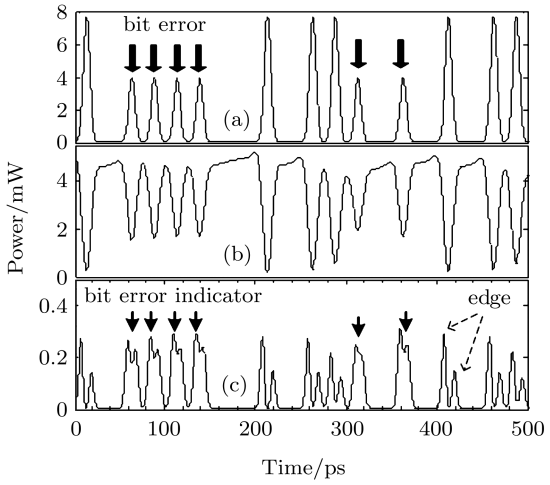


Fig.2. Simulation result for 40 Gb/s RZ signal, the probe signal is continuous wave, (a) the input RZ signal with bit errors, (b) the inverted signal in SOA1, and (c) the error indicator signals in SOA2.

In order to monitor the error bits more clearly, we present an improved scheme to avoid the edge pulse-pairs. The CW probe signal is replaced by a 40 GHz clock signal, which is synchronized with the RZ signal. Then the output of the first stage is still logic NOT due to XGM, but the data format remains RZ format. The clock signal has a peak power of 1mW. Figure 3 demonstrates the monitor with the clock probe. Figure 3(a) is the incoming data signal with error bits. Figure 3(b) shows the inverted waveform in the first stage. We notice that the inverted waveform remains RZ format. The filter with a detuning of –0.32 nm is still necessary to enhance the SOA modulation speed. Figure 3(c) shows the output waveform of the second stage. All the error bits in the original signals are indicated, and no edge pulse-pairs appear.

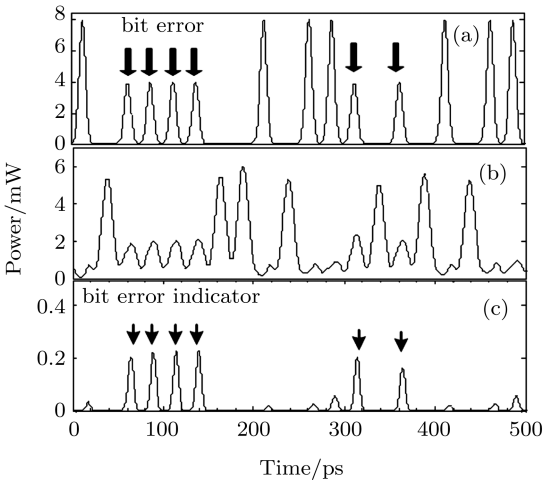


Fig.3. Simulation result for 40Gb/s RZ signal, the probe signal is synchronized clock, (a) the input RZ signal with bit errors, (b) the inverted signal in SOA1, and (c) the error indicator signals in SOA2.

Figure 4 shows the eye diagram of error bit indicator signals in Fig.3(c). Some 'ghost pulses' exist on the base, which is caused by the limited extinction ratio of the inverted waveform. We define the eye opening (EO) as the logarithm of the minimum ratio

between the one power level and zero power level, i.e.

$$\mathrm{EO} = 10\log_{10}\left[\frac{\min(P_1)}{\max(P_0)}\right]. \tag{1}$$

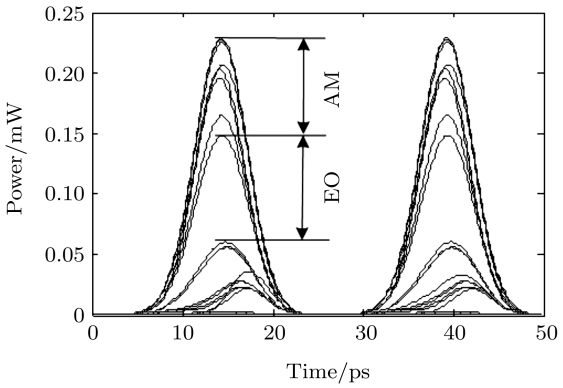


Fig.4. Eye diagram of the error bit indicator signals.

The amplitude modulation (AM) is defined as the logarithm of the ratio of maximum one power level and minimum one power level, i.e.,

$$\mathrm{AM} = 10\log_{10}\left[\frac{\max(P_1)}{\min(P_1)}\right]. \tag{2}$$

Where P_0 and P_1 are zero power level and one power level respectively.

We also define the normalized error amplitude (NEA) as the error bit power over bits '1' power. The NEA represents the effective monitoring range of error bits. Figure 5 shows the EO of output signals as a function of the NEA at RZ duty cycles of 33%, 50% and 67%. As the NEA increases, the EO increases first, and then decreases subsequently. It is interesting that the largest EO is obtained at NEA of 0.25, but not 0.5 (half amplitude). Since the detuning filter is necessary to accelerate the gain recovery in the first stage, one can consider SOA1 and the detuning filter as an integral system. The system gain is nonlinear variation, as shown in Fig.6. Because the input probe is a synchronized clock signal, the output of the first stage is still RZ format, but the data sequence is a NOT gate of the input pump data sequence. When the NEA is 0.25, i.e., the error bit power is 1mW in the simulation, we can see that the output power of error bit is just half amplitude, which is helpful for FWM effect in the second stage. However, when the NEA is 0.5, the output power of error bits is very low. Therefore, the optimal EO is obtained when the NEA is 0.25, but not 0.5.

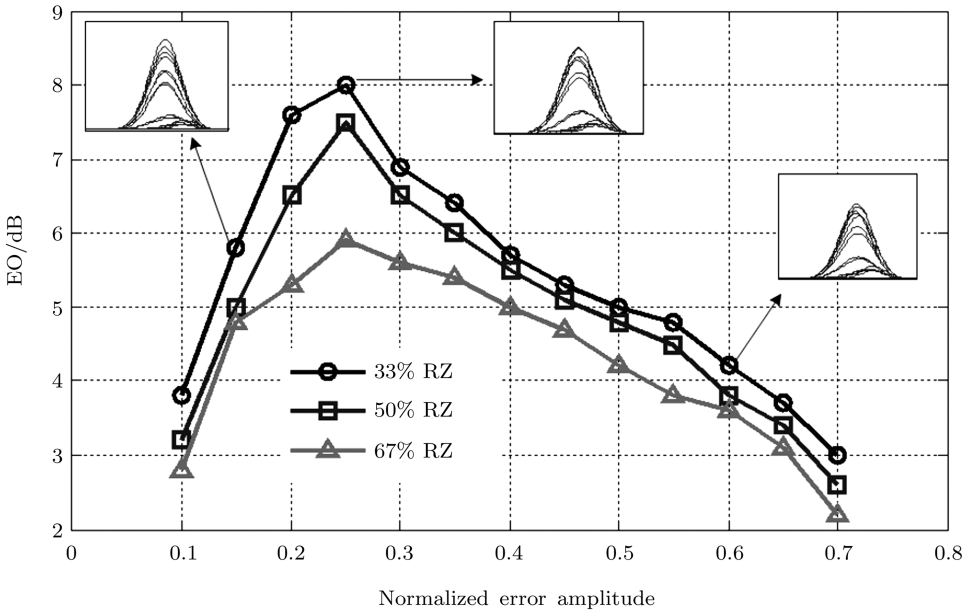


Fig.5. Eye opening as a function of the normalized error amplitude when the RZ duty cycle is 33%, 50%, and 67% respectively.

The insets of Fig.5 are the corresponding eye diagrams of 33% RZ signal monitoring. Among the RZ formats of different duty cycles, 33% RZ format is preferred to obtain the largest EO. In the first stage, 33% RZ pulses can induce large phase variation and frequency chirps, and the detuning filter can accelerate the gain recovery easily and obtain inverted signals with high performances. We define that the amplitude

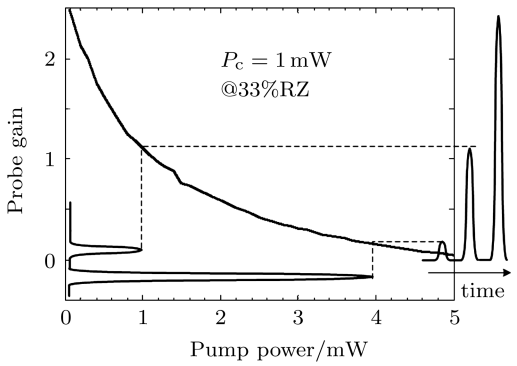


Fig.6. Probe gain as a function of the input pump power by considering SOA1 and its following detuning filter as a whole system.

monitor fails to work when the EO is lower than 3 dB. From Fig.5, one can see that the NEA has a dynamic range from 0.1 to 0.65 for all RZ formats. This means that all bits with normalized amplitudes between 0.1 and 0.65 will be detected as error signals.

We also investigate the input power dynamic range. Figure 7 shows the output EO and AM as a function of input pump peak power when the probe peak power is 1mW and 0.5 mW, respectively. The NEA is 0.5, and the RZ duty cycle is 33%. The AM describes the amplitude fluctuation of bits '1'. When the AM is larger than 3 dB, the output performance is rather bad, and we define that the monitor fails to work in such a case. As for 1 mW probe injection, both EO and AM increase as the pump peak power increases. One can see that the pump power should be higher than 2.4 mW in order to get the EO over 3 dB, and the pump power should be lower than 5.6 mW so that the AM is less than 3 dB. Therefore, the input pump power has a dynamic range from 2.4 mW to 5.6 mW, which is a limited range. Similarly, when the probe peak power is 0.5 mW, we get the small power dynamic range from 1.6 mW to 3.2 mW. The small power dynamic range results from the nonlinear gain variation, shown in Fig.6. For example, when the pump peak power is very high, its half amplitude, the error bit, has also a high power. The error bits will be converted to zero, but not half amplitude in the first stage. Conversely, if the pump power is very low, the inverted waveform could be obtained with very low extinction ratio, which definitely degrades the output performances of the second stage. Therefore, the monitor has a small power dynamic range. From Fig.7, we can see that the EO increases as the pump peak power increases. Therefore the NEA will have a larger dynamic range if the input pump power increases.

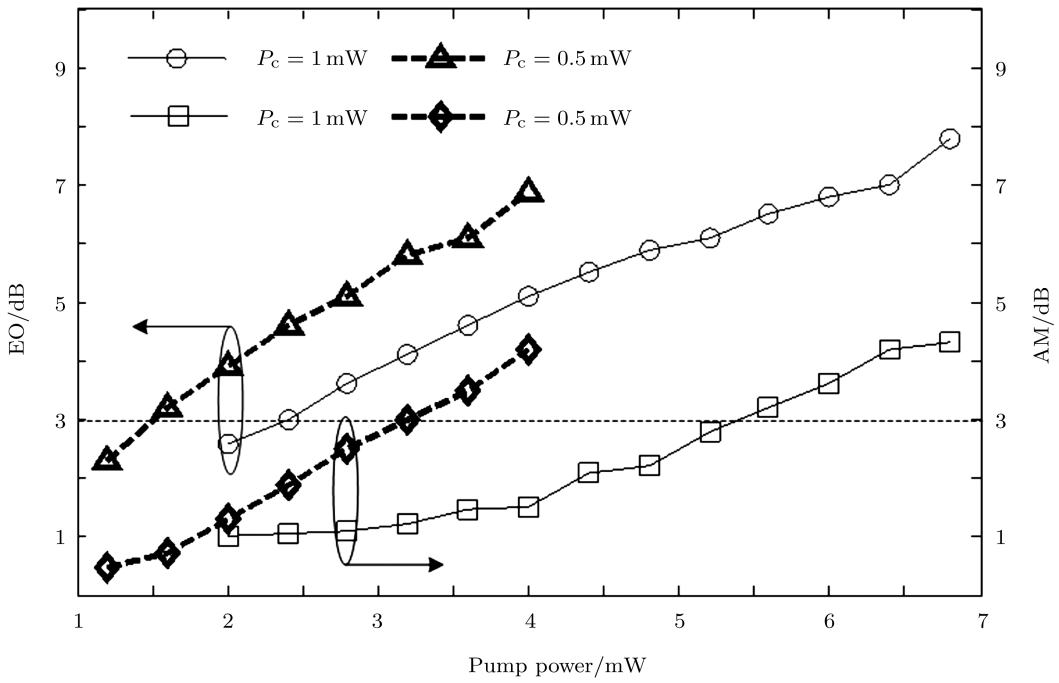


Fig.7. EO and AM of output eye diagrams as a function of the pump peak power when the input probe power is 1 mW and 0.5 mW, respectively. The NEA is 0.5, and the RZ duty cycle is 33%.

We also simulate the monitor for 10 Gb/s NRZ signal. In such a case, the probe signal is CW light. Figures 8(a)–8(c) show the temporal waveforms of input NRZ signal at 10 Gb/s, its inverted waveform in SOA1, and its error indicator signals in SOA2, respectively. The probe power is 1mW, and the OBF has no detuning. In the simulation, the error bits have different amplitudes. From Fig.8(c) we can see that all the error bits are identified, marked as solid arrow. The inset is the eye diagram of error indicator signals. Good EO is shown, and the edge pulse-pairs appear at the rising or falling edges. The edge pulse-pairs have no impacts on the bit-error monitoring. Although our monitor is competent for 10 Gb/s NRZ format, operation speed beyond 40 Gb/s will not be effective in our monitor because the detuning filter fails to enhance SOA gain dynamics with NRZ format.

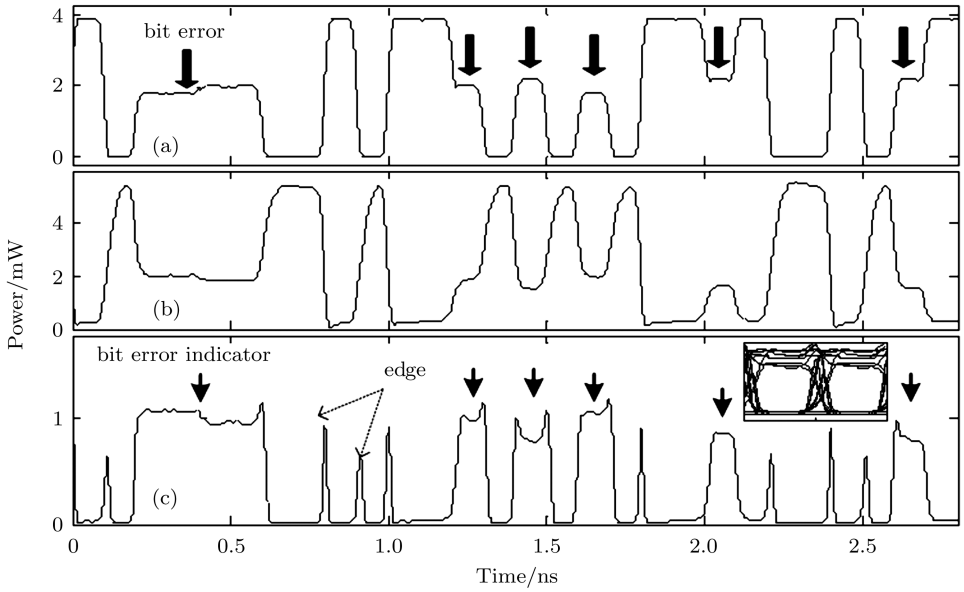


Fig.8. Simulation result for the synchronized temporal waveforms of (a) the input NRZ signal with bit errors at 10 Gb/s, (b) the inverted signal in SOA1, and (c) the error indicator signals in SOA2.

4. Conclusion

We have proposed and simulated all-optical error-bit amplitude monitor based on two cascaded SOAs, which realize logic NOT due to XGM and logic AND due to FWM respectively. We simulate the monitor for 40 Gb/s RZ signals with duty cycle of 33%, 50% and 67%, respectively. A clock probe signal is used to avoid the edge pulse-pairs in the output waveform. Among these RZ formats, 33% RZ format is preferred to obtain the largest EO. The normalized error amplitude has a dynamic range from 0.1 to 0.65 for all RZ formats. The monitor shows small input power dynamic range because of the nonlinear gain variation in the first stage. Our scheme is competent for 10 Gb/s NRZ format as well.

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