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The analysis of the integral gated mode single photon detector*

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This paper critically analyses and simulates the circuit configuration of the integral gated mode single photon detector which is proposed for eliminating the transient spikes problem of conventional gated mode single photon detector. The relationship between the values of the circuit elements and the effect of transient spikes cancellation has been obtained. With particular emphasis, the bias voltage of the avalanche photodiode and the output signal voltage of the integrator have been calculated. The obtained analysis results indicate that the output signal voltage of the integrator only relates to the total quantity of electricity of the avalanche charges by choosing the correct values of the circuit elements and integral time interval. These results can be used to optimize the performance of single photon detectors and provide guides for the design of single photon detectors.

Keywords: single photon detector, quantum cryptography, integrator, gated mode
PACC: 0762, 0367

1. Introduction

The single photon detectors (SPD) used at telecom wavelengths have become a focus with the boom of quantum cryptography technique.[1−3] At present, the best choice is the InGaAs/InP avalanche photodiode (APD) with separate absorption multiplication (SAM) at telecom wavelengths. The APD is operated above its breakdown voltage, which is called Geiger mode operation,[4] so that a photon induced avalanche can grow into a macroscopic pulse, then the avalanche should be quenched to protect the APD from over current. There are basically three techniques to practice Geiger mode operation: active quenching,[4] passive quenching[5] and gated mode quenching.[6] The process technology for InGaAs based detector is not as mature as that for silicon. Hence, generation–recombination centres and trap densities are much higher in these materials which lead to high dark counts probability and high afterpulse probability.[7]

The gated mode operation is the most effective method to decrease the dark count probability and afterpulse probability by using the gate pulses synchronized with the arrival of photons.[5] The APD is only gated on during short time interval, and if the APD has been gated off for a sufficiently long time interval much longer than the trap release time before ringing it into operation, the trapped carriers have been almost all released and do not trigger the afterpulse count.

Although this method works well, the use of short gate pulses leads to the following drawback. The gate pulses coupled to the load resistor through the APD's junction capacitance produce two transient spikes that obscure the photon induced avalanche pulses. A high threshold voltage of the pulse height discriminator is necessary to avoid the transient spikes triggering false counts. Generally, in a pulse height distribution of the APD output signals for single photons, the probability that lower-height pulses are generated is greater than that for higher-height pulses.[8] Therefore, higher threshold voltage rejects more avalanche pulses and decreases the detection efficiency of the SPD. Although increasing bias voltage can compensate for this, it also results in an increase of dark count probability and afterpulse probability.

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The transient spikes are the main problem that degrades the performance of gated mode single photon detector (GSPD) when the APD is certain. Many of the recent works on GSPDs have focused on solving this problem. These works include the coaxial cable reflection lines scheme,[9,10] the two similar APDs balanced scheme,[11] the capacitor balanced scheme,[12] and the discharge pulse counting scheme.[13] In our previous work we demonstrated an integral GSPD (JGSPD) proposal at telecom wavelength.[14]

In this paper, the character of the IGSPD is analysed with particular emphasis on bias voltage and output signal voltage. The relationship between the values of the circuit elements and the effect of transient spikes cancellation has been obtained. And to test the performance of the proposal, the circuit is simulated by using OrCAD 9.2.

2. Configuration of the proposed circuit

The simplified schematic of the IGSPD is shown in Fig.1. The APD is reverse biased by an alternating current (AC) coupled bias tee and an integral capacitor $C_{\rm L}$ is employed in the single photon detector instead of the 50Ω load resistor. The gate pulse and the avalanche current during a same detection cycle are integrated by the integral capacitor. The voltage across $C_{\rm L}$ increases at a rate proportional to the number of the integrated charges. This integrated voltage is amplified by the charge amplifier for single photon counting. The integral capacitor is discharged by an electronic switch in order to reset the circuit for the next detection.

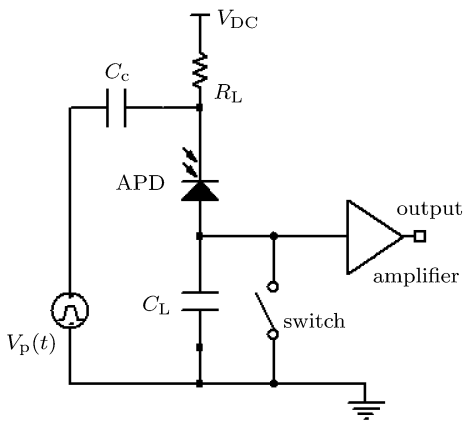


Fig.1. Schematic of the integral gated mode single photon detector.

The equivalent circuit of the main circuit for AC signal analysis is shown in Fig.2. The circuit in broken line is the equivalent circuit of the APD, where $i_{\rm APD}(t)$ is the body current of the APD which includes the dark current $i_{\rm dark}(t)$ and avalanche current $i_{\rm avalanche}(t)$, and $C_{\rm d}(t)$ is the junction capacitance which varies with the bias voltage $v_{\rm A}(t)$. $C_{\rm c}$ is the AC coupling capacitor, $R_{\rm L}$ is the ballast resistor, $R_{\rm i}$ is the input resistance of the charge amplifier, and $C_{\rm s}$ is the stray capacitance (capacitance to ground of the APD terminal connected to $R_{\rm L}$, typically a few picofarads).

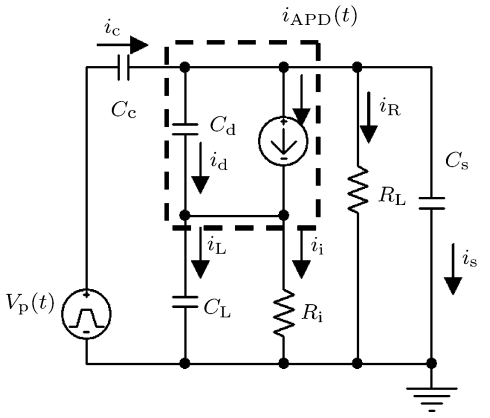


Fig.2. Schematic of the equivalent circuit of the main circuit for AC signals analysis.

3. Characteristic analysis of the IGSPD bias circuit

The functions of the bias circuit are producing the bias voltage $v_{\rm A}(t)$ for the APD operation and sensing the avalanche current of the APD to generate an output signal voltage $v_{\rm L}(t)$ for single photon discrimination.

According to Fig.2, by applying Kirchhoff theory, we can obtain the following equations:

$$v_{\rm p}(t) = v_{\rm c}(t) + v_{\rm A}(t) + v_{\rm L}(t), \tag{1}$$

$$i_{\rm c}(t) = i_{\rm R}(t) + i_{\rm L}(t) + i_{\rm i}(t) + i_{\rm s}(t), \tag{2}$$

$$v_{\rm A}(t) + v_{\rm L}(t) = v_{\rm s}(t) = R_{\rm L} i_{\rm R}(t), \tag{3}$$

$$i_{\rm d}(t) + i_{\rm APD}(t) = i_{\rm L}(t) + i_{\rm i}(t), \tag{4}$$

$$i_{\rm d}(t) = \frac{{\rm d}C_{\rm d}(t)v_{\rm A}(t)}{{\rm d}t}, \tag{5}$$

$$i_{\rm L}(t) = C_{\rm L}\frac{{\rm d}v_{\rm L}(t)}{{\rm d}t}, \tag{6}$$

$$i_{\rm c}(t) = C_{\rm c}\frac{{\rm d}v_{\rm c}(t)}{{\rm d}t}, \tag{7}$$

$$i_{\rm s}(t) = C_{\rm s}\frac{{\rm d}v_{\rm s}(t)}{{\rm d}t}, \tag{8}$$

$$i_{\mathrm{R}}(t)=\frac{v_{\mathrm{s}}(t)}{R_{\mathrm{L}}}, \tag{9}$$

$$i_{\mathrm{i}}(t)=\frac{v_{\mathrm{L}}(t)}{R_{\mathrm{i}}}, \tag{10}$$

where $v_{\mathrm{p}}(t)$ is the gate pulse voltage, $v_{\mathrm{c}}(t)$ is the voltage across the capacitor C_{c}, $v_{\mathrm{A}}(t)$ is the voltage across the capacitor $C_{\mathrm{d}}(t)$, $v_{\mathrm{s}}(t)$ is the voltage across the capacitor C_{s}, $v_{\mathrm{L}}(t)$ is the voltage across the integral capacitor C_{L}, $i_{\mathrm{c}}(t)$ is the current through C_{c}, $i_{\mathrm{d}}(t)$ is the current through $C_{\mathrm{d}}(t)$, $i_{\mathrm{s}}(t)$ is the current through C_{s}, $i_{\mathrm{L}}(t)$ is the current through C_{L}, $i_{\mathrm{R}}(t)$ is the current flowing through R_{L}, and $i_{\mathrm{i}}(t)$ is the current flowing through R_{i}.

Substituting Eqs.(5) and (6) into Eq.(4), we can obtain

$$\frac{\mathrm{d}C_{\mathrm{d}}(t)v_{\mathrm{A}}(t)}{\mathrm{d}t}=C_{\mathrm{L}}\frac{\mathrm{d}v_{\mathrm{L}}(t)}{\mathrm{d}t}+i_{\mathrm{i}}(t)-i_{\mathrm{APD}}(t). \tag{11}$$

The range of integration can be set by controlling the open and close time of the switch. Designating the initial integrating time is before the arrival of gate pulse, the initial condition of the circuit can be written as

$$v_{\mathrm{c}}(0)=v_{\mathrm{s}}(0)=v_{\mathrm{A}}(0)=v_{\mathrm{L}}(0)=0, \tag{12}$$

$$C_{\mathrm{d}}(0)=C_{\mathrm{DC}}. \tag{13}$$

where C_{DC} is the value of the junction capacitance when the bias voltage equates to the DC bias voltage V_{DC}.

By integrating between the times 0 and t and between the corresponding voltages $v_{\mathrm{A}}(0)$ and $v_{\mathrm{A}}(t)$, considering the initial condition of the circuit, we can obtain

$$v_{\mathrm{A}}(t)=\frac{C_{\mathrm{L}}}{C_{\mathrm{d}}(t)}v_{\mathrm{L}}(t)+\frac{1}{C_{\mathrm{d}}(t)}\int_0^t[i_{\mathrm{i}}(t)-i_{\mathrm{APD}}(t)]\mathrm{d}t. \tag{14}$$

v_{s} can be obtained from Eqs.(3) and (14),

$$v_{\mathrm{s}}=\frac{C_{\mathrm{L}}+C_{\mathrm{d}}(t)}{C_{\mathrm{d}}(t)}v_{\mathrm{L}}(t)+\frac{1}{C_{\mathrm{d}}(t)}\int_0^t[i_{\mathrm{i}}(t)-i_{\mathrm{APD}}(t)]\mathrm{d}t. \tag{15}$$

Substituting Eqs.(6), (7) and (8) into Eq.(2), we can obtain

$$\frac{\mathrm{d}v_{\mathrm{c}}(\mathrm{t})}{\mathrm{d}t}=\frac{v_{\mathrm{s}}(t)}{C_{\mathrm{c}}R_{\mathrm{L}}}+\frac{C_{\mathrm{L}}}{C_{\mathrm{c}}}\frac{\mathrm{d}v_{\mathrm{L}}(t)}{\mathrm{d}t}+\frac{i_{\mathrm{i}}(\mathrm{t})}{C_{\mathrm{c}}}+\frac{C_{\mathrm{s}}}{C_{\mathrm{c}}}\frac{\mathrm{d}v_{\mathrm{s}}(t)}{\mathrm{d}t}. \tag{16}$$

Then, by integrating between the times 0 and t and between the corresponding voltages $v_{\mathrm{c}}(0)$ and $v_{\mathrm{c}}(t)$, the solution of equation (16) can be written as

$$\begin{aligned}v_{\mathrm{c}}(\mathrm{t})=&\int_0^t\left[\frac{v_{\mathrm{s}}(t)}{C_{\mathrm{c}}R_{\mathrm{L}}}+\frac{i_{\mathrm{i}}(\mathrm{t})}{C_{\mathrm{c}}}\right]\mathrm{d}t\\&+\frac{C_{\mathrm{L}}}{C_{\mathrm{c}}}v_{\mathrm{L}}(t)+\frac{C_{\mathrm{s}}}{C_{\mathrm{c}}}v_{\mathrm{s}}(t).\end{aligned} \tag{17}$$

Substituting Eq.(15) into Eq.(17), we can obtain

$$\begin{aligned}v_{\mathrm{c}}(t)=&\frac{C_{\mathrm{d}}(t)C_{\mathrm{L}}+C_{\mathrm{s}}C_{\mathrm{L}}+C_{\mathrm{s}}C_{\mathrm{d}}(t)}{C_{\mathrm{c}}C_{\mathrm{d}}(t)}v_{\mathrm{L}}(t)\\&+\frac{1}{C_{\mathrm{c}}R_{\mathrm{L}}}\int_0^t\frac{C_{\mathrm{L}}+C_{\mathrm{d}}(t)}{C_{\mathrm{d}}(t)}v_{\mathrm{L}}(t)\mathrm{d}t\\&-\int_0^t\left[\frac{C_{\mathrm{s}}}{C_{\mathrm{c}}C_{\mathrm{d}}(t)}i_{\mathrm{APD}}(t)\right.\\&\left.+\frac{1}{C_{\mathrm{c}}C_{\mathrm{d}}(t)R_{\mathrm{L}}}\int_0^t i_{\mathrm{APD}}(\xi)\mathrm{d}\xi\right]\mathrm{d}t\\&+\int_0^t\left[\frac{C_{\mathrm{s}}}{C_{\mathrm{c}}C_{\mathrm{d}}(t)}i_{\mathrm{i}}(t)+\frac{1}{C_{\mathrm{c}}C_{\mathrm{d}}(t)R_{\mathrm{L}}}\right.\\&\left.\times\int_0^t i_{\mathrm{i}}(\xi)\mathrm{d}\xi\right]\mathrm{d}t+\int_0^t\frac{i_{\mathrm{i}}(t)}{C_{\mathrm{c}}}\mathrm{d}t.\end{aligned} \tag{18}$$

The first term is derived from gate pulse divided by the capacitive voltage divider composed of C_{c}, C_{s}, $C_{\mathrm{d}}(t)$ and C_{L}. C_{s}, $C_{\mathrm{d}}(t)$ and C_{L} are typically of the same order of pF. To avoid the voltage pulse actually applied to the APD being attenuated by C_{c}, it is advisable to minimize the relative loss by employing a sufficiently high C_{c}[4]:

$$C_{\mathrm{c}}\geq 100\left(\frac{C_{\mathrm{d}}(t)C_{\mathrm{L}}}{C_{\mathrm{d}}(t)+C_{\mathrm{L}}}+C_{\mathrm{s}}\right). \tag{19}$$

Therefore, in comparison with $V_{\mathrm{L}}(t)$, the first term approaches to zero. The second term is the decaying of the first term caused by the current flowing through R_{L} and can be given as $\frac{t}{C_{\mathrm{c}}R_{\mathrm{L}}}\overline{\frac{C_{\mathrm{L}}+C_{\mathrm{d}}(t)}{C_{\mathrm{d}}(t)}v_{\mathrm{L}}(t)}$, where $\overline{\frac{C_{\mathrm{L}}+C_{\mathrm{d}}(t)}{C_{\mathrm{d}}(t)}v_{\mathrm{L}}(t)}$ is the mean value of $\frac{C_{\mathrm{L}}+C_{\mathrm{d}}(t)}{C_{\mathrm{d}}(t)}v_{\mathrm{L}}(t)$. $C_{\mathrm{c}}R_{\mathrm{L}}$ has the dimensions of time, thus $\frac{R_{\mathrm{L}}C_{\mathrm{c}}}{t}$ is a dimensionless factor. To avoid the modified waveform of the gate pulses, it is advised that

$$\frac{R_{\mathrm{L}}C_{\mathrm{c}}}{t}\overline{\frac{C_{\mathrm{L}}+C_{\mathrm{d}}(t)}{C_{\mathrm{d}}(t)}}\geq 100. \tag{20}$$

Therefore, in comparison with $V_{\mathrm{L}}(t)$, the second term approaches to zero. The third term is derived from the current flowing through the APD, which also approaches to zero, when inequalities (19) and (20) are satisfied. The fourth and fifth term are derived from the input current of the charge amplifier, considering the input current of the charge amplifier is of the order of pA, we find that the dark current of the APD $i_{\mathrm{dark}}(t)$ is typically several nA and the avalanche current $i_{\mathrm{avalanche}}(t)$ is typically of order of mA, which also approaches to zero, when inequalities (19) and (20) are satisfied.

As analysed above, when

$$\frac{R_{\rm L}C_{\rm c}}{t}\overline{\frac{C_{\rm L}+C_{\rm d}(t)}{C_{\rm d}(t)}} \geq 100$$

and

$$C_{\rm c} \geq 100(\frac{C_{\rm d}(t)C_{\rm L}}{C_{\rm d}(t)+C_{\rm L}}+C_{\rm s}),$$

in comparison with $V_{\rm L}(t)$, $v_{\rm C}(t)$ approaches to zero.

Substituting Eq.(14) into Eq.(1) and a little manipulation, we can obtain an integral equation

$$\begin{aligned} v_{\rm p}(t) =& \frac{C_{\rm L}+C_{\rm d}(t)}{C_{\rm d}(t)}v_{\rm L}(t) \\ &+ \frac{1}{C_{\rm d}(t)}\int_0^t [i_{\rm i}(t)-i_{\rm APD}(t)]{\rm d}t + v_{\rm c}(t) \\ \approx& \frac{C_{\rm L}+C_{\rm d}(t)}{C_{\rm d}(t)}v_{\rm L}(t) \\ &+ \frac{1}{C_{\rm d}(t)}\int_0^t [i_{\rm i}(t)-i_{\rm APD}(t)]{\rm d}t. \end{aligned} \tag{21}$$

By a little manipulation, $v_{\rm L}(t)$ can be given as

$$\begin{aligned} v_{\rm L}(t) =& \frac{C_{\rm d}(t)}{C_{\rm L}+C_{\rm d}(t)}v_{\rm p}(t) \\ &- \frac{1}{C_{\rm L}+C_{\rm d}(t)}\int_0^t [i_{\rm i}(t)-i_{\rm APD}(t)]{\rm d}t \\ =& \frac{C_{\rm d}(t)}{C_{\rm L}+C_{\rm d}(t)}v_{\rm p}(t) - \frac{1}{C_{\rm L}+C_{\rm d}(t)}\int_0^t i_{\rm i}(t){\rm d}t \\ &+ \frac{1}{C_{\rm L}+C_{\rm d}(t)}\int_0^t i_{\rm APD}(t)]{\rm d}t. \end{aligned} \tag{22}$$

Considering the order of $i_{\rm avalanche}(t)$, $i_{\rm dark}(t)$ and $i_{\rm i}(t)$, we can write approximately Eq.(22) as

$$\begin{aligned} v_{\rm L}(t) =& \frac{C_{\rm d}(t)}{C_{\rm L}+C_{\rm d}(t)}v_{\rm p}(t) \\ &+ \frac{1}{C_{\rm L}+C_{\rm d}(t)}\int_0^t i_{\rm avalanche}(t){\rm d}t. \end{aligned} \tag{23}$$

Therefore, when the gate pulse becomes zero, the transient spikes can be eliminated, and because $v_{\rm p}(t) = v_{\rm p}(0) = 0$, then $C_{\rm d}(t) = C_{\rm d}(0) = C_{\rm DC}$ and $v_{\rm L}(t)$ can be given as

$$\begin{aligned} v_{\rm L}(t) =& \frac{1}{C_{\rm L}+C_{\rm DC}}\int_0^t i_{\rm avalanche}(t){\rm d}t \\ =& \frac{Q(t)}{C_{\rm L}+C_{\rm DC}}, \end{aligned} \tag{24}$$

where $Q(t) = \int_0^t i_{\rm avalanche}(t){\rm d}t$ is the quantity of electricity of the avalanche charges. According to Eq.(24), if the range of integration includes the gate pulse, the total charges injected into the integral capacitor by the gate pulse are zero, even though the junction capacitance of the APD varies during the integral time interval. Therefore the output voltage of the charge amplifier is only in proportion to the number of avalanche charges. The transient spikes can be eliminated completely independent of height, duration, shape, symmetry of the gate pulses, or type of APD even if without any regulation.

By substituting Eq.(23) into Eq.(14) and a little manipulation, we can derive the voltage pulse actually applied to the detector from

$$\begin{aligned} v_{\rm A}(t) =& \frac{C_{\rm L}}{C_{\rm L}+C_{\rm d}(t)}v_{\rm p}(t) \\ &- \frac{1}{C_{\rm L}+C_{\rm d}(t)}\int_0^t i_{\rm avalanche}(t){\rm d}t. \end{aligned} \tag{25}$$

The bias voltage before the avalanche can be simplified as

$$v_{\rm bias}(t) = \frac{C_{\rm L}}{C_{\rm L}+C_{\rm d}(t)}v_{\rm p}(t). \tag{26}$$

If the avalanche happens, the bias voltage decreases

$$\begin{aligned} \Delta v_{\rm A}(t) =& -\frac{1}{C_{\rm L}+C_{\rm d}(t)}\int_0^t i_{\rm APD}(t){\rm d}t \\ =& -\frac{Q(t)}{C_{\rm L}+C_{\rm d}(t)}. \end{aligned} \tag{27}$$

Considering that this decline is persistent until the electronic switch resets the circuit, the APD can also be self-quenched besides quenched by gate termination. And the total quantity of electricity of avalanche charges is certain

$$Q_{\rm pc} = [C_{\rm L}+C_{\rm d}(t)][V_{\rm p}+V_{\rm DC}-V_{\rm q}], \tag{28}$$

where $V_{\rm p}$ is the amplitude of gate pulse, and $V_{\rm q}$ is the voltage at which quenching occurs. In most computations $V_{\rm q}$ can be assumed practically equal to the avalanche voltage $V_{\rm B}$ although it is slightly higher.[4]

4. Simulation result

By means of OrCAD 9.2, we simulated the performance of the IGSPD with particular emphasis on the bias voltage and the output signal voltage. The default simulation parameters are: 5 ns during time, 0.5 ns fallen time, 0.5 ns rise time, and 5 V peak to peak value of the gate pulse. Because the output signal voltage of the IGSPD is independent on the waveform of the avalanche pulse as analysed above, the

avalanche pulse is defined as a current pulse of 1ns during time, 0.5 ns fallen time, 0.5 ns rise time, and 1 mA peak to peak value. The junction capacitance of APD $C_{\rm d}$ is 0.5 pF. The AC coupling capacitor $C_{\rm c}$ is 0.1 μF. The ballast resistor $R_{\rm L}$ is 100 kΩ. The input resistance of the charge amplifier $R_{\rm i}$ is 100 GΩ, and the stray capacitance $C_{\rm s}$ is 1pF. Additionally, the integral capacitor is replaced by a 50 Ω resistor for the conventional GSPD simulation.

Figure 3 shows the comparison of output waveform of the conventional GSPD and the IGSPD. The top curve is the waveform of gate pulse, the second is the waveform of avalanche current pulse, the third is the output waveform of the conventional GSPD, and the fourth is the output waveform of the IGSPD. The APD's junction capacitance and the load resistance composed a differentiator in the conventional GSPD. The transient spikes voltage are given by

$$v_{\rm o} = -R_{\rm L}C_{\rm d}\frac{{\rm d}v_{\rm p}(t)}{{\rm d}t}. \tag{29}$$

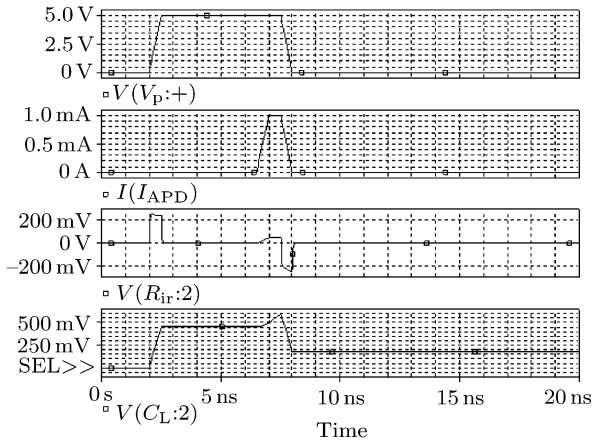


Fig.3. Comparison between the outputs of the conventional GSPD (gate quenched by gate termination) and the IGSPD.

One can see the two spikes occur at the rise and fall edge of the gate pulse, and the peak signal produced by the avalanche current of order of 1 mA is much smaller than the positive spike. Therefore higher avalanche current or transient spikes cancellation is required for single photon discrimination.

The output waveform of the IGSPD shows the integral effect. The integral capacitor is charged by the rise edge of the gate pulse firstly, and then charged by the avalanche current. The voltage across the integral capacitor increases continually and reaches a peak value until the fall edge arrives. After the gate pulse the output voltage remains at $\dfrac{Q(t)}{C_{\rm L}+C_{\rm DC}}$.

Figure 4 is the effect of transient spikes cancellation with different gate pulse amplitude from 3 V to 6 V with the increment of 1 V, when avalanche does not happen. Though the gate pulse divided by the capacitive voltage divider increases, the output voltage stays zero after the gate pulse.

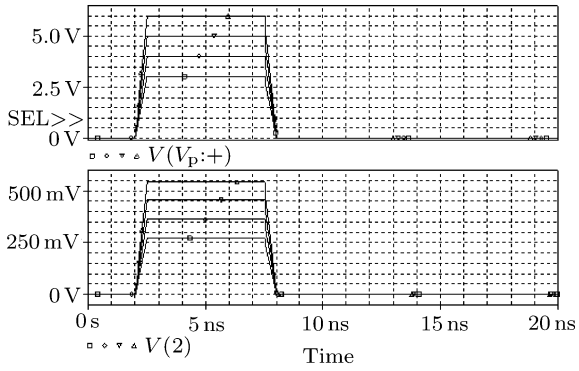


Fig.4. The effect of transient spikes cancellation with different gate pulse amplitude from 3 V to 6 V with the increment of 1 V.

Figure 5 is the output signal waveforms corresponding to different avalanche currents from 0 to 3 mA with the increment of 1 mA. The bottom trace corresponds to the output signal waveform without avalanche and the higher the currents are, the upper the traces are.

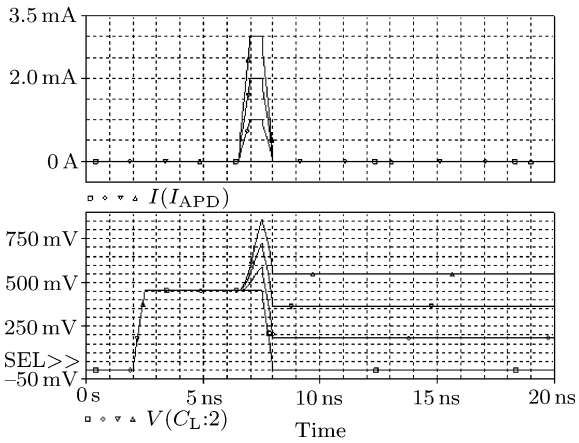


Fig.5. The output signal waveforms corresponding to different avalanche currents from 0 to 3 mA with the increment of 1 mA.

Figure 6 shows the bias voltage with different avalanche current from 0 to 3 mA with the increment of 1 mA. Because $v_{\rm p}(t) \approx v_{\rm A}(t) + v_{\rm L}(t)$, $v_{\rm A}(t)$ drops with the increase of the avalanche current.

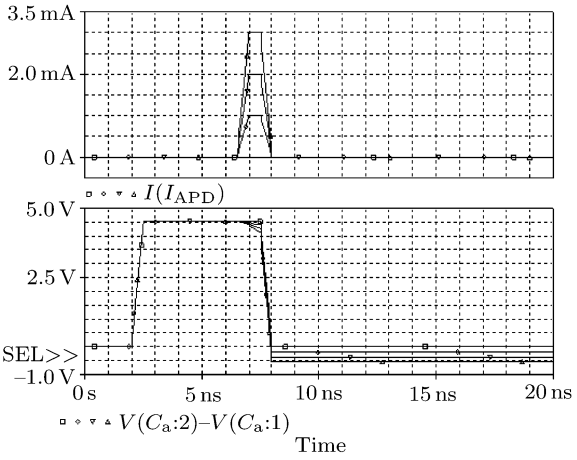


Fig.6. The bias voltage with different avalanche current from 0 to 3 mA with the increment of 1 mA.

5. Experimental results

The experimental results of transient spikes cancellations we achieve are shown in Fig.7. Where the

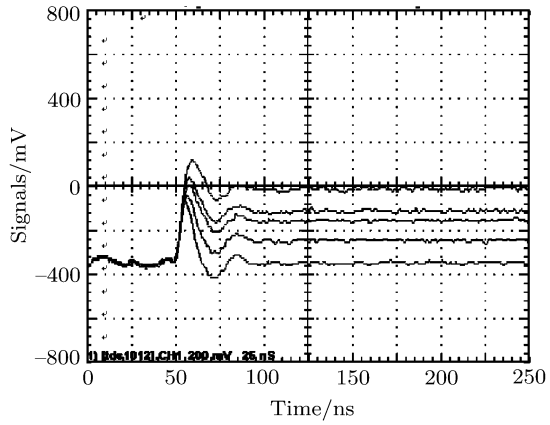


Fig.7. The experimental output waveforms of the charge amplifier responding to single photon incidence.

gate pulses of 5.13 ns FWHM and 4.4 V peak to peak value are applied to the APD after they combined with DC bias of 43.1 V, the integral capacitor is 33 pF and a fast field effect transistor input operational amplifier AD8067 is employed as a +10 gain charge amplifier. Its output waveforms are similar with the simulation results although they are spread wide by the relative slow amplifier. Cancelling the spikes enables us to reduce the threshold voltage of the discriminator and thus decrease bias voltage, which reduces the dark count probability without sacrificing detection efficiency. Therefore the optimal excess bias voltage of the IGSPD is 0.9 V. The threshold voltage of the discriminator of the IGSPD can be set at 20 mV. Considering the amplifier gain of +10 and a 33 pF integral capacitance, we find that the avalanche pulses whose charge number exceeds 0.066pC can trigger a count. Therefore a single photon detection efficiency of 29.9% at dark count probability per gate $P_{\rm D} = 5.57 \times 10^{-6}$/gate has been achieved. The single photon detection performance of the IGSPD is shown in Fig.8 (△) and (□) at $V_{\rm E}$=1.3 V and $V_{\rm E}$=0.9 V, respectively.

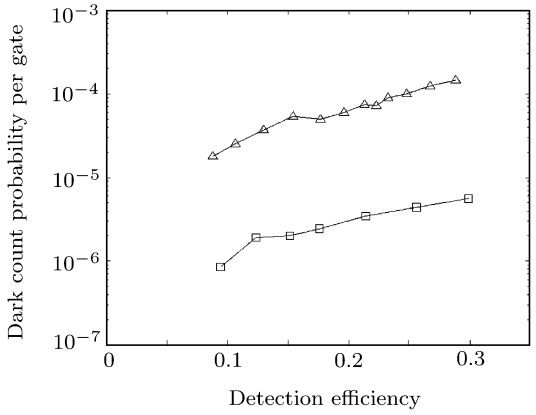


Fig.8. Dark count probability per gate versus detection efficiency for the IGSPD: (△) and (□) at $V_{\rm E}$=1.3 V and 0.9 V, respectively.

6. Summary and conclusion

In conclusion, we have calculated the output signal voltage and the bias voltage of the IGSPD. The qualification of transient spikes cancellation has been achieved and the accordant performance results have been presented by simulating with OrCAD 9.2. This proposal enables one to eliminate transient spikes, thus decrease bias voltage which reduces the dark count probability and the afterpulse probability without sacrificing detection efficiency. The paper would be helpful for designing and optimizing SPDs.

References

[1] Bennett C H and Brassard G 1984 *Proc. Int. Conf. Computer Systems and Signal Processing* (Bangalore, India) p175

[2] Deng F G, Li X H, Li C Y, Zhou P and Zhou H Y 2007 *Chin. Phys.* **16** 3553

[3] Stucki D, Ribordy G, Stefanov A, Zbinden H, Rarity J and Wall T 2001 *J. Modern Opt.* **48** 1967

[4] John G Rarity, Thomas E Wall and Kevin D Ridley 2000 *Appl. Opt.* **39** 6746

[5] Cova S, Ghioni M and Lacaita A 1996 *Appl. Opt.* **35** 1956

[6] Levine B F and Bethea C G 1984 *Appl. Phys. Lett.* **44** 553

[7] Ivan Prochazka 2001 *Appl. Opt.* **40** 6012

[8] McIntyre R J 1972 *IEEE Trans. Electron Devices* **19** 703

[9] Bethune D S and Risk W P 2004 *IEEE J. Quantum Electron.* **36** 340

[10] Bethune D S, Risk W P and Pabst P G 2004 *J. Modern Opt.* **51** 1359

[11] Tomita A and Nakamura K 2002 *Opt. Lett.* **27** 1827

[12] Zhou C Y, Wu G and Zeng H P 2006 *Appl. Opt.* **45** 1773

[13] Yoshizawa A, Kaji R and Tsuchida H 2004 *Appl. Phys. Lett.* **84** 3606

[14] Wei Z J, Zhou P and Wang J D 2007 *J. Phys.* D: *Appl. Phys.* **40** 6922