Vol 17 No 10, October 2008
1674-1056/2008/17(10)/3565-09

Chinese Physics B

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Planar ion chip design for scalable quantum information processing*

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(Received 27 February 2008; revised manuscript received 24 March 2008)

We investigate a planar ion chip design with a two-dimensional array of linear ion traps for scalable quantum information processing. Qubits are formed from the internal electronic states of trapped $^{40}Ca^{+}$ ions. The segmented electrodes reside in a single plane on a substrate and a grounded metal plate separately, a combination of appropriate rf and DC potentials is applied to them for stable ion confinement. Every two adjacent electrodes can generate a linear ion trap in and between the electrodes above the chip at a distance dependent on the geometrical scale and other considerations. The potential distributions are calculated by using a static electric field qualitatively. This architecture provides a conceptually simple avenue to achieving the microfabrication and large-scale quantum computation based on the arrays of trapped ions.

Keywords: ion traps, ion chip, quantum information processing
PACC: 0367, 4250

1. Introduction

Recently, the quantum computing community has demonstrated the basic building blocks of scalable ion trap quantum computers.[1−4] Ion trap quantum computing, as originally proposed by Cirac and Zoller,[1] is by now one of the most promising candidates for quantum information processing, where qubits are formed from the electronic states of single trapped ions and coupled through the Coulomb interaction. All the elementary requirements for quantum computation,[5] including efficient quantum state preparation,[6−8] manipulation[8−12] and readout,[8,13,14] have been demonstrated in this system. Ions confined in a linear rf Paul trap are cooled and form a stable spatial array whose motion is described by using normal modes. The spacing between ions is typically large enough so that the direct coupling of internal states of ions is negligible, thereby precluding logic states based on internal state interactions. The ion trap scheme satisfies the main requirements for a quantum computer. Most of these requirements subsequently have been demonstrated experimentally.

Current ion trap research is largely pursued in the quest of building operational useful large-scale ion trap schemes. Many experiments are recently carried out at Aarhus, Innsbruck, Michigan, MIT, NIST, and so on. Recent experiments have accomplished state readout,[13] one- and two-qubit gates,[11,15] and ion shuttling in straight lines and through T-junction.[16,17] There has also been made much progress in the deformation of conventional linear traps to scale the ion trap geometry beyond a few qubits and implement operational arrays of ion traps.[18−23] Some possible architectures work at holding and shuttling selected ion qubits in separate trapping regions.[2,17,24,25] However, most of these schemes are multilayered, which are difficult to construct and extend to more complicated layouts. Meanwhile, several planar ion trap geometries are brought forward due to their relatively easy design and fabrication.[26−28] but current planar architectures can generate only linearly trapped ions above the surface with several flat electrodes. Little achievement has been made on arrays of ion traps based on the planar geometries for scalable quantum information processing. Here we propose a novel approach to planar ion chip which can generate a linear trap only with two parallel segmented electrodes on a dielectric substrate and a thin grounded metal plate. Moreover, it could

*Project supported by the Shanghai Pujiang Programme and the National Basic Research Programme of China (Grant No 2006CB921202).
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be extended to an array of linear ion traps between adjacent electrodes above the plane easily by increasing the number of electrodes. The potentials applied to all of the electrodes are the same rf potential $V_0 \cos(\Omega t)$ for radial confinement. The short end segments are biased at a DC voltage U_0 for axial confinement and ion motion. Because of its straightforward design, any current microfabrication technique is applicable, such as photolithography and metal deposition or electro plating.

Various ions satisfy the requirements for the qubits of an ion trap quantum computer (Ca^+, Sr^+, Ba^+, Yb^+, Be^+, Mg^+, Hg^+, Cd^+), of these ions, $^{40}Ca^+$ offers the advantage of transitions that can be accessed with titanium-sapphire or diode lasers and a reasonably long-lived metastable state. We use $^{40}Ca^+$ ions here. In this paper, we report on a novel planar ion chip design for scalable quantum information processing. The ion chip that we describe in detail, is designed especially for storing two-dimensional trapped ions with the aim of using them as a scalable quantum processor. This architecture may provide a conceptually simple avenue to achieve the microfabrication and large-scale quantum computation based on the arrays of trapped ions.

2. Model description

2.1. Basic model

A conventional design for a linear rf Paul trap[29] consists of four parallel linear electrodes: each is equidistant from the trap axis and from its two nearest neighbours. The classical motion of a charged particle in such a trap can be determined by solving the Mathieu equations associated with the equations of motion of the particle in an applied potential.[30,31] Recent implementations of this four-rod design have involved, for example, macroscopic rods in a quadrupole formation[32,33] and a quadrupole formed by the inside edges of slots cut into pairs of alumina wafers[16] as well as other designs.[34−39] All of these devices involve the macroscopic machining of some sorts. Such traps function well, but they do not appear to offer a path toward the smaller, more complicated devices that will be necessary for large scale quantum information processing (QIP) with trapped ions. A straightforward approach to incorporate microfabrication into trap construction is to use multi-layer processing to reproduce the quadrupole geometry on a smaller scale. A first significant simplification in fabrication is the surface-electrode ion traps and the trapped ions all reside above a single surface.[26] But most of these geometries only generate one string of ions with four or five electrodes, and it seems difficult to scale up to large scale ion trap arrays. Though these different realizations of ion traps appear dissimilar, the basic physics of the trapping potential remains the same.

The planar ion chip we propose in this paper is a scalable geometry and the generated array of ion traps could be used for large scale quantum information processing. Its basic schematic diagram is shown in Fig.1. Two parallel three-segment gold electrodes

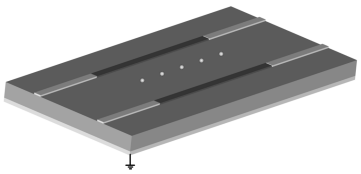


Fig.1. A three-dimensional drawing of the two-electrode planar ion chip. Two three-segment thin flat electrodes are on an insulating substrate (silicon dioxide) and a grounded metal plate. A string of trapped ions would lie between the electrodes and above the chip as shown here.

reside on the silicon dioxide substrate and a grounded gold plate separately, which is similar to early designs in Ref.[40] for guiding molecules and in Ref.[41]. The potentials applied to the electrodes are the same rf potential $V_0 \cos(\Omega t)$ for radial confinement, and the four end segments are biased at a DC voltage U_0 for axial confinement and ion motion. The segments of each electrode are capacitively coupled so that each one can be biased at a different static potential but remain at the same rf potential. The grounded gold plate is used as a mirror plate to generate mirror electrodes symmetrical to the above ones and carry corresponding opposite voltages, separately. This distribution is somewhat like that of conventional linear rf traps which have four parallel electrodes, whereas the advantage is that it makes the trap above the plane because of different potential arrangement, thereby facilitating easier fabrication and control. We choose a low rf-loss material silicon dioxide as a substrate and gold as an electrode material. The electrode's width w is 20 μm, its thickness t is 2 μm, the interelectrode distance $2a$ is 120 μm, the substrate's height h is 10 μm, the gold plate's thickness is 2 μm. The cross section and top view are shown in Fig.2. The peak amplitude of the rf potential V_0 is 300 V at a drive frequency $\Omega/2\pi = 15$ MHz. The DC voltage U_0 is about a few

volts. Since all of the trap electrodes reside on a single plane and the ions are trapped above this surface, a simplification in fabrication is achieved, and any typical chip fabrication method such as photolithography and metal deposition or electro plating is applicable. We have designed and made an atom chip by using photolithography method and succeeded in trapping atoms on the chip.[42] Thus we have the ability to fabricate this basic structure, and the fabrication process will not be discussed in detail here.

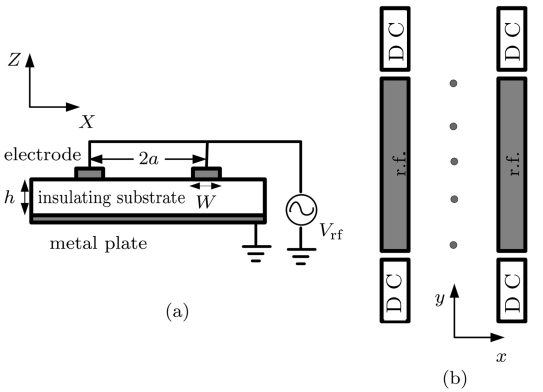


Fig.2. The cross section and top view of the two-electrode geometry. Both of the electrodes are driven by an rf potential for radial confinement, while the four end segments are biased at a positive static voltage for axial confinement.

2.2. Potential analysis

Generally, the pseudopotential in a linear ion trap is cylindrically symmetric near the centre of the trapping region, the motion of an ion in the pseudopotential can be approximated by using a ponderomotive potential[43]

$$\psi = \frac{e^2}{4m\Omega^2}|\nabla V(\boldsymbol{r})|^2 = \frac{e^2}{4m\Omega^2}\langle \boldsymbol{E}^2(\boldsymbol{r})\rangle. \qquad (1)$$

Ion motion in the pseudopotential can be approximated as a secular harmonic motion[2] with frequency

$$\omega_p^2 = \frac{e^2}{4m^2\Omega^2}\frac{\partial^2}{\partial x^2}(|\nabla V(\boldsymbol{r})|^2). \qquad (2)$$

The micromotion due to the time dependence of the rf potential is small in the limit where $2\sqrt{2}\omega_p/\Omega \ll 1$.[43] From Eq.(2) it is clear that the secular ion motion is dependent only on the gradient of $V(\boldsymbol{r})$, thus it is possible to calculate the effective (or ponderomotive) potential of the linear microtrap by using an electrostatic analysis. Moreover, since the rf potential is approximately uniform along the trapping axis near the centre of the trap, it can be described in the lateral plane i.e. in $x-y$ plane, reducing the calculation of the rf potential to the two-dimensional case. The distribution of lateral electric field of the basic model is calculated in Fig.3 by using the finite element analysis method (FEAM), there is a minimum point above and between the two parallel electrodes. It indicates the pseudopotential distribution of the trap and the trapping region is in this minimum axis along the electrodes. Similar to most of the surface-electrode ion traps, the trap well depth is relatively shallow because the potential distribution is asymmetric along the z axis. Since we only concern the region near the trapping centre, it can be assumed that in the central region the distribution is symmetric which is similar to that of the typical linear rf Paul trap.

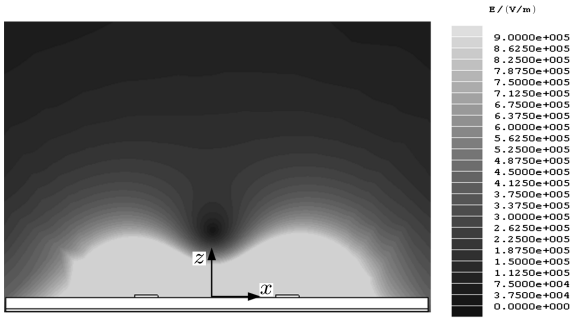


Fig.3. Radial contours of the electric field simulated through FEAM for the planar ion chip. Colours from black to white indicate low to high fields, respectively, showing that there exists a minimum place above and between the electrodes.

The potential benefit of the design is that the location and strength of the trapping region may be altered by varying the electrode structure in one dimension (the lateral direction or longitudinal direction) only. Through overall scaling of the electrodes's size and spacing, the distance of the trap axis from the chip can be controlled, effectively creating a trapping region for any desired surface-ion separation distance. Next, the relationship between the trap and its scale will be investigated theoretically. Moreover, since the rf potential is approximately uniform along the z-axis near the centre of the trap, it can be described in the $y = 0$ plane as a function only of x and z, thereby reducing the calculation of the rf potential to the two-dimensional case. The electrodes are assumed to be thin enough as charged wires. Figure 4 shows its cross section in the lateral plane, the coordinates of two top electrodes and their corresponding mirror electrodes are $O_1(x_1, y_1)$, $O_2(x_2, y_1)$, $O_3(x_2, y_2)$, and $O_4(x_1, y_2)$, respectively. Therefore $x_1 = a$, $x_2 = -a$, $y_1 = 0$, and

$y_2 = -2h$. According to the Gauss theorem and image

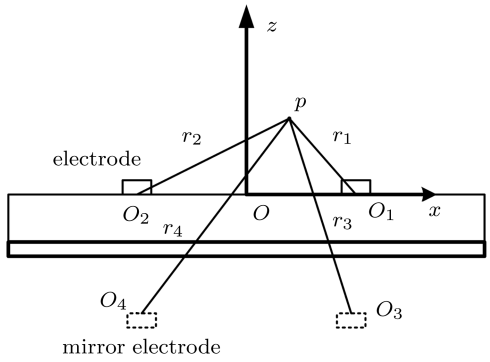


Fig.4. Schematic diagram of the planar ion chip design showing its cross section and the mirror electrodes.

method, we can derive the electric field distribution at an arbitrary point $P(x, y)$ as follows:

$$\boldsymbol{E}(x,y) = \frac{\lambda}{\pi(\varepsilon+\varepsilon_0)}\left(\frac{\hat{r_1}}{r_1} + \frac{\hat{r_2}}{r_2} - \frac{\hat{r_3}}{r_3} - \frac{\hat{r_4}}{r_4}\right), \quad (3)$$

where

$$\begin{aligned} r_1 &= \sqrt{(x-x_1)^2+(y-y_1)^2}, \\ r_2 &= \sqrt{(x-x_2)^2+(y-y_1)^2}, \\ r_3 &= \sqrt{(x-x_2)^2+(y-y_2)^2}, \end{aligned}$$

and

$$r_4 = \sqrt{(x-x_1)^2+(y-y_2)^2}, \quad (4)$$

which r_1, r_2, r_3 and r_4 are the distances from each wire to the point p, respectively; $\hat{r_1}, \hat{r_2}, \hat{r_3}$ and $\hat{r_4}$ are the corresponding unit vectors; λ is the electric line density of the charged wire; ε and ε_0 are the permittivity of vacuum and the dielectric constant of the substrate, respectively.

Then

$$|\boldsymbol{E}(x,y)| = \sqrt{E_x^2 + E_y^2}, \quad (5)$$

where

$$\begin{aligned} E_x &= \frac{\lambda}{\pi(\varepsilon+\varepsilon_0)} \\ &\times \left(\frac{x-x_1}{r_1^2} + \frac{x-x_2}{r_2^2} - \frac{x-x_2}{r_3^2} - \frac{x-x_1}{r_4^2}\right), \quad (6) \end{aligned}$$

and

$$\begin{aligned} E_y &= \frac{\lambda}{\pi(\varepsilon+\varepsilon_0)} \\ &\times \left(\frac{y-y_1}{r_1^2} + \frac{y-y_1}{r_2^2} - \frac{y-y_2}{r_3^2} - \frac{y-y_2}{r_4^2}\right). \quad (7) \end{aligned}$$

The coordinate of the minimum electric field $\boldsymbol{E}_0(0, y_0)$ is $x = 0$ and $y_0 = 231\,\mu$m in this dimension. Then let $x = 0$ and $|\boldsymbol{E}| = 0$, the zero field position is derived from Eq.(5)

$$y_0 = -h + \sqrt{h^2 + a^2}. \quad (8)$$

According to expression 8, the dependences of minimum electric field on the geometric parameters are shown in Fig.5. Figure 5(a) shows the variation of y_0 with distance h at a fixed value of a. It is clear that y_0 is a descending function of h. When $a = 60\,\mu$m and h increases from 5 to $90\,\mu$m, the position of y_0 decreases from 55.2 to $18.2\,\mu$m. Figure 5(b) shows that when h is constant, the value of y_0 increases almost linearly with half the distance between the electrodes, i.e. a.

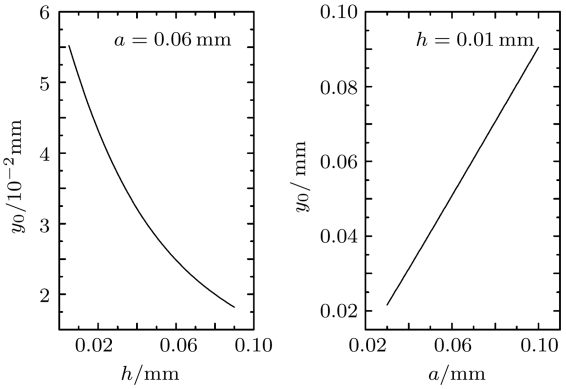


Fig.5. The relationships between the zero field position y_0 with and, separately, (a) the substrate's height h from 5 to $90\,\mu$m at $a = 60\,\mu$m and (b) the half distance a from 30 to $100\,\mu$m at $h = 10\,\mu$m.

For example, when $h = 10\,\mu$m and a increases from 30 to $100\,\mu$m, y_0 increases from 21.6 to $90.5\,\mu$m. In the calculation, the gold metal plate is set to be grounded, then a voltage U_g is applied to it to see its effect on the place of the trap axis and the trap well. Figure 6 shows the electric fields in the z axis from 0 to 0.1 mm which are calculated at voltage from -100 V to 100 V, indicting that the axis's positions are almost unchanged whereas the trap wells become deeper with the decrease of the voltages applied to the gold plate. So the zero voltage is quite appropriate for our system. Then we could draw a conclusion that an advantage of the configuration is the location and the strength of the trapping region, which can be altered easily by varying the scale of the trap. Through overall scaling of the electrode's size and spacing, the distances from the trapping axis, separately, to the electrodes and the substrate may be controlled and changed continuously along the length by shifting a distance a or h.

The number of dimensions can be much smaller than most of current designs with an appropriate proportion of the chip's size, and the trapped ions could be located much closer to the surface than that in current and previous planar ion traps.

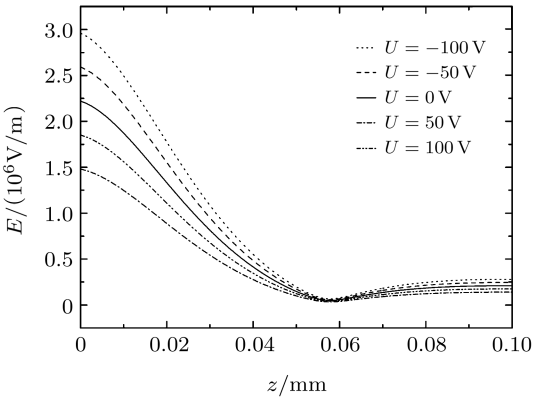


Fig.6. The electric field in the z-axis direction, with the applied voltage varying from $-100\,\mathrm{V}$ to $100\,\mathrm{V}$. The axis's positions are almost unchanged whereas the trap wells become deeper with the decrease of the applied voltage.

2.3. Two-dimensional ion chip geometry

As described above, just two-parallel electrode geometry can generate a linear ion trap above the plane. Furthermore, when the number of the electrodes increases, a two-dimensional array of linear ion traps will be created above the chip just as shown in Fig.8. There are produced six electrodes and five ion traps. That is quite an amazing progress of planar ion traps for the development of large scale QIP because current surface geometries are still staying on the one-dimensional scale. All of the geometrical scales and materials are the same as those for the two-electrode configuration except that half the distance of the adjacent electrodes decreases to $20\,\mu\mathrm{m}$. The potentials applied to all of the electrodes are the same rf potential, whose amplitude V_0 is $300\,\mathrm{V}$. Each electrode is segmented into two unequal lengths and the short end parts are biased at a static voltage U_0 of a few volts. The radial potential distribution is calculated in Fig.8, where it is easily seen that there are five parallel linear ion traps lying on the chip, so a two-dimensional ion chip is achieved. From Fig.8 one can see that the central three trap wells are almost the same and symmetric along the x axis, while the side two traps are a little different from them. Thus a promising conclusion can be reached that when the number of the electrodes increases to n, $(n-1)$ linear traps will be

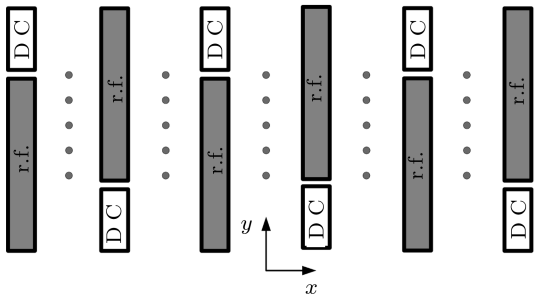


Fig.7. The top view of the six-electrode geometry. The potentials applied to all of the two-segment electrodes are the same rf potentials for radial confinement and the short end segments are biased at the same DC potentials for axial confinement. An array of trapped ions is generated above and between adjacent electrodes.

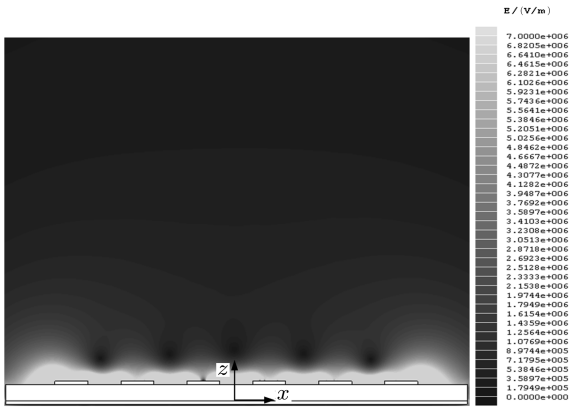


Fig.8. Radial contours of the electric field simulated through FEAM for the six-electrode geometry. Colours from black to white indicate low to high fields, respectively, showing that there exist five linear ion traps above and between adjacent electrodes.

formed in an array on the chip, the central $(n-5)$ traps will be symmetric and at the equal height, which can be used for many-qubit quantum logic gates. Therefore a two-dimensional ion chip is obtained and ions are stored in an array of linear traps. Ions in a single and among traps can be entangled by applying appropriate external laser fields to trapped $^{40}\mathrm{Ca}^{+}$ ions whose long-lived internal states carry the qubits. The feature of our scheme is that in the single linear traps, qubits are based on the exchange of phonons corresponding to the collective centre-of-mass (CM) motion of the ions. While among the traps, a laser controlled lead ion can move above the plane of the ions, approaching any particular ion, then the lead and the trapped target ions form a two-qubit gate, so the state of the target ion can be swapped for that of the lead ion. Furthermore, ions in each linear trap are interacted, thus through the head ion's motion, all of the ions among the array of traps can be entangled.

This is a desirable design for large-scale quantum information processor. In the future, traps with much smaller dimensions should have a shorter separation time, thereby minimizing heating. For manipulating a large number of ions, two-dimensional layouts with simpler methods of construction will be required. We expect traps to have dimensions smaller than those of previous traps and the heating problem to be solved as well.

3. Choice of ion and laser systems

Many species of ions are available for the qubits of an ion trap quantum computer. In this scheme each qubit consists of two internal levels of an ion trapped in a linear configuration. In order to perform the required logic gates, a third atomic state known as the auxiliary level is required. The quantum bus channel is realized by using the phonon modes of the ions' collective oscillations. These quantum systems may be manipulated by using precisely controlled laser pulses. Several kinds of ions and qubit schemes have been proposed. Among the ions used in current ion trap experiments, $^{40}Ca^{+}$ ions have the advantages of transitions that can be accessed by using titanium-sapphire or diode lasers and a reasonably long-lived metastable state. We use $^{40}Ca^{+}$ ions in the system. The relevant energy levels of $^{40}Ca^{+}$ ion are shown in Fig.9. The dipole-allowed transition from the $4^2S_{1/2}$ ground state to the $4^2P_{1/2}$ level with a wavelength of 397 nm is used for Doppler cooling and quantum jump readout; the 732 nm electric quadrupole transition from the $4^2S_{1/2}$ ground state to the $3^2D_{3/2}$ metastable level (lifetime ≈ 1.08 s) is suitable for sideband cooling. In the single laser computation scheme, the qubits and the auxiliary level can be chosen as the following electronic states:

$$|0\rangle = |4^2S_{1/2}, \quad M_j = 1/2\rangle, \tag{9}$$

$$|1\rangle = |3^2D_{5/2}, \quad M_j = 3/2\rangle, \tag{10}$$

$$|aux\rangle = |3^2S_{1/2}, \quad M_j = -1/2\rangle. \tag{11}$$

The ion can also be used for Raman type qubits, with the two Zeeman sublevels of the $4^2S_{1/2}$ ground state forming the two qubit states $|0\rangle$ and $|1\rangle$ separately, and with one of the sublevels of the $4^2P_{1/2}$ being the upper level $|2\rangle$. A magnetic field should split these two levels so that they can be resolved by the lasers. The pump and Stokes beams can be formed by splitting a 397 nm laser into two beams, and shifting the frequency of one beam with respect to that of the other beam by using an acousto-optic or electro-optic modulator. This arrangement has a great advantage in that any fluctuation in the phase of the original 397 nm laser will pass through both the pump and the Stokes beams, thereby being cancelled out. Radial contours of the electric field simulated through FEAM for the six-electrode geometry. Colours from black to white indicate low to high field, respectively. It shows that there are five linear ion traps above and between adjacent electrodes. The level $(4^2S_{1/2}, M_j = 1/2)$ is the ground state, while $(3^2D_{5/2}, M_j = 3/2)$ is a metastable level with a long lifetime of 1.06s. Both the electric dipole transition $4^2S_{1/2} \rightarrow 4^2P_{1/2}$ at a 397 nm wavelength and the electric quadrupole transition $4^2S_{1/2} \rightarrow 3^2D_{3/2}$ at 732 nm are suitable for Doppler cooling and sideband laser cooling, respectively. In Doppler cooling the laser radiation pressure slows down the axial motion of the ions until temperature T reaches a few mK. To further reduce the temperature ($T \approx$ a few μK) until no phonons are present, one can resort to the sideband cooling.

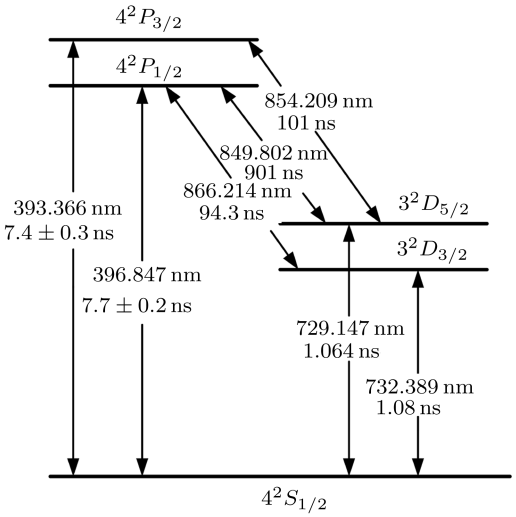


Fig.9. The lowest energy levels of $^{40}Ca^{+}$ ion, with transition wavelengths and lifetimes indicated.

$^{40}Ca^{+}$ ions can be easily produced by photoionization. The first stage is to cool a small number of ions down to their Doppler limit in the ion trap, which requires a beam at 397 nm to excite the $4^2S_{1/2}$–$4^2P_{1/2}$ resonant transition. In this procedure, a laser beam with a frequency slightly less than that of the resonant transition of an ion is used to reduce its kinetic energy. Owing to the Doppler shift of the photon frequency, ions preferentially absorb photons that oppose their motion, whereas they re-emit photons in all directions,

resulting in a net reduction in momentum along the direction of the laser beam. After carefully selecting the trap parameters, many cycles of absorption and re-emission will bring the system to the Lamb–Dicke regime, leaving the ions in a string-of-pearls geometry. In order to achieve the Doppler cooling of these ions, the required power and linewidth of the 397 nm laser are modest. The saturation intensity of $^{40}Ca^{+}$ ions is about $10\,mW/cm^2$, and the laser linewidth must be less than 10 MHz. During the Doppler cooling, the ions may decay from the $4^2P_{1/2}$ state to the $3^2D_{3/2}$ state, whose lifetime is about 1 s. To empty this metastable state, a second laser at 866 nm should be used. Once the string of ions is Doppler cooled to the Lamb–Dicke regime, the second optical cooling, sideband cooling, will be used to reduce the collective motion of ions to its lowest vibrational level.[44] The last stage is the transitions required for the realization of quantum logic gates and readout. These can be performed by using the lasers similar to those used in the Doppler and sideband cooling procedures. There are some other considerations concerning the laser systems for quantum computation which should be mentioned. To reduce the total complexity of the whole system, diode lasers and a frequency doubling cavity should be used to handle the Doppler cooling and quantum jump readout. Furthermore, complex quantum computations require the laser on the $4^2S_{1/2} - 3^2P_{5/2}$ computation transition to have a coherence time as long as the computation time.

4. Fabrication considerations

The novel planar ion chip geometry can be constructed just in a few microfabricated steps. We describe only the basic structure, which can be realized by means of patterned metal deposition onto an insulating substrate, photolithography or electron beam lithography that can be used to determine the electrodes. Such a method is similar to that used for neutral atom optics and atom guides on chips.[45−51] The dissipation of the trap can be modelled as a resistor representing the leads in series with the trap capacitance and its equivalent series resistance, which is proportional to the dielectric loss. In our design the proximity of insulating surfaces between the electrodes can hold charges and so perturb the trapping field in the vicinity of the ions. We set the spaces between the electrodes to be of bare insulator, therefore charges on these surfaces may be reduced. Trenches that undercut the electrode layer may be etched into the substrate to minimize the effect of charging. Therefore the electrode materials must be chosen to have a low rf loss, and the chip must contain some different metals. The evaporation, sputtering, and electroplating technologies also may be applied to a wide variety of materials. For Gold the relative cleanliness of its surface makes it a reasonable option as electrode material. Similarly, as for the choice of substrate material, the fabrication method requires its surface to be relatively smooth and reasonably adhesive to metallic films. Therefore we use silicon dioxide as the substrate material for its low rf loss and some ability to be etched. Other materials such as fused silica and quartz are also applicable. If the electroplating technique is used, aluminium nitride, sapphire, alumina, and diamond are optional materials. It is suggested that silicon carbide should be used as structural support for metallic electrodes. There still exist some experimental challenges to the realization of the scalable quantum computer. First, after the arrays of linear traps have been created and loaded with $^{40}Ca^{+}$ ions, decoherence must be avoided because the motional states of the ions can be entangled with the environment during the gate operation. Second, laser intensity fluctuation must be controlled to avoid dephasing and light scattering.

Further investigation should focus on how to implement an adequate set of logic gates. In order to realize any computation we need to both initialize the state of the computer and to read out the final state of the computation. Initialization is possible by using laser cooling techniques. It is possible to optically pump the ion to the state where all qubits are $|0\rangle$. Once the computation is finished, the readout, i.e. the state measurement, of the quantum register is possible by using the quantum jump technique previously discussed. Readout can play a role in error correction schemes likewise. Finally, note that measurements require a strong coupling of the quantum system to the environment, which is in strong contrast to the initially discussed isolation requirement. It follows that we need a means to switch on and off the interaction of any arbitrary qubit with the environment deliberately.

So the test of the scaling of the heating rates is much important, thus the requirements for laser cooling and constraints on ion motion must be determined. Charging of trap or structural components due to electrons from impact ionization may also lead to unpre-

dictable heating or ion-trapping behaviour. Ion motion in a single trap or among traps must be studied and slowed down to avoid non-trapping point by applying reasonable static voltages to the end electrode segments. Additionally, the ease of fabrication allows the rapid testing of new trap geometries and ion shuttling techniques. So we effectively create a trapping region for any desired surface ion separation distance.

5. Conclusions and discussion

We have proposed a novel planar ion chip design for scalable quantum information processing with a two-dimensional array of linear traps to perform quantum computations with trapped ions. In particular, such a two-dimensional array setup offers a realizable scheme for a scalable quantum computer. Despite being conceptually simple, the scheme is within the reach of current experimental technologies. The planar ion chip we proposed in this paper is of a scalable geometry with parallel segmented gold electrodes residing on the silicon dioxide substrate and a grounded gold plate separately. A combination of appropriate rf and DC potentials is applied to the electrodes for the stable radial confinement and axial confinement of trapped ions, respectively. And as the number of the electrodes increases, more linear ion traps will be generated efficiently to achieve more realizable physical architecture.

Furthermore, since the fabrication of such a geometry is straightforward and allows easy deformation in design and construction, typical microfabrication techniques can be used to fabricate basic chip structure without further difficulties in fabrication. The effective potential of the trap is calculated through an electrostatic analysis by FEAM qualitatively, which is able to answer the problem. The trapping depth can be controlled by changing the geometrical dimensions. The advantage of our design is that it can create an array of linear traps while current surface ion traps only generate a linear trap above the plane. Some limitations to this study are that the accurate values of the pseudopotential and the depth of trapping well are not obtained and the micromotion of trapped ions is not investigated in detail because it could be controlled by applying appropriate DC voltages to the end electrode segments. However, all of these limited problems are within the reach of current experimental technologies and could be solved in the oncoming experiment. Despite being conceptually simple, it is believed that this scheme is reasonable and will bring forward a new avenue to reaching a scalable quantum computer. Furthermore, we should stress that apart from its use for large-scale quantum computer, the scheme can also be used to build up scalable ion clocks. Future work will focus on experimental fabrication and the ions' micromotion in such a two-dimensional linear trap array. In a word, we have brought forward a novel and effective experimental scheme for large-scale quantum information processing and quantum computers.

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