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$Si_1Sb_2Te_3$ phase change material for chalcogenide random access memory*

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This paper investigated phase change $Si_1Sb_2Te_3$ material for application of chalcogenide random access memory. Current–voltage performance was conducted to determine threshold current of phase change from amorphous phase to polycrystalline phase. The film holds a threshold current about 0.155 mA, which is smaller than the value 0.31 mA of $Ge_2Sb_2Te_5$ film. Amorphous $Si_1Sb_2Te_3$ changes to face-centred-cubic structure at $\sim 180\,^{\circ}C$ and changes to hexagonal structure at $\sim 270\,^{\circ}C$. Annealing temperature dependent electric resistivity of $Si_1Sb_2Te_3$ film was studied by four-point probe method. Data retention of the films was characterized as well.

Keywords: phase change, chalcogenide random access memory, Si–Sb–Te
PACC: 8130H, 7360F

1. Introduction

Chalcogenide random access memory (C-RAM) is considered to be the most promising next-generation nonvolatile memory due to its advantages of long lifetime, high speed, low cost and high scalability.[1,2] It is based on electric current pulse which induced reversible phase change between amorphous state and polycrystalline state in chalcogenide phase change materials. In the past two decades, great efforts have been made on new phase change materials development. Various kinds of materials were proposed, such as In–Se[3], Se–Sb–Te,[4] Ag–In–Te,[5] Ag–In–Sb–Te,[6] $(Ge_1Sb_2Te_4)_{1-x}(Sn_1Bi_2Te_4)_x$,[7] In–Te,[8] Si–Te,[9] Ge–Te–Bi.[10] However, the more current candidate for C-RAM is the Ge–Sb–Te series, especially $Ge_2Sb_2Te_5$.[11−12] It is well known that $Ge_2Sb_2Te_5$ has already been commercially used in digital versatile discs.[13−14] Low programming current is one of the desired qualities in C-RAM research and development. To reduce programming current researchers not only have to enhance resistivity of the materials by doping,[15−19] and scale down the contact area,[20] but also have to determine new and better phase change materials more outstanding than $Ge_2Sb_2Te_5$.

According to Ref.[21], a sufficiently large electronic band-gap is required in order to reduce threshold current. The band-gap of Si (1.12 eV) is much wider than that of Ge (0.74 eV). For increasing band-gap width of the material, Si doping into the narrow-gap semiconductor Sb–Te will be much more helpful than Ge doping. Lankhorst *et al* reported that doped-SbTe materials, which have advantage of a shorter programming time are more suitable than standard GeSb-Te materials for line-concept memory operation.[22] However, no Si doping had been mentioned. In this work, SiSbTe material was prepared and investigated.

2. Experimental details

$Si_1Sb_2Te_3$ thin films (500 nm) were prepared by co-sputtering a silicon target and a Sb_2Te_3 alloy target on aluminium foil, SiO_2/Si and W/Si substrates. The background pressure and Ar pressure were 1×10^{-4} Pa and 0.21 Pa respectively. Structure of the films annealed in N_2 atmosphere at various temperatures

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was measured by employing x-ray diffraction (XRD). The diffraction patterns was taken in the 2θ range of 20–60 ° by using Cu/K-α radiation (λ = 1.54056 Å) with the scanning step of 0.02 °. Differential scanning calorimetry (DSC) measurement was performed by using $Si_1Sb_2Te_3$ powder scratched from glass substrates. Using film deposited on aluminium foil, we determine the composition of the film by energy dispersive spectroscopy (EDS, Oxford INCAEnergy quipped in Hitachi S4700). Current–voltage (I–V) test was carried out by employing a sandwiched structure shown in Fig.1. The contact size between top electrode and phase change material is about 10×10 μm^2.

Data retention assessment relies on the evaluation of the time-dependent resistance change of the amorphous phase change film under a constant temperature annealing. In order to avoid oxidation and evaporation in the measurement, phase change film was covered with 10 nm-thick SiO_2 layer.

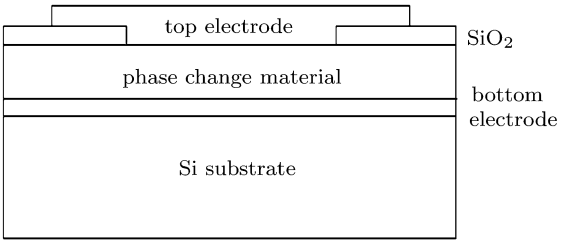


Fig.1. Cross-section of prototype device for $I-V$ measurement.

3. Results and discussion

The DSC curves of $Si_1Sb_2Te_3$ measured with various heating rates are shown in Fig.2. Two separate exothermal peaks are observed in each curve which suggests that the phase change of the material is a two-step process, this is similar to that of GeSbTe materials.[23–25] The two exothermal peaks correspond the crystallization temperatures respectively. The temperatures at the observed peaks are ∼180 and ∼270 °C when the heating rate is 10 °C/min. DSC curves of Sb_2Te_3, $Si_{0.25}Sb_2Te_3$ and $Si_{0.5}Sb_2Te_3$ at heating rate of 10 °C/min were also measured. The corresponding first crystallization temperatures for Sb_2Te_3, $Si_{0.25}Sb_2Te_3$ and $Si_{0.5}Sb_2Te_3$ are approximately 110, 148 and 166 °C respectively. Crystallization temperature increases with the increase of silicon concentration within the material. Obviously crystallization temperature of the $Si_xSb_2Te_3$ can be controlled by adjusting silicon concentration. It is well known that proper increase of crystallization temperature will be helpful in data retention, especially for C-RAM used in high temperature environments. The activation energy of $Si_1Sb_2Te_3$ for the crystallization from amorphous structure to polycrystalline face-centred-cubic (FCC) structure was derived via Kissinger's analysis of DSC curves.[26] The crystallization activation energy is about 1.51 eV, which is much smaller than that of $Ge_2Sb_2Te_5$.[12] This is due to the low concentration of silicon atom within the material. DSC result also suggests that the melting temperature of $Si_1Sb_2Te_3$ is about 606 °C, while those of Sb_2Te_3 and $Ge_2Sb_2Te_5$ are 550 and 618 °C respectively. An increase of 17 at.% of silicon in Sb_2Te_3 thin film results in an increase of crystallization temperature about 70 °C and an increase of melting temperature about 56 °C. Consequently, both crystallization and melting temperature can be controlled by adjusting silicon concentration within the $Si_xSb_2Te_3$ material. It is well known that crystallization temperature can also be controlled by O or N doping. However, no doping dose higher than 12 at.% has been reported.[19,27] On the other hand, $Si_xSb_2Te_3$ material will lose its phase change phenomenon only when silicon concentration exceeds 95 at.% according to our research.[28] Hence, the 'cut-off' point of phase change phenomenon at 95 at.% will make $Si_xSb_2Te_3$ films have a bigger range of tunability than O and N doping.

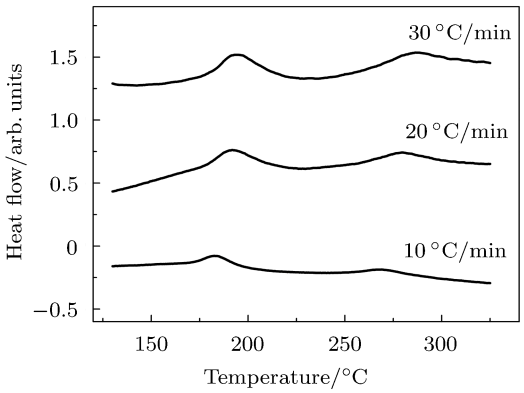


Fig.2. DSC curves of $Si_1Sb_2Te_3$ at different heating rate of 10, 20 and 30°C/min respectively.

XRD patterns for the $Si_1Sb_2Te_3$ films annealed at 200, 300 and 400 °C respectively are shown in Fig.3. In each case, the 500 nm-thick $Si_1Sb_2Te_3$ films were annealed for 30 minutes in N_2 atmosphere. The figure shows that the film crystallizes to FCC structure when annealed at 200 °C and to hexagonal structure when annealed at 300 and 400 °C, which is similar

to the two-step phase change process of $Ge_2Sb_2Te_5$. But the crystallization of the Sb_2Te_3 thin film occurs via a single-step phase change in which the film transits from amorphous structure to hexagonal rhomb-centred structure around 110 °C.

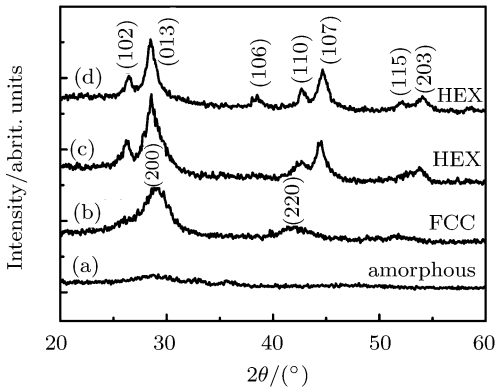


Fig.3. XRD patterns of $Si_1Sb_2Te_3$ thin film deposited on SiO_2/Si substrate which were annealed at various temperatures for 30 minutes: (a) as-deposited, (b) 200°C, (c) 300 °C and (d) 400 °C.

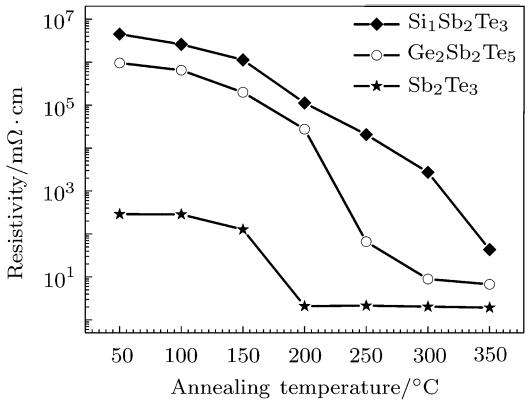


Fig.4. Electric resistivity as a function of annealing temperature for $Si_1Sb_2Te_3$, Sb_2Te_3 and $Ge_2Sb_2Te_5$ thin films.

The temperature dependent electric resistance of phase change material is an important parameter. Four-point probe method was performed to study the annealing temperature dependent resistivity of the $Si_1Sb_2Te_3$ thin film deposited on SiO_2/Si substrate. Resistivity decreases with the increase of annealing temperature, with quick drops at about 200 and 350 °C, as shown in Fig.4. The resistivity of $Si_1Sb_2Te_3$ film is about one order of magnitude higher than that of $Ge_2Sb_2Te_5$ film sputtered from $Ge_2Sb_2Te_5$ alloy. Furthermore, resistivity of $Si_xSb_2Te_3$ film increases with increase of silicon concentration. Proper improvement of the resistivity of phase change material may result in a low programming current in C-RAM operation. According to $P = I^2R$, higher resistivity leads to better heating efficiency. For this reason, researchers concentrate their efforts in increasing the resistivity of phase change film by doping with nitrogen and oxygen, etc.[15−19] For example, Horii *et al* have successfully reduced the programming current by nitrogen doping.[18]

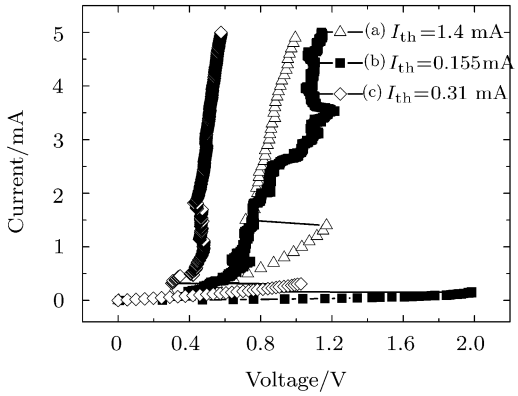


Fig.5. *I–V* curves for (a) $Si_1Sb_2Te_3$ and (b) $Ge_2Sb_2Te_5$ thin film inserted prototype devices. The phase change threshold currents are 0.155 and 0.31 mA respectively.

I–V measurement was conducted on prototype C-RAM devices (structure shown in Fig.1) containing 500 nm-thick amorphous $Si_1Sb_2Te_3$ or $Ge_2Sb_2Te_5$ inset material. Figure 5 shows that threshold current is about 0.155 mA and 0.31 mA for $Si_1Sb_2Te_3$ and $Ge_2Sb_2Te_5$ respectively. Since the contact size is 10×10 μm^2, I_{th} can be further reduced by decreasing the size. It should be emphasized that in this performance I_{th} of $Si_1Sb_2Te_3$ is even smaller than that of $Ge_2Sb_2Te_5$, which is widely adopted in C-RAM development. Three main reasons are proposed for this. (1) Silicon doping leads to wider electronic band-gap of the amorphous material. A sufficiently wide electronic band-gap is required in order to reduce threshold current.[21] (2) Resistivity of $Si_1Sb_2Te_3$ film is higher than that of $Ge_2Sb_2Te_5$, according to Fig.4. It is well known that higher resistivity of phase change film may lead to a lower threshold current. (3) $Si_1Sb_2Te_3$ film possesses a lower crystallization activation energy than that of $Ge_2Sb_2Te_5$. The low I_{th} of $Si_1Sb_2Te_3$ will make Si–Sb–Te series thin film an important candidate for the next-generation low programming current and high density C-RAM devices. However, the lower activation energy of the film may result in poor data retention, especially at high temperature environment. We expect the film to exhibit a good balance between programming current and data retention.

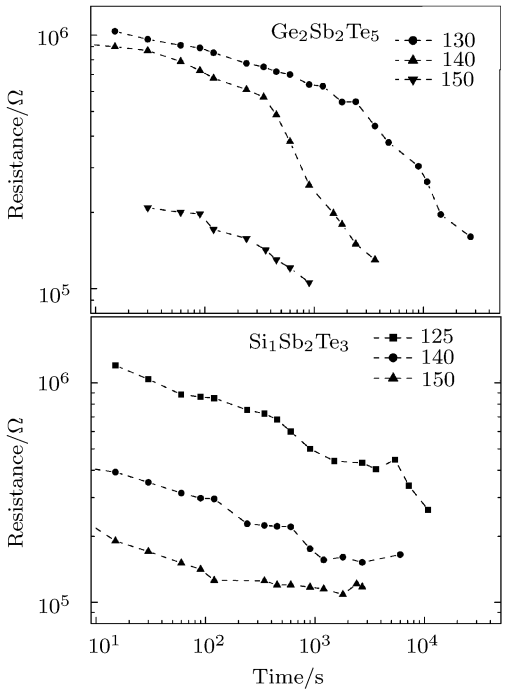


Fig.6. Resistance as a function of time at various temperatures for $Ge_2Sb_2Te_5$ and $Si_1Sb_2Te_3$ thin films.

Thermal stabilities of the amorphous $Si_1Sb_2Te_3$ and $Ge_2Sb_2Te_5$ films were studied by *in situ* resistance measurement at various annealing temperatures, in the range of 125–150 °C, as shown in Fig.6. According to the figure, $Ge_2Sb_2Te_5$ has a better thermal stability than $Si_1Sb_2Te_3$, which is mainly due to the higher activation energy. This result suggests that $Ge_2Sb_2Te_5$ is a better candidate for application in high temperature environment. One effective method to improve data retention is to increase silicon concentration of the $Si_xSb_2Te_3$ material. For example, data retention of $Si_2Sb_2Te_5$ is much better than that of $Ge_2Sb_2Te_5$.[28]

4. Conclusions

In conclusion, a phase change material with high resistivity and low phase change threshold current was prepared and investigated. The first and second crystallization temperatures of $Si_1Sb_2Te_3$ material are about 180 and 270 °C respectively. The crystallization activation energy is approximately 1.51 eV. The film shows an ideal electrical property, with an I_{th} of 0.155 mA, which is only half that of $Ge_2Sb_2Te_5$. However, due to plain data retention, $Si_1Sb_2Te_3$ thin film may be not suitable for applications in high temperature environment. However, it is still one of the promising candidates for the next-generation low energy cost and high density C-RAM devices. According to our investigation, both the crystallization temperature and the resistivity can be controlled by adjusting silicon concentration of $Si_xSb_2Te_3$.

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