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Actions of negative bias temperature instability (NBTI) and hot carriers in ultra-deep submicron p-channel metal–oxide–semiconductor field-effect transistors (PMOSFETs)*

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Hot carrier injection (HCI) at high temperatures and different values of gate bias V_g has been performed in order to study the actions of negative bias temperature instability (NBTI) and hot carriers. Hot-carrier-stress-induced damage at $V_g = V_d$, where V_d is the voltage of the transistor drain, increases as temperature rises, contrary to conventional hot carrier behaviour, which is identified as being related to the NBTI. A comparison between the actions of NBTI and hot carriers at low and high gate voltages shows that the damage behaviours are quite different: the low gate voltage stress results in an increase in transconductance, while the NBTI-dominated high gate voltage and high temperature stress causes a decrease in transconductance. It is concluded that this can be a major source of hot carrier damage at elevated temperatures and high gate voltage stressing of p-channel metal–oxide–semiconductor field-effect transistors (PMOSFETs). We demonstrate a novel mode of NBTI-enhanced hot carrier degradation in PMOSFETs. A novel method to decouple the actions of NBTI from that of hot carriers is also presented.

Keywords: ultra-deep submicron PMOSFETs, negative bias temperature instability (NBTI), hot carrier injection (HCI), positive fixed oxide charges

PACC: 7340Q, 7300, 7220J

1. Introduction

Of many reliability issues arising from the silicon complementary metal–oxide–semiconductor (CMOS) transistors and integrated circuits, the earliest identified one is the negative bias temperature instability (NBTI).[1−3] The phenomenon happens at high temperatures (usually above 100 °C) under the influence of high negative voltages applied to the gate of a p-channel transistor. The effect behaves as a shift toward more negative gate voltages in the threshold of the transistor, and a decrease in the subthreshold slope due to an increase in the number of positive fixed charges in the oxide, as well as an increase in interface states density.[4,5] Another problem of reliability is about the hot carrier injection (HCI), where the application of a high voltage to the drain of a transistor (with a gate voltage being above the threshold voltage V_{th}) causes a gradual change in the I–V characteristics.[6−10] Both interface states and oxide traps are created under the action of hot carrier (HC) stress in PMOSFETs.

While much is known about the effect of gate voltage stress on the device characteristics, little is known of the joint actions of NBTI and HCs.[11,12] This paper is devoted to the study of the importance of the NBTI under the HCI condition. Measurements of degradations are carried out under various stress biases, and the results show that NBTI stress enhances HC degradation (NBTI-induced HC degradation). The acceleration is explained in terms of the role that holes play in creating NBTI type damage. We also demonstrate the coupling effect and decoupling effects of NBTI and HCI in the present paper, respectively.

2. Experimental procedure

Stress measurements were performed on surface channel PMOSFETs of 0.25 μm long channel. A 5 nm

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thick gate oxide grew through a two-step oxidation process. PMOSFETs of 0.25 μm long channel were stressed in an oven at temperatures from 125 °C to 165 °C in two different sets of electric stress conditions as shown in Fig.1 and Fig.2, respectively. Devices were stressed in the NBTI stress condition of $V_g = V_{stress}$ and $V_s = V_d = V_{sub} = 0$ and in the HCI stress condition of $V_g = V_d = V_{stress}$ and $V_s = V_{sub} = 0$. The stress was interrupted at regular intervals and device parameters were measured.

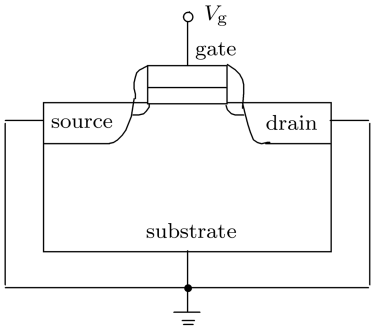


Fig.1. Configuration in NBTI-stress condition.

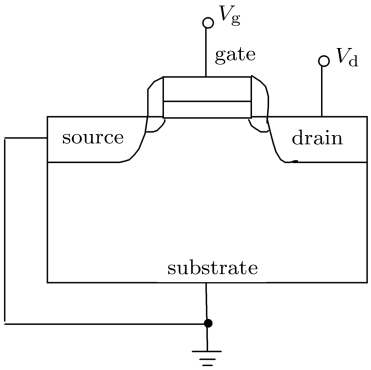


Fig.2. Configuration in HCI-stress condition.

3. Results and discussion

3.1. NBTI-stress

In analogy and mixed-signal applications, the reliability of threshold voltage (V_{th}) shift is a matter of utmost concern. Many high-precision analogy circuits such as data converters and comparators require the threshold voltages to be extremely stable over the course of the circuit lifetime. Higher V_{th} shift at or near operating electric field in PMOSFETs of advanced process technologies is becoming a major concern in industries.

Unlike HCI or time-dependent dielectric breakdown (TDDB) test, the estimation of V_{th} shift has no standard methods or specification limits for NBTI, though the characterization of the V_{th} shift in a wide range of stress condition is very important in understanding the reliability limits.

Experiments were performed on PMOSFETs with the channel length and width, respectively, being 5 μm and 0.25 μm and the oxide thickness being 5 nm. A set of devices was stressed for a fixed period of time 35000 s at different temperatures. The values of V_{th} were measured before and after stressing. The results of the fixed duration measurements are shown in Fig.3 as the V_{th} shift versus $1/kT$, giving an activation energy of 0.21 eV for the NBTI stress that is in agreement with that in the literature. However, for NBTI and HCI stresses, the activation energy is 0.17 eV. It suggests that the HCI stress enhances the NBTI degradation in PMOSFETs.

The V_{th} shifts are found to be negative, which corresponds to net positive charges build-up at the Si–SiO_2 interface, and it is also in agreement with what is indicated in the literature. This degradation arises from the trapped holes existing in the oxide, coupled with the creation of interface states.[13] Slow or relaxable states are also created.

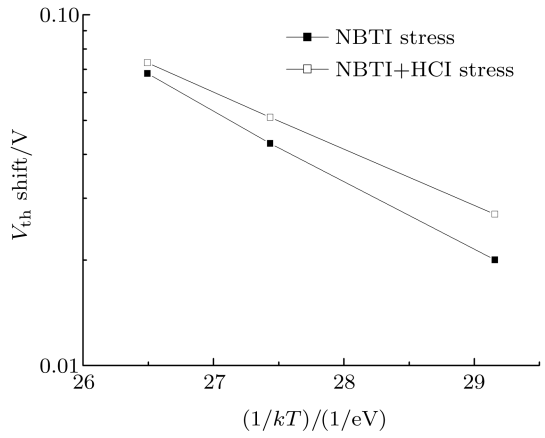


Fig.3. V_{th} shift as a function of $1/kT$ for NBTI stress ($V_d = 0$) and for NBTI coupled HCI stress ($V_d = V_g$).

3.2. HCI stress

It has been shown that the hot carrier degradation of PMOSFETs at low gate voltages and at room temperature is intimately related to the gate current, which can increase the transconductance (G_m). Line *a* in Fig.4 shows the transconductance change as a function of gate voltage for a device to be stressed at $V_d = -3.5$ V for 35000 s at 25 °C. It can be seen that the variation of transconductance is positive rather than negative for the device manufactured

by using this particular technology. Line b in Fig.4 shows the G_{mmax} shift versus V_{g} under the same voltage condition. At low gate voltages, the low- and high-temperature stresses appear similar. However, at high gate voltages, the high temperature stress results in a decrease in transconductance. It indicates that a different type of damage creation takes place, which can be either interface donor states or positive trapped charges, but not negative trapped charges, as this will lead to an increase in transconductance.

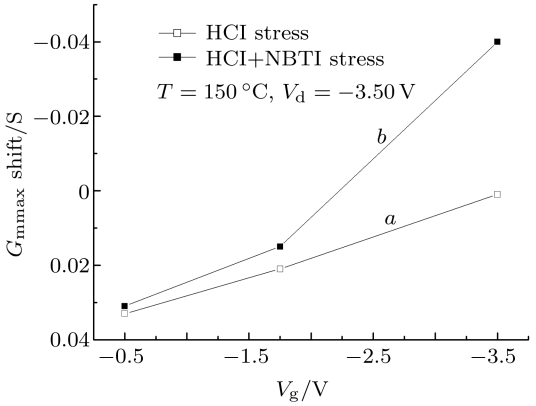


Fig.4. G_{mmax} shift as a function of V_{g} for HCI stress ($V_{\mathrm{d}} = -3.5\mathrm{V}$) and for HCI coupled NBTI stress ($T = 150\,^{\circ}\mathrm{C}$).

Figure 5 shows that the evolution of the damage with time at $T = 150^{\circ}\mathrm{C}$, $V_{\mathrm{d}} = -3.5\,\mathrm{V}$, and $V_{\mathrm{g}} = -0.5\,\mathrm{V}$, $-0.75\,\mathrm{V}$, $-3.5\,\mathrm{V}$ manifests the saturation effect that is normally found at the low-gate voltage hot-carrier stresses. Attention must be paid to

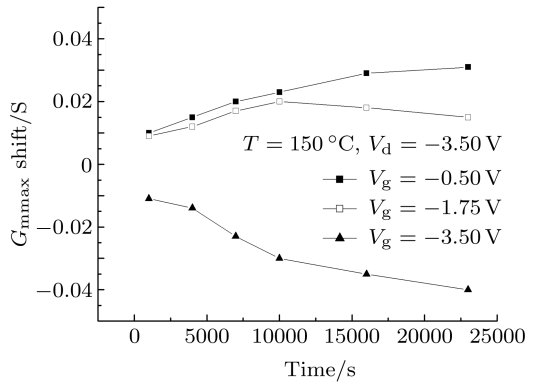


Fig.5. G_{mmax} shift as a function of time under the joint action of HCI coupled NBTI stress at different values of V_{g}.

the following phenomenon: the degradation for a short time results in an increase of the transconductance G_{m}, while the degradation for a longer time can result in a decreases of it. The initial increase of G_{m} is due to the channel-shortening effect discussed earlier, while the decrease of G_{m} arises from an NBTI compensating mechanism. The increase or decrease of G_{m} can degrade the transistor performances and further the transistor cannot work any more. At $V_{\mathrm{g}} = V_{\mathrm{d}}$, the transconductance degradation is purely associated with NBTI-like effects. Furthermore, while the low-temperature hot-carrier stress effects can restrict the changes in transconductance and drive current, the threshold voltage still changes in the case of these HCI stresses.

3.3. Damage identification

In order to understand the types of damage appearing at high gate voltages, the measurement of stress was performed as a function of gate bias, which was varied from 0 to $-3.0\,\mathrm{V}$. Figure 6 shows the change of G_{m} after a stress for 25000 s at $V_{\mathrm{d}} = -3.5\,\mathrm{V}$ and $T = 125\,^{\circ}\mathrm{C}$. It can be seen that the transconductance G_{m} and substrate current I_{sub} both reach their peaks at the same value of V_{g}, which indicates the variation in G_{m} is caused by the HCI.

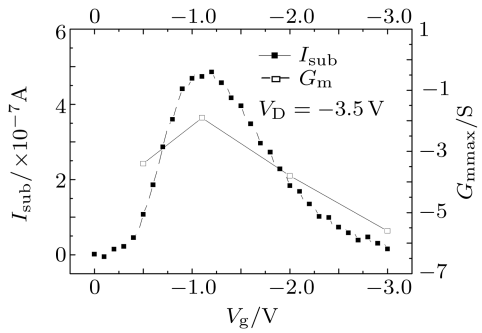


Fig.6. G_{mmax} shift and substrate current versus V_{g}.

Figure 7 shows the V_{th} shift as a function of the substrate current after a 25000 s stress under the same condition. This figure shows that the V_{th} increases with V_{g} increasing. For high voltages, more holes gain energy from the vertical electrical field and become hot carriers. These hot carries can break dangling bonds, generate oxide traps and positive fixed oxide charges, by which V_{th} is degraded greatly. Comparing G_{m} versus I_{sub} degradation with V_{th} versus $\mathrm{I_{sub}}$ degradation shows that they do not obey the same rule, which implies that the V_{th} versus G_{m} degradation is governed by a different mechanism.

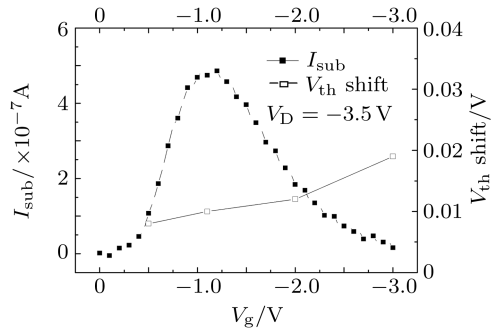


Fig.7. V_{th} shift and substrate current versus V_g.

The NBTI–stress–induced degradation is mainly determined by the positive fixed oxide charges located at Si–SiO_2 interface, which is governed by the vertical electrical field ($V_g - V_{sub}$). However, for the HCI stress, hot holes are the primary cause of damage, which is mainly controlled by the horizontal electric field. The joint action of HCI and NBTI stresses can make the MOSFET's lifetime prediction much more complicated.

Figure 8 shows the variation of V_{th} shift with channel length L for the cases of NBTI and HCI stresses. For the HCI stress, V_{th} shift significantly decreases with the increase of channel length. However, for the NBTI stress, V_{th} is almost the same for different channel lengths. Based on the above experimental phenomena, we can decouple the NBTI effect from the HCI effect. First, the values of V_{th} shift under the NBTI stress and HCI stress are measured for

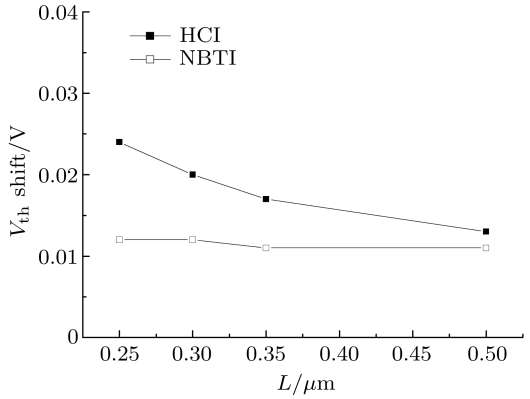


Fig.8. V_{th} shift versus channel length L for HCI and NBTI stresses.

a long channel and short channel respectively. Then, we subtract the value of V_{th} shift for a long channel from the values of V_{th} shift for a short channel, the difference between them is the HCI-induced damage for short channel PMOSFETs.

3.4. Degradation mechanism of HCI/NBTI

It is known that there are three different kinds of degradation mechanisms for HCI effect in ultra-deep submicron PMOSFETs at room temperature, i.e. electrons trapping, interface traps generation and positive charge formation in gate oxide under low-, medium- and high-gate bias conditions respectively. And the NBTI effect is mainly induced by the generation of donor-type interface traps and fixed charges. So the degradations of devices under $V_g = V_d$ at high temperatures are jointly influenced by HCI and NBTI effects.

According to the stress conditions and cause of degradation, damages induced by HCI mainly concentrate near the drain, while those coming from NBTI take place symmetrically near the source (S) and drain (D). The previous investigations suggested that degradations due to HCI were independent of the channel length, which is unapplicable to small size devices. In ultra-deep submicron PMOSFETs, the damage happens more severely in regions near S and D than in the channel. This is the reason why there exist more holes in the overlapped regions between gate and S/D than in the channel. Besides, in the processes of etching gate and ion injection, many initial oxide defects perhaps occur near the margins of gate. As devices are scaled down, the fraction of this difference increases correspondingly. Figure 9 shows that the area influenced by the NBTI stress is larger than that by the HCI stress.

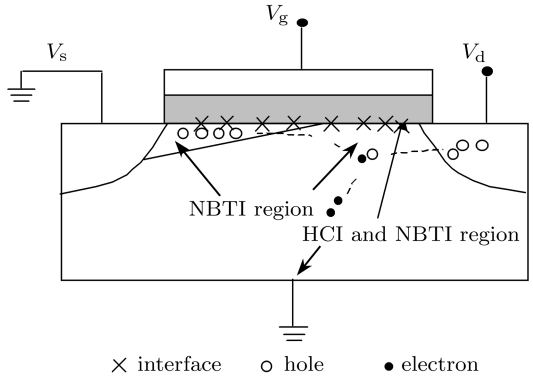


Fig.9. Illustration of degradation regions under the actions of NBTI and HCI stresses and their joint action.

In regions such as near the source and in the channel, degradations are mainly caused by the NBTI stress, while in the region near the drain the largest degradation is generated by the joint action of HCI and NBTI stresses.

4. Conclusion

NBTI and HCI effects have become significant reliability issues in ultra-deep submicron devices. The NBTI effect is mainly governed by a diffusion process, and it generates donor-type interface states and fixed oxide positive charges, thus resulting in significant $V_{\rm th}$ shift. In contrast, the HCI effect gives rise to different degradation phenomena at high temperatures and room temperature respectively. Its degradation at high temperatures is due to the generation of interface states and positive charges different from those in three kinds of stress regions where the degradation is produced at room temperature. On the other hand, at both high temperatures and room temperature, the largest degradation occurs at $V_{\rm g} = V_{\rm d}$. In static parameters, the NBTI and HCI stresses can jointly induce a larger $V_{\rm th}$ shift and require smaller activation energy than the NBTI stress alone. The damages near the drain result from the joint action of NBTI and HCI stresses, while the damages in the channel and near the source mainly originate from the NBTI stress. A novel method to decouple the action of NBTI from that of HCI is presented.

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