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Yield estimation of metallic layers in integrated circuits*

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In the existing models of estimating the yield and critical area, the defect outline is usually assumed to be circular, but the observed real defect outlines are irregular in shape. In this paper, estimation of the yield and critical area is made using the Monte Carlo technique and the relationship between the errors of yield estimated by circular defect and the rectangle degree of the defect is analysed. The rectangular model of a real defect is presented, and the yield model is provided correspondingly. The models take into account an outline similar to that of an original defect, the characteristics of two-dimensional distribution of defects, the feature of a layout routing, and the character of yield estimation. In order to make the models practicable, the critical area computations related to rectangular defect and regular (vertical or horizontal) routing are discussed. The critical areas associated with rectangular defect and non-regular routing are developed also, based on the mathematical morphology. The experimental results show that the new yield model may predict the yield caused by real defects more accurately than the circular model. It is significant that the yield is accurately estimated using the proposed model for IC metals.

Keywords: real defects, critical area model, mathematical morphology, yield estimation
PACC: 8116, 6630L, 8220W, 6780M

1. Introduction

Yield estimation can be used in production control, material management, timely product delivery, operations of planning tool, improving designs that have the yields much lower than anticipated, determining the cost of new devices and resource, therefore, it is a focal point in the industries ranging from standard products such as memories to the applications of specific integrated circuit (ASIC) and system on chip (SOC) products. Also, according to the results of yield estimation, some modifications to, such as, layout outlines, design rules and processes, can be made to obtain the maximum yields.[1,2]

Particles falling on wafers during processing is a dominant factor and always exists no matter how super-clean the environment is and how super-pure the chemical reagent used for the integrated circuit (IC) processing is. Any deformity in the form of extra material or the missing of some layer of the circuit resulting from contamination is called a defect. An estimation suggests that particles are responsible for 75% of the yield loss in volume-manufacturing of very large-scale integration integrated circuits (VLSI ICs).[3,4] The particle defect probability is generally found to increase sharply with the decrease of its size, which has a more serious effect on the design and manufacture of the components with their sizes decreasing increasingly. The particle defect always plays an important role in IC yields, and the design sensitivity to these physical particles is increasingly required to increase in nanometre technologies nowadays.[5,6] Among the typical complementary metal-oxide semiconductor (CMOS) processes, the particle defect is one of the serious loss factors resulting in the electrical faults. The real defect outline is usually modelled as being circular,[7−11] which can cause the errors of critical area estimations.[12−16]

In general, based on the circular defect outlines, the following Poisson yield model and the negative binomial model are often used to estimate the yield loss.

Poisson model

$$Y_{\mathrm{F}} = \prod_{i=1}^{M} \mathrm{e}^{-A_i^{(\mathrm{c})} D_i}, \tag{1}$$

negative binomial model

$$Y_{\mathrm{F}} = \prod_{i=1}^{M} \left(1 + \frac{D_i A_i^{(\mathrm{c})}}{\alpha_i}\right)^{-\alpha_i}, \tag{2}$$

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where Y_F denotes the yield of a chip, which is the product of all layer yields, D_i denotes the average number of defects per unit of area associated with the ith step of the manufacturing process. The Poisson yield is used to estimate the pessimistic yield for large devices. In the better negative binomial model, α_i is the clustering parameter. In both Poisson yield and negative binomial models, $A_i^{(c)}$ is the critical area related to a layout for layer i, and it can be written as

$$A_i^{(c)} = \int_{R_{min}}^{R_{max}} A(R)h(R)dR, \tag{3}$$

where $A(R)$ denotes the area in which the centre of a defect with diameter R must fall to cause the circuit failure, and $h(R)$ is the density function of defect size. R_{min} is the minimal diameter, and R_{max} the maximal diameter based on the circular model. It is always assumed that a defect is a round spot of either extra or missing conducting material with maximal diameter R. Defects in a layer are not the same in size, but have an exponential size distribution, which can be modelled as

$$h(R) = \begin{cases} CR^q/R_0^{q+1} & 0 \le R \le R_0, \quad q \ge 0, \\ CR_0^{p-1}/R^q, & R_0 \le R \le R_{max}, \quad p \ge 0, \\ 0, & R \ge R_{max}. \end{cases}$$

$$C = \begin{cases} \dfrac{(q+1)(p-1)}{(p+q)-(q-1)(R_0/R_{max})^{p-1}}, & p \ne 1, \\ \dfrac{q+1}{1+(q+1)\ln(R_{max}/R_0)}, & p = 1, \end{cases} \tag{4}$$

where p and q are real numbers (typically, $p = 3$, and $q = 1$), R_{max} is the maximal diameter and R_0 is the peak diameter of the probability density of defect size. Generally, the diameter of defect is presented from the following models:

1) Maximum or minimum circular defect model The diameter of a defect equals a maximal or minimal extension of the defect spot.

2) Circular model based on the mean extension of defect The defect is regarded as a round spot, and its diameter is taken as the diameter of mean extension of defect.

3) Circular model based on elliptical extension of defect The diameter of a defect is determined by the maximal extension of defect (d_{max}) or minimal extension of defect (d_{min}) as $1/2\sqrt{d_{max}d_{min}} + d_{min}d_{max}/(d_{min} + d_{max})$.

The circular model of real defect according to the above methods gives rise to the inaccurate estimation of IC yield. One reason for this is that it is difficult to determine the diameter of a defect accurately, and the other reason is due to a great variety of outlines of real defects existing. The present paper presents a rectangular model of real defects and places a special emphasis on the yield model study based on the rectangular defect outlines. Some experiments are performed to verify the proposed models.

The rest of this paper is organized as follows: Section 2 analyses the yield estimation error by the circular model; Section 3 describes the new yield model associated with the rectangular outline of a real defect; in Section 4 some experimental results are presented, and the conclusion is given in Section 5.

2. Error analysis of yield estimation for circular defect model

Because there may appear a variety of defect outlines for a given maximal diameter of a real circular defect, the defect outline cannot be determined uniquely. For example, Fig.1 shows seven defects having the same diameter for the maximal circular model, their remarkable differences in outline result in differences in yield estimation.

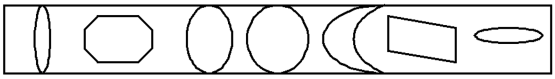


Fig.1. Different outlines with the same diameter.

To analyse the error caused by the circular model of a real defect, taking the feature of a layout routing into account (the vertical or horizontal routing), outlines with the same diameter of defect can be described by a rectangular degree T, which is defined as the ratio of width B_w to length B_h of the minimal rectangle enclosing the defect, and given by

$$T = B_h/B_w. \tag{5}$$

According to the value of T, the slender objects can be distinguished from roughly square or circular objects. For example, $T = 1$ corresponds to the maximal circular model; $T < 1$, to a slenderer defect in the horizontal direction; $T > 1$, to a slenderer defect in the vertical direction. The defect for $T > 1$ is not considered here in that the defect after a clockwise rotation through 90° has the same outline as that of the defect in the horizontal direction. Based on the 4×4 shift register layout, the variation in error of critical

area with rectangular degree T is simulated by Monte Carlo method as shown in Fig.2. Based on the distribution of defect sizes, 60 defects are sampled, so the defect density of a specific layout can be obtained.

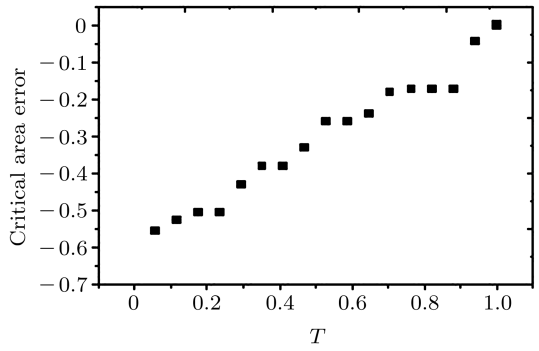


Fig.2. Critical area error versus rectangle degree T.

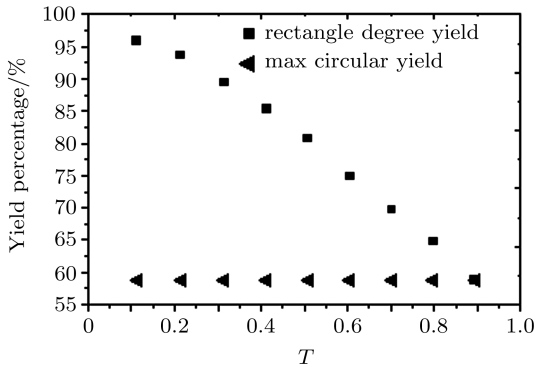


Fig.3. Yield percentage versus rectangle degree T.

Based on the maximal circular model, the critical area $A_i^{(c)}$ and the yield Y can be obtained. For the same defect density but different values of T, the different yields can be estimated from Fig.3. The dependence of maximal circular defect yield on rectangular degree T can be expressed by a higher-degree polynomial below as:

$$Y_{\mathrm{E}} = \sum_{i=0}^{N} P_i T^i, \tag{6}$$

where p_i is the coefficients of a polynomial, and T is an average rectangular degree of a defect. For Fig.3, we have

$$\begin{aligned} Y_{\mathrm{E}} = \; & -0.4576T^4 + 1.3929T^3 - 1.6354T^2 \\ & +0.4928T + 0.2077. \end{aligned} \tag{7}$$

Especially, if $T = 1$, then $Y_{\mathrm{E}} = 0$, which means that all the defects have circular outlines. If T is a minimum, the Y_{E} is a maximum, which means all the defects take the minimal circle outlines.

3. Yield model related to rectangular outline of real defect

3.1. New yield model

Based on the above analysis, the rectangular model of a real defect is given as follows. For a real defect, its maximum possible extension between two parallel straight lines, which correspond to the horizontal routing direction of the special layout and touch the defect, is termed the length (represented by the symbol H) of the real defect. The maximum possible extension of the real defect between two parallel straight lines, which correspond to the vertical routing direction of the special layout and touch the defect, is named the width (represented by the symbol B) of the real defect as shown in Fig.4. Thus we may model the real defect as a rectangle with length H and width B and call it the rectangular model.

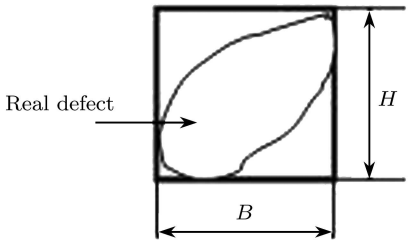


Fig.4. The rectangular model of a real defect.

Intuitively, the rectangular model of a real defect is more accurate for the metallic strips of a layout than the circular model of a real defect in the sense of yield estimation. Figure 5 shows the sampled defects: the defect in Fig.5(a) can cause a short fault but the defect in Fig.5(b) cannot. The maximal circles of those two defects are shown in Fig.6. If those two defects are replaced by their equivalent rectangles, they will lead to the circuit fault as effectively as those two real defects do. However, Figs.6(a) and (b) show the maximal defect outlines, where both circular outlines can cause the short fault, which is a consequence of an inaccurate maximal circular model.

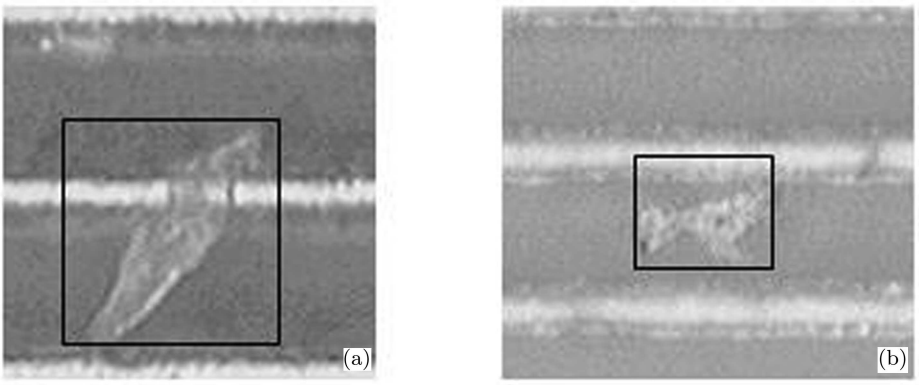


Fig.5. Real defect and its corresponding rectangular outline.

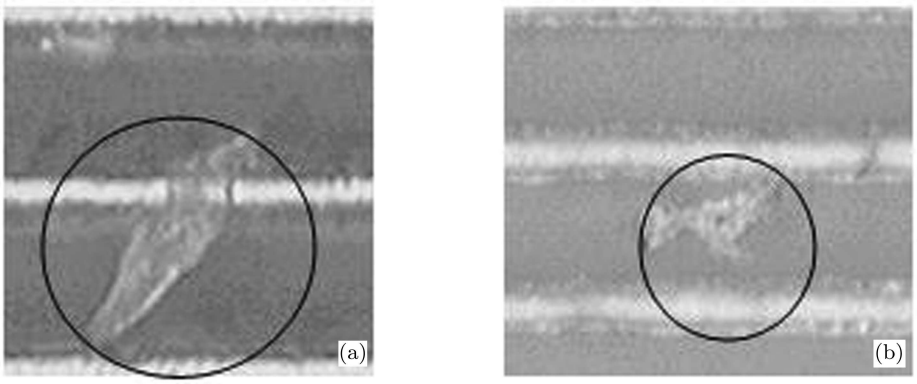


Fig.6. Real defect and its corresponding maximal circular outline.

Similarly, the minimal circular and the equivalent ellipse models also induce the error estimation of the circuit fault. The minimal circle of the defect in Fig.7 does not cause any faults, but the real defect causes a short fault (see Fig.5(a)).

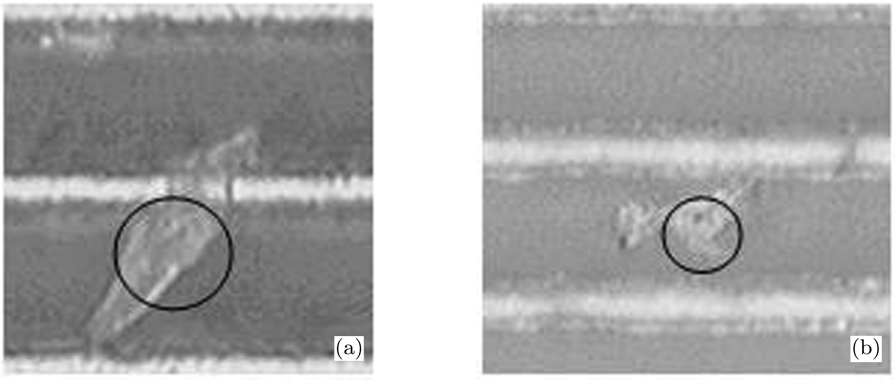


Fig.7. Real defect and its corresponding minimal circular model.

According to the rectangular defect outline model, the critical area Eq.(3), which is caused by a rectangular defect and a layout associated with the ith process, now can be rewritten as

$$A_i^{(\mathrm{c})} = \int_{H_{\min}}^{H_{\max}} \int_{B_{\min}}^{B_{\max}} A(H,B)h(H)b(B)\mathrm{d}H\mathrm{d}B, \quad (8)$$

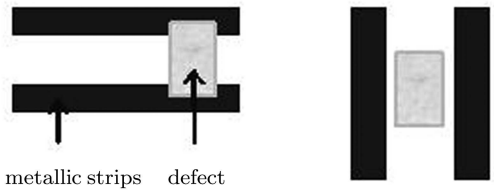
where $H_{\min}$ is the minimal length of the rectangular defect, and $R_{\max}$ the maximal length. $B_{\min}$ is the minimal width of the rectangular defect, and $B_{\max}$ the maximal width. $h(H)$ is the density function of length, and $b(B)$ is the density function of width. Using the relationship between the length H and width B of a defect, the critical area $A(H,B)$ can be con-

tained, which is clearly shown to be determined by the feature of layout routing and the used model of the defect.

For mature processes, the distributed functions $h(H)$ and $b(B)$ are fixed and cannot be changed. Therefore, the key to Eq.(8) is to find $A(H, B)$. The computation of critical area is related to the outlines of both the real defect and the layout. According to the feature of IC layout metals, their routings consist of regular (vertical or horizontal) and irregular routings. Generally, there are two kinds of defects that have a remarkable influence on the structure of a circuit for IC: the conductor extra defects and the conductor missing-defects. Accordingly, there are two kinds of critical areas that are short-circuit critical area and open-circuit critical area. We only discuss the short-circuit critical area computation here in this paper, due to the open-circuit critical area computation being similar to that of short-circuit's.

3.2. The computation of critical area for the regular routing of a layout and the rectangular defect

The short-circuit critical area is the area in which the centre of a defect must fall to cause two metallic strips to be completely linked with each other. Since the projection sizes in the horizontal or vertical direction of a rectangular defect are dissimilar, the fault probabilities caused by the rectangular defect in the two directions are also dissimilar. For instance, the rectangular defect in Fig.8(a) causes the horizontal conductor to be short-circuited but cannot cause the vertical conductor to be short-circuited in Fig.8(b).



(a) with short-circuiting (b) without short-circuiting

Fig.8. Fault caused by rectangular outline.

In the following section, the computations of a short-circuit critical area related to a regular routing for layout are performed in the following two cases.

Case 1 Two horizontally orientated metallic strips. Two metallic strips are assumed to be the same in length. The failures in this case are of short-circuits caused by extra defects each with a length of H and a width of B, and the model of critical area $A^{\rm hc}_{\rm short}(H, B)$ (see Fig.9) is described as

$$A^{\rm hc}_{\rm short}(H,B)=\begin{cases}0, & 0\le H\le P,\\ (H-P)L+(H-P)B, & P\le H\le W+2P,\\ (P+W)L, & H>W+2P,\end{cases} \tag{9}$$

where L and W are the length and width of metallic strip respectively, and P is the spacing between the two metallic strips.

Case 2 Two vertically orientated metallic strips. For the two vertical metallic strips, the critical region in which the centre of a defect with a length of H and a width of B must fall to cause the two metallic strips to be completely linked with each other, and the model of critical area $A^{\rm hc}_{\rm short}(H, B)$ is described as

$$A^{\rm vc}_{\rm short}(H,B)=\begin{cases}0, & 0\le B\le P,\\ (H-P)L+(B-P)H, & P<B\le W+2P,\\ (P+W)L, & H>W+2P,\end{cases} \tag{10}$$

where L and W are the length and width of metallic strip respectively, and P is the spacing between the two metallic strips.

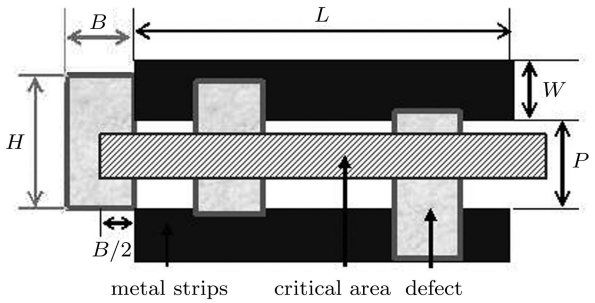


Fig.9. Short-circuit critical area by rectangular outline.

3.3. The computation of critical area for irregular routing and rectangular defect

For a layout, there are many conductors whose outlines each are similar to a rectangle. In the layout, because the outline consists of irregular rectangles, one must find a method to compute the critical area. Generally, since a layout can be converted into a fattened binary image, from which the critical area associated with the layout can be obtained.

Mathematical morphology has been developed.[17] It has several advantages over other techniques especially when applied to image processing, but no application to extracting the critical area. There are four foundational operations in morphology: dilation, erosion, opening and closing. The dilation operation of binary morphology is defined as follows:

$$\mathrm{DILATE}(S, E) = \cup \mathrm{TRAN}(E; i, j), (i, j) \in D_{\mathrm{S}}, \quad (11)$$

where D_{s} represents the S domain, which is the set of the known pixel positions of the image S. E is the structure element, which is converted by S. TRAN $(E; i, j)$ is defined as the operation in which the centre of E is moved to the position (i, j) of image S and then the image E is copied.

According to the definition, the critical area associated with rectangular extra defects and irregular layout routing is formed by a set of lines, and each line can be obtained in the following steps:

Step 1 Let the top side of a rectangular defect be parallel to the bottom side of layout N_1, the tangential point be T_1, and the centre of defect be located at point A (see Fig.10(a)).

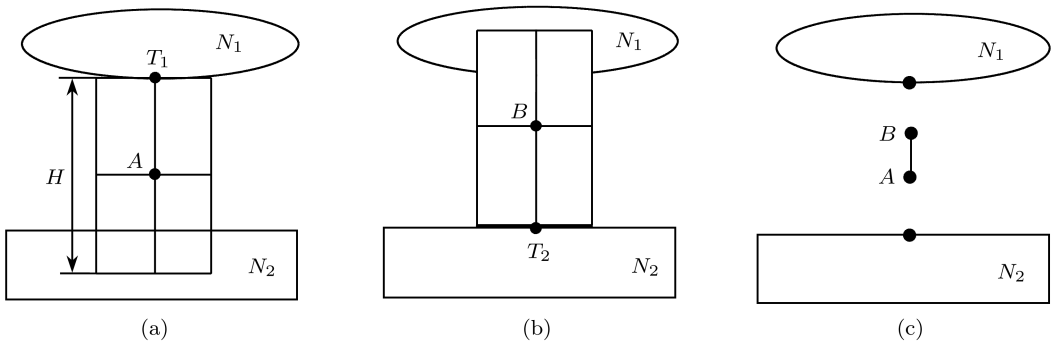


Fig.10. Computation method 1 of short-circuit critical area.

Step 2 Move the defect in the vertical direction, make the bottom side of rectangular defect parallel to the top side of layout N_2, and let the tangential point be located at T_2, and the centre of defect be at B (see Fig.10(b)). As a result, line AB belongs to the critical area (see Fig.10(c)).

Line AB can be derived in another approach as shown in Fig.11. It is clear that the length of line T_1A is $H/2$(see Fig.10(a)), the point A in Fig.10(a) is identical to the point C in Fig.11(a). That is to say, if the centre of the defect is located at the point T_1 of the N_1, the position A is just the point C that is the bottom side centre of the defect. Analogously, the point B in Fig.10(b) is identical to the point D in Fig.11(b). As a result, the line AB is identical to the line CD in Fig.11(c).

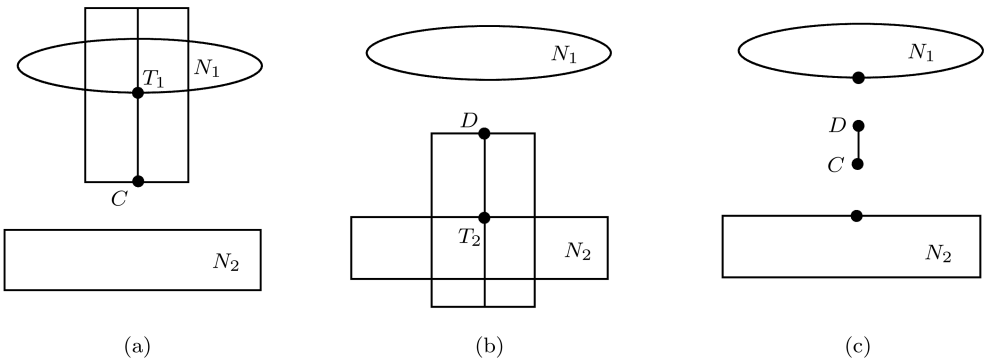


Fig.11. Computation method 2 of short-circuit critical area .

The key difficulty in mathematical morphology consists in selecting the structure element. Selecting the structure element is concerned with an original image and the computing aim. Generally, one can chose a quadrate structure element, a line structure element, or a diagonal element, and so on.

Based on the definition of mathematical dilation operation and the second method of the critical area computation, we suggest here a critical area computation method for short-circuit metallic strips.

Let $d(H,B)$ represent a structure element, N_1 and N_2 denote the outlines of metallic strips on a layout, then the critical area(see Fig.12) $AS(H,B,N_1,N_2)$ will be expressed as

$$AS(H,B,N_1,N_2) = ASD(H,B,N_1,N_2) - ASD(H,B,N_1,N_2) \cap N_1 - ASD(H,B,N_1,N_2) \cap N_2 \qquad (12)$$

with

$$ASD(H,B,N_1,N_2) = \mathrm{DILATE}(N_1, d(H,B)) \cap \mathrm{DILATE}(N_2, d(H,B)), \qquad (13)$$

where $\mathrm{DILATE}(N_1, d(H,B))$ denotes the dilating of metallic strip N_1 by defect $d(H,B)$; $\mathrm{DILATE}(N_2, d(H,B))$ represents the dilating of conductor N_2 by defect $d(H,B)$, and $ASD(H,B,N_1,N_2)$ is the intersection between $\mathrm{DILATE}(N_1, d(H,B))$ and $\mathrm{DILATE}(N_2, d(H,B))$. If the size of defect is small, $ASD(H,B,N_1,N_2)$ is zero, and the critical area is zero, which implies that the small size defect cannot cause short circuiting between conductors.

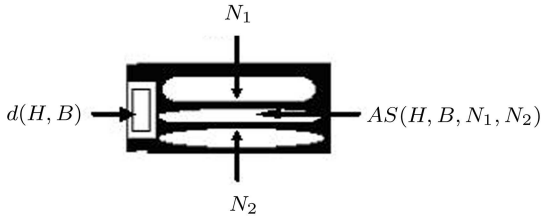


Fig.12. Critical area for a rectangular defect and irregular routing of a layout.

It is assumed that layouts are changed into multi-layer planar configurations which are CIF file format, where CIF stands for Caltech Intermediate Form. By using expressions (12) and (13), an extraction algorithm A can be designed based on the new model as follows.

Algorithm A:

Step 1. Decode the layout into many flat layers.

Step 2. Input the data of metallic layer i of a layout and the defect data.

Step 3. Convert the layout into binary images and label each of connected regions, and obtain the number of conductors c and their positions.

Step 4. Let $j = 1$, $h = j+1$,and structure element be denoted by $d(H,B)$.

Step 5. Dilate the metallic strip j by $d(H,B)$.

Step 6. Dilate the conductors $h, h/h \in (j+1, c)$ by $d(H,B)$. Using expressions (12) and (13), obtain the dilation results,that is the critical area of the metallic

strips j and h.

Step 7. $j = j + 1$, if $j < c$ go to Step 5, otherwise go to Step 8.

Step 8. Output the critical area.

With algorithm A, the number of metallic strips c is labelled according to their columns, and then the critical area of each pair of strips is extracted based on the short-circuit critical area model. The critical areas at different layers can be obtained by iterating the algorithm A.

4. Experimental results

The critical area extraction is carried out on a computer equipped with the Intel Celeron(TM) AT COMPATIBLE 1.2GHZ processor and 256MB RAM. Figure 13 shows the layout of a defect test chip used for our experiments.

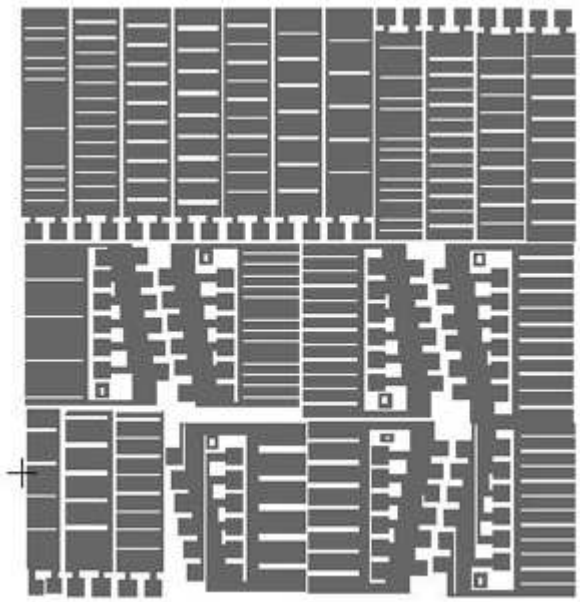


Fig.3. Layout of test chip.

The chip area is $2.63 \times 3.0\text{mm}^2$ and the minimal characteristic size is 0.7μm. The test chip consists of three different patterns and each of them includes eight parts of different sizes. For a 0.5μm manufacture process, two wafers filled with the test layout are used to collect real defect samples. More than 300 real defect samples are obtained with optical microscopes and scanning electron microscope (SEM). The rectangular outlines of these defects are derived by the segmentation method of processing colour images, which has been presented in the authors' previous paper.[18] Parameters H and B are extracted from these outlines, and then substituted into the proposed algorithm to calculate the critical area of the layout in Fig.13.

Tables 1–3 show the CPU time for the layout in Fig.13 with the values of defect $d : 20e$ and $15e$, where $e = 0.3095\mu$m. The first columns in Tables 1–3 indicate the critical areas of the nest layout, the comb layout and shake layout respectively, and the third columns in Tables 1–3 show the CPU time. From Tables 1–3, it can be seen that the CPU time to extract the critical area of the sub-layout is less than 1 min, so the proposed algorithm is practical.

Table 1. Critical area extraction and CPU time for nest structure layout.

parameter / layout	critical area /(10^{-3}cm^2/defect)	CPU time/s
Nest55	0.375	37.171
Nest44	0.872	36.337
Nest33	1.005	46.235
Nest22	1.045	50.729
Nest11	1.467	36.258
Nest109	1.490	36.818
Nest108	0.684	46.473

Table 2. Critical area extraction and CPU time for comb structure layout.

parameter / layout	critical area /(10^{-3}cm^2/defect)	CPU time/s
Comb55	0.391	4.296
Comb44	0.731	4.649
Comb33	0.827	3.736
Comb22	0.849	3.740
Comb11	1.119	4.292
Cobm109	1.271	3.299
Comb108	1.149	3.541
Comb107	0.880	3.938

Table 3. Critical area extraction and CPU time for shake structure layout.

parameter / layout	critical area/(10^{-8}cm^2/defect) vertical /horizontal strips	CPU time/s vertical /horizontal strips
Shake44ver	0.091	6.519
Shake44hor	0.900	18.171
Shake33ver	0.093	7.714
Shake33hor	0.740	20.394
Shake22ver	0.096	9.226
Shake22hor	1.365	25.210
Shake11ver	0.072	17.212
Shake11hor	0.645	19.918
Shake109ver	0.068	9.901
Shake109hor	0.420	19.401
Shake108ver	0.032	11.291
Shake108hor	0.585	25.841
Shake107ver	0.030	16.341
Shake107hor	0.871	39.482

Note that ver stands for vertical, and hor for horizontal.

To verify the rectangular yield model, the experimental results are given below. We assume a $1/x^3$ defect size distribution and a random distribution of defect in length and width respectively. According to the features of the real layout, we obtain 5 defects with different sizes and different outlines, of which maximal circular diameters are 2.5, 3, 4, 5 and 7.9μm, respectively. Correspondingly, their probability distributions are that P_{D1} and P_{D5} each are a few 0.11, P_{D2} is 0.22, P_{D3} is 0.33, and P_{D4} is 0.22. For the real defects, the minimal circle diameter, mean circle diameter, equivalent circle diameter, rectangular outline and fault probability are all calculated as shown in Table 4. From Table 4, it can be proved that a fault probability of 0.2129 caused by the rectangular model is the closest to the true fault probability 0.2089 caused by a real defect outline, that is, the yield caused by the rectangular model is the most approximate to the true yield caused by a real defect outline.

Table 4. Fault probabilities caused by defect models and a real defect.

defect / fault probability	Sm1(1)	Sm2(2)	Sm3(3)	Sm4(2)	Sm5(1)	average value with weight
mean circle	0.0000	0.0000	0.0625	0.3125	1.0000	0.2014
maximal circle	0.0000	0.0625	0.2500	0.4375	1.0000	0.2986
minimal circle	0.0000	0.0000	0.0000	0.1667	1.0000	0.1482
equivalent circle	0.0000	0.0000	0.0000	0.2708	1.0000	0.1713
rectangle	0.0000	0.0431	0.0000	0.4098	1.0000	0.2129
real defect	0.0000	0.0418	0.0000	0.3982	1.0000	0.2089

On the other hand, 23 defects are sampled from among 385 defect samples. For the maximal circular outline, the minimal circular outline, average circular outline and rectangular outline of a defect, the observations show that the errors related to different defect models are respectively 4, 9, 2 and 0. Especially, the fault probability is related not only to the outline of a defect but also to the outline of a layout routing. Since it is assumed that the metallic strips on a layout are long in the vertical or horizontal direction in the above experiment, the error is zero. However, at the ends of a metallic strips, the error may appear for the rectangular model, which will be discussed in author's later paper.

5. Conclusion

Based on the analysis of the yield estimation error in the use of the existing circular model of a real defect, a new yield estimation model has been reported. Because the grid lines in a layout are perpendicular

to each other, the analysis of the fault caused by defects can be converted into the bound measurement of a defect in the horizontal or vertical direction. As a result, the rectangular model of a real defect is presented and confirmed in the experiments. In the final analysis, the different models of a real defect must aim at accurately estimating and improving the yield, so the yield for a rectangular defect model is developed, and the experimental result shows that the new yield estimation model may predict the yield estimation of real defects more accurately than the circular model.

In conclusion, the rectangular model to predict the yield of metallic layer in IC is presented and confirmed by the experimental results. A comparison with the routing layout shows that the new model can be used to estimate yield more accurate than the existing yield estimation model. This approach can have a significant influence on the estimation and improvement of the IC yield.

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