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A threshold voltage model for high-k gate-dielectric MOSFETs considering fringing-field effect*

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In this paper, a threshold voltage model for high-k gate-dielectric metal–oxide–semiconductor field-effect transistors (MOSFETs) is developed, with more accurate boundary conditions of the gate dielectric derived through a conformal mapping transformation method to consider the fringing-field effects including the influences of high-k gate-dielectric and sidewall spacer. Comparing with similar models, the proposed model can be applied to general situations where the gate dielectric and sidewall spacer can have different dielectric constants. The influences of sidewall spacer and high-k gate dielectric on fringing field distribution of the gate dielectric and thus threshold voltage behaviours of a MOSFET are discussed in detail.

Keywords: Threshold voltage, MOSFET, conformal mapping, fringing field
PACC: 7340Q, 1240Q

1. Introduction

The increasing need for smaller and more powerful microprocessors has given an impetus to the reducing of the feature size.[1] It is well known that the channel length, gate-oxide thickness and depletion width of a MOSFET have to be simultaneously shrunk to maintain proper device characteristics.[2] However, a thinner gate oxide can introduce an exponential increase of gate leakage current. To reduce the gate leakage current and standby power, high-dielectric-constant (high-k) materials have been explored as gate dielectrics to replace the conventional SiO_2.[3−5] Recently, the factors influencing the electric characteristics of a high-k gate-dielectric MOSFET have been widely studied,[6−8] but the study of the effects of sidewall spacer on the threshold-voltage behaviour is little involved.

In this work, the gate-dielectric fringing potential is derived through the conformal mapping transformation method considering the influences of both high-k gate-dielectric and sidewall spacer, and then a threshold voltage model based on the distribution is developed. It is the first time that the influence of sidewall spacer on threshold voltage has been involved. As a result, the simulated threshold voltage exhibits good agreement with experimental data. It is proposed that threshold-voltage roll-off of high-k MOSFET can be alleviated by selecting a sidewall spacer with a lower dielectric constant (e.g. SiO_2).

2. Model derivation

A schematic diagram of a high-k gate-dielectric MOSFET with fringing-field lines emanating from the bottom of the gate electrode to the drain and source regions is shown in Fig.1.

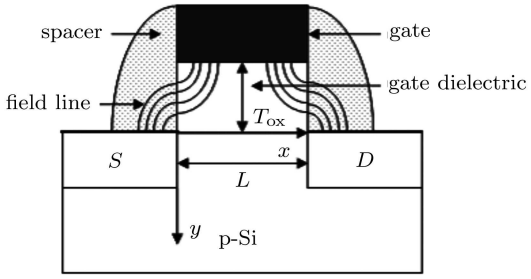


Fig.1. Schematic diagram of a high-k gate-dielectric MOSFET with fringing-field lines.

For simplicity, the polysilicon depletion effect[9,10] and quantum effect[11,12] are neglected. So, the 2D Poisson's equation in the channel region and gate dielectric region, and relevant boundary conditions can be written as

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$$\begin{aligned}
&\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=\begin{cases}0, & -T_{\rm ox}\le y\le 0, \quad 0\le x\le L,\\ \dfrac{{\rm q}N_{\rm A}}{k_{\rm si}}, & 0\le y\le x_{\rm d}, \quad 0\le x\le L,\end{cases}\\
&\varphi(x,-T_{\rm ox})=V_g-V_{\rm fb}, \quad 0\le x\le L,\\
&k_{\rm ox}\frac{\partial\varphi(x,y)}{\partial y}\Big|_{y=0}=k_{\rm si}\frac{\partial\varphi(x,y)}{\partial y}\Big|_{y=0},\\
&\frac{\partial\varphi(x,y)}{\partial y}\Big|_{y=x_{\rm d}}=0,\\
&\varphi(0,y)=g_{\rm s}(y),\\
&\varphi(L,y)=g_{\rm d}(y),
\end{aligned} \tag{1}$$

where $N_{\rm A}$ is the doping concentration of p-type substrate; $k_{\rm ox}$ and $k_{\rm si}$ are permittivities of gate dielectric and substrate respectively; L is the channel length; $x_{\rm d}$ is the width of depletion region in substrate ($x_{\rm d}$ is the variable); $T_{\rm ox}$ is the gate-dielectric thickness; $V_{\rm g}$ is the gate voltage; $V_{\rm fb}$ is the flat-band voltage; $g_{\rm s}(y)$ and $g_{\rm d}(y)$ are the boundary conditions at the source and drain ends respectively. Electric potential $\varphi(x,y)$ can be expressed as a sum of three potentials:

$$\varphi(x,y)=\varphi_0(y)+\varphi_{\rm s}(x,y)+\varphi_{\rm d}(x,y), \tag{2}$$

where $\varphi_0(y)$ is the solution of the 1D Poisson's equation for a long-channel MOSFET; $\varphi_{\rm s}(x,y)$ and $\varphi_{\rm d}(x,y)$ are the channel-potential distributions under the following boundary conditions of the source and drain ends respectively:

$$\begin{aligned}
&\varphi_{\rm s}(L,y)=0,\\
&\varphi_{\rm d}(0,y)=0.
\end{aligned} \tag{3}$$

Once $\varphi_{\rm s}(x,y)$ and $\varphi_{\rm d}(x,y)$ are found, the solution of $\varphi(x,y)$ can be obtained. Substituting expression (3) into expression (2) gives

$$\varphi_{\rm s}(0,y)=\varphi(0,y)-\varphi_0(y), \tag{4}$$

with $\varphi(0,y)$ being the boundary condition at the source end. By using the variational method,[13−15] the functional equation of $\varphi_{\rm s}(x,y)$ is obtained as follows:

$$\begin{aligned}
J(\varphi_{\rm s}(x,y))=\ &\frac{1}{2}\int_0^L {\rm d}x\int_{-T_{\rm ox}}^{x_{\rm ds}+x_{\rm j}}k(y)\\
&\times\left[\left(\frac{\partial\varphi_{\rm s}(x,y)}{\partial x}\right)^2+\left(\frac{\partial\varphi_{\rm s}(x,y)}{\partial y}\right)^2\right]{\rm d}y,
\end{aligned} \tag{5}$$

where $x_{\rm ds}$ is the width of depletion region for source-substrate junction; x_j is the junction depth of source-drain region. Since the right-hand side of the Poisson's equation in Eq.(1) is a constant, the solution of $\varphi_{\rm s}(x,y)$ can be decomposed and written as

$$\varphi_{\rm s}(x,y)=\phi_{\rm s}(y)f_{\rm s}(x). \tag{6}$$

To satisfy expression (3), the boundary conditions of $f_{\rm s}(x)$ in Eq.(6) are adopted as follows:

$$\begin{aligned}
&f_{\rm s}(0)=1,\\
&f_{\rm s}(L)=0.
\end{aligned} \tag{7}$$

Equations (6) and (7) give

$$\varphi_{\rm s}(0,y)=\phi_{\rm s}(y). \tag{8}$$

Substituting expression (8) into expression (4) yields

$$\phi_{\rm s}(y)=\varphi(0,y)-\varphi_0(y). \tag{9}$$

Substituting Eq.(6) into Eq.(5) gives

$$\begin{aligned}
J(\varphi_{\rm s}(x,y))=&\frac{1}{2}\int_0^L {\rm d}x\int_{-T_{\rm ox}}^{x_{\rm ds}+x_{\rm j}}k(y)\left[\phi_{\rm s}^2(y)\left(\frac{\partial f_{\rm s}(x)}{\partial x}\right)^2\right.\\
&\left.+f_{\rm s}^2(x)\left(\frac{\partial\phi_{\rm s}(y)}{\partial y}\right)^2\right]{\rm d}y.
\end{aligned} \tag{10}$$

The Euler function of Eq.(10) is

$$l_{\rm s}^2\frac{{\rm d}^2f_{\rm s}(x)}{{\rm d}x^2}-f_{\rm s}(x)=0, \tag{11}$$

where $l_{\rm s}$ is the characteristic length for $\varphi_{\rm s}(x,y)$ and given by

$$l_{\rm s}=\left[\frac{\int_{-T_{\rm ox}}^{x_{\rm ds}+x_{\rm j}}k(y)\phi_{\rm s}^2(y){\rm d}y}{\int_{-T_{\rm ox}}^{x_{\rm ds}+x_{\rm j}}k(y)\left[\frac{{\rm d}\phi_{\rm s}(y)}{{\rm d}y}\right]^2{\rm d}y}\right]^{1/2} \tag{12}$$

with

$$k(y)=\begin{cases}k_{\rm ox}, & -T_{\rm ox}\le y\le 0,\\ k_{\rm si}, & 0\le y\le x_{\rm ds}+x_{\rm j}.\end{cases} \tag{13}$$

Then, $f_{\rm s}(x)$ can be found from Eq.(11) to be

$$f_{\rm s}(x)=\frac{\sinh[(L-x)/l_{\rm s}]}{\sinh(L/l_{\rm s})}. \tag{14}$$

Substituting expressions (9) and (14) into expression (6) gives

$$\varphi_{\rm s}(x,y)=[\varphi(0,y)-\varphi_0(y)]\frac{\sinh[(L-x)/l_{\rm s}]}{\sinh(L/l_{\rm s})}. \tag{15}$$

Similarly, $\varphi_{\rm d}(x,y)$ can be derived as follows:

$$\varphi_{\rm d}(x,y)=[\varphi(L,y)-\varphi_0(y)]\frac{\sinh[x/l_{\rm d}]}{\sinh(L/l_{\rm d})}, \tag{16}$$

where $l_{\rm d}$ is the characteristic length for $\varphi_{\rm d}(x,y)$ and written as

$$l_{\rm d}=\left[\frac{\int_{-T_{\rm ox}}^{x_{\rm dd}+x_{\rm j}}k(y)\phi_{\rm d}^2(y){\rm d}y}{\int_{-T_{\rm ox}}^{x_{\rm dd}+x_{\rm j}}k(y)\left[\frac{{\rm d}\phi_{\rm d}(y)}{{\rm d}y}\right]^2{\rm d}y}\right]^{1/2} \tag{17}$$

with

$$\phi_{\rm d}(y)=\varphi(L,y)-\varphi_0(y), \tag{18}$$

where $x_{\rm dd}$ is the width of depletion region for drain-substrate junction; $\varphi(L,y)$ is the boundary condition at the drain end. For a low drain voltage ($V_{\rm ds}$) (e.g. 50 mV), $l_{\rm d}\approx l_{\rm s}\equiv l$, which is defined as a common characteristic length. Substituting expressions (15) and (16) into expression (2), the channel potential can be expressed as

$$\begin{aligned}\varphi(x,y)=\ &\varphi_0(y)+[\varphi(0,y)-\varphi_0(y)]\frac{\sinh[(L-x)/l]}{\sinh(L/l)}\\ &+[\varphi(L,y)-\varphi_0(y)]\frac{\sinh(x/l)}{\sinh(L/l)}.\end{aligned} \tag{19}$$

Based on expression (19), the location x_0 of the minimum surface potential ($\varphi_{\rm sf\ min}$) in the channel can be determined by $\left.\frac{{\rm d}\varphi(x,y)}{{\rm d}x}\right|_{y=0}=0$, and given as follows:

$$\begin{aligned}x_0=\ &\frac{L}{2}+\frac{l}{2}\ln\{[(V_{\rm bi}-\varphi_0(x))-(V_{\rm bi}+V_{\rm ds}-\varphi_0(x))\exp(L/l)]\\ &\times[(V_{\rm bi}+V_{\rm ds}-\varphi_0(x))-(V_{\rm bi}-\varphi_0(x))\exp(L/l)]^{-1}\}.\end{aligned} \tag{20}$$

Substituting x_0 into expression (19), $\varphi_{\rm sf\ min}$ can be determined. The threshold voltage is determined by $\varphi_{\rm sf\ min}=2\phi_{\rm f}$, where $\phi_{\rm f}=\frac{k_{\rm b}T}{q}\ln\frac{N_{\rm A}}{n_{\rm i}}$ is the Fermi potential of the substrate. Thus, for a small $V_{\rm ds}$, the threshold voltage can be expressed as

$$V_{\rm th}=V_{\rm th0}-\frac{[2(V_{\rm bi}-2\phi_{\rm f})+V_{\rm ds}]}{2\cosh(L/2L)-2}, \tag{21}$$

where $V_{\rm bi}$ is the built-in potential of the source-substrate and drain-substrate junctions. In order to calculate the threshold voltage in Eq.(21), the characteristic length l must be known first. So, it is important to derive the boundary conditions of $\varphi(0,y)$ and $\varphi(L,y)$ to calculate l according to expressions (9) and (12).

Figure 2(a) depicts the fringing field lines near the interface between the gate dielectric and spacer at the drain end in the complex $U+{\rm j}P$ coordinate system (U is the abscissa and P is the ordinate), denoted as $u-p$ coordinate system. The $u-p$ coordinate system is a mapping from the real $x-y$ coordinate system in Fig.1, by using mapping functions of $u=-L+x, p=-y$. $V(p)$ (i.e. $V(0,p), 0\le p\le T_{\rm ox}$) is the fringing potential distribution at the interface in the $u-p$ coordinate system, which corresponds to $\varphi(L,y)(-T_{\rm ox}\le y\le 0)$ in the $x-y$ coordinate system.

It is assumed that the potential between p and $p+{\rm d}p$ is $V(p)$ as shown in Fig.2(b). At the interface between the spacer and gate dielectric, we have

$$k_{\rm ox}E_{11}=k_1E_1, \tag{22}$$

where k_1 is permittivity of the spacer. Now the system can be mapped into an equivalent parallel-plate system by transforming the $u-p$ coordinates to the $\eta-\xi$ coordinates. The mapping functions are given as follows:

$$\eta+{\rm j}\xi=f(u+{\rm j}p), \tag{23}$$

with

$$\begin{aligned}u&={\rm e}^{\eta}\cos(\xi),\\ p&={\rm e}^{\eta}\sin(\xi),\end{aligned} \tag{24}$$

thus

$$\eta=\ln\sqrt{u^2+p^2}. \tag{25}$$

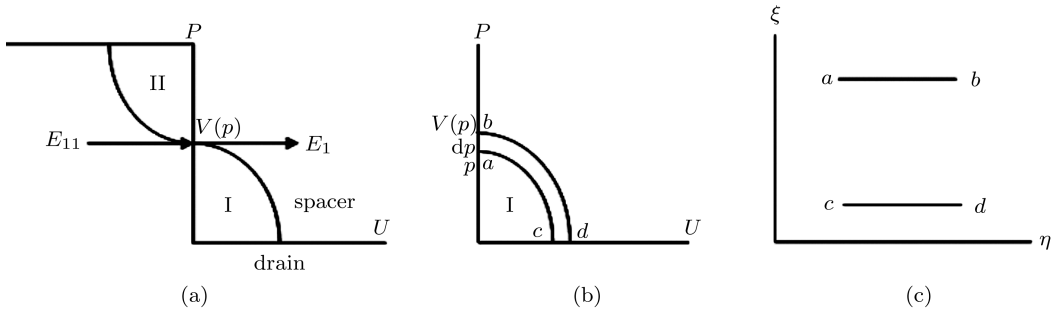


Fig.2. (a) Cross-section near the interface between the gate dielectric and the spacer at the drain end with fringing field lines, (b) and (c) the fringing field lines in the spacer before and after conformal mapping for model derivation. (a) and (b) are in u-p coordinate system, and (c) is in the η-ξ coordinate system.

Region I of the spacer is transformed, and the mapped result is shown in Fig.2(c). In the $\eta-\xi$ coordinate system, the capacitance per unit length is given by

$$C_1(p) = k_1 \frac{\eta_{bd} - \eta_{ac}}{\xi_{ab} - \xi_{cd}}. \tag{26}$$

Substituting points $a(0, p)$ and $c(p, 0)$ into expression(24) yields

$$\begin{aligned} \xi_{ab} &= \frac{\pi}{2}, \\ \xi_{cd} &= 0. \end{aligned} \tag{27}$$

Inserting points $a(0, p)$ and $b(0, p+\mathrm{d}p)$ into expression (25) gives

$$\eta_{bd} - \eta_{ac} = \ln(p + \mathrm{d}p) - \ln p. \tag{28}$$

Substituting expressions (27) and (28) into expression (26), the capacitance per unit length of the region I is calculated to be

$$C_1(p) = \frac{2k_1}{\pi}[\ln(p + \mathrm{d}p) - \ln p]. \tag{29}$$

According to the theory of electromagnetism, $C_1(p)$ can be also expressed as

$$C_1(p) = k_1 \frac{E_1(p)}{V(p) - (V_{\mathrm{bi}} + V_{\mathrm{ds}})}. \tag{30}$$

Thus, a comparison between expressions (29) and (30) leads to

$$E_1(p) = \frac{2}{\pi} \frac{(V(p) - (V_{\mathrm{bi}} + V_{\mathrm{ds}}))}{p} \tag{31}$$

Similarly, $E_{11}(p)$ for region Π in the gate dielectric can be expressed as

$$E_{11}(p) = \frac{2}{\pi} \frac{((V_{\mathrm{g}} - V_{\mathrm{fb}}) - V(p))}{T_{\mathrm{ox}} - p} \tag{32}$$

Substituting expressions (31) and (32) into Eq.(22), the distribution of gate-dielectric fringing potential can be derived as follows:

$$V(p) = \frac{k_{\mathrm{ox}} p(V_{\mathrm{g}} - V_{\mathrm{fb}}) + k_1(V_{\mathrm{bi}} + V_{\mathrm{ds}})(T_{\mathrm{ox}} - p)}{k_1(T_{\mathrm{ox}} - p) + k_{\mathrm{ox}} p}. \tag{33}$$

The classical boundary conditions are used for $\varphi(L, y)$ in the substrate region ($0 \le y \le x_{\mathrm{j}} + x_{\mathrm{dd}}$). Thus, when V_{ds} is so small that it can be ignored, the boundary conditions at the drain end for the high-k gate-dielectric MOSFET are

$$\varphi(L, y) = \begin{cases} \dfrac{k_{\mathrm{ox}} y(V_{\mathrm{g}} - V_{\mathrm{fb}}) - k_1 V_{\mathrm{bi}}(T_{\mathrm{ox}} + y)}{k_{\mathrm{ox}} y - k_1(T_{\mathrm{ox}} + y)}, & -T_{\mathrm{ox}} \le y \le 0, \\ V_{\mathrm{bi}}, & 0 \le y \le x_{\mathrm{j}}, \\ V_{\mathrm{bi}} \left(1 - \dfrac{y}{x_{\mathrm{dd}}}\right)^2, & x_{\mathrm{j}} \le y \le x_{\mathrm{j}} + x_{\mathrm{dd}}, \end{cases} \tag{34}$$

and

$$\varphi(0, y) = \varphi(L, y). \tag{35}$$

Thus, substituting expressions (35) (8),(9) and (12) into expression (21), the threshold voltage can be obtained. This is a threshold voltage model including the fringing-field effect. It should be noted that when $k_1 = k_{ox}$, the first part on the right-hand side of expression (34) becomes a linear function of y, and thus the proposed model is identical to the linear fringing potential (LFP) model. In other words, the LFP model is only a special case of the proposed model, and thus becomes less accurate for MOSFETs with different permittivities for their gate dielectric and sidewall spacer.

3. Results and discussion

The simulated results are compared with experimental data in Fig.3. The simulated results of threshold voltage exhibit good agreement with experimental ones for MOSFET with SiO_2 as gate dielectric,[16] indicating the validity of this model.

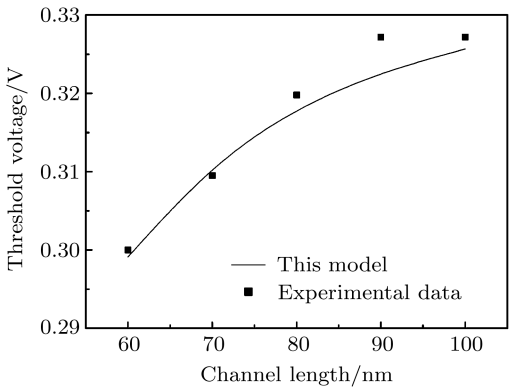


Fig.3. Comparison between simulated and experimental threshold voltages of MOSFET with SiO_2 gate dielectric.

As can be seen from expression (34), the gate-dielectric fringing potential, thus threshold voltage, is affected by the dielectric constant k_{ox} of gate dielectric. Figure 4 describes the influences of dielectric constant k_{ox} and channel length L on the threshold voltage roll-off for devices with a SiO_2 spacer (k_1=3.9) and an equivalent oxide thickness (EOT) of 2 nm. For a large k_{ox}, the threshold voltage begins to decrease at a larger channel length (e.g. L=200 nm), due to the enhanced fringing-field effects. In other words, for a given channel length, the larger the k_{ox}, the stronger the influence of the fringing field on the threshold voltage, and thus the weaker the control of gate voltage on the channel potential.[17] Therefore, the fringing-field effect can be well described by this model, which is important for accurately calculating the threshold voltage for a small MOSFET with a high-k material as gate dielectric. On the other hand, for a given k_{ox}, with the channel length shrinking, the threshold voltage roll-off increases, indicating the influence of the short-channel effect on V_{th}. These results show that the threshold voltage roll-off is influenced by both the fringing-field effect and short-channel effect. In addition, as shown in Fig.4, the threshold voltage roll-off of the LFP model is larger than that of our model. This is because the k_1 value in the LFP model is always set to be k_{ox}, resulting in the enhancing of fringing-field effect due to the higher-k spacer, and thus a larger threshold voltage roll-off for a MOSFET with high-k gate dielectric.

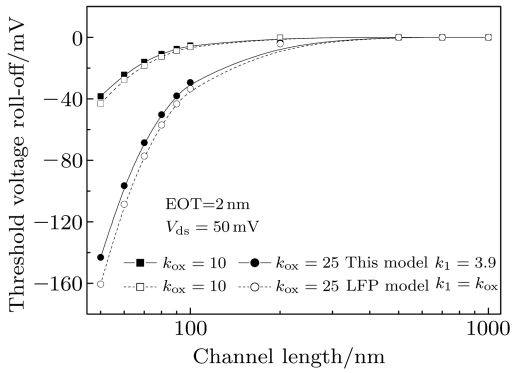


Fig.4. Dependence of threshold voltage roll-off on channel length for different values of k_{ox}.

The influence of sidewall spacer on surface potential is shown in Fig.5. For a given value of k_{ox} (i.e. gate dielectric permittivity), the surface potential increases with k_1 value of sidewall spacer increasing. This means that sidewall spacer with a high dielectric

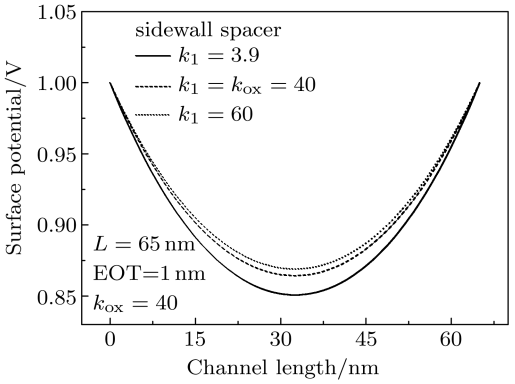


Fig.5. The influence of k_1 value of sidewall spacer on surface potential for a given gate dielectric permittivity k_{ox}.

constant can degrade the fringing-induced barrier-lowering (FIBL) effect,[18] thus leading to a larger

threshold voltage roll-off. The fringing potentials corresponding to the different surface potentials are shown in Fig.6. It is obviously seen that the fringing potential at the same position for low-k_1 (such as k_1=3.9) is higher than that for high-k_1 (such as k_1=k_{ox}=40 and k_1= 60). The result shows that the low-k_1 spacer for a high-k MOSFET can confine the electric field within the channel region and thus the control of gate voltage over the channel potential is strengthened, leading the FIBL effect to weaken.

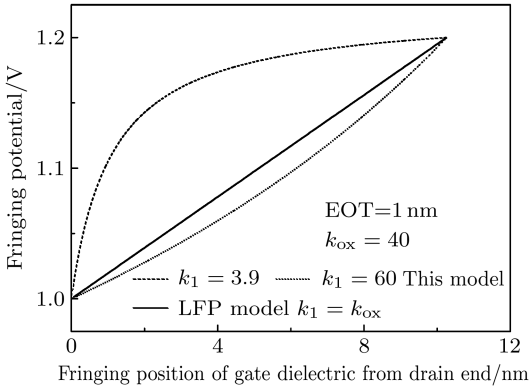


Fig.6. Gate-dielectric fringing-potential distribution for spacer with different values of k_1 (for the LFP model, $k_1 = k_{ox}$).

The expression $V_{off} = |V_{k_1}| - |V_{SiO_2}|$ can be employed to show the influence of sidewall spacer on threshold voltage. Here, V_{SiO_2} is the threshold voltage with SiO_2 spacer, V_{k_1} is the threshold voltage with another kind of spacer ($k_1 > 3.9$). For a given value of k_{ox}, V_{off} (which is 16 mV for k_{ox} = 30, and 24 mV for k_{ox}= 40) increases with k_1 in an approximately linear manner as shown in Fig.7. This shows that the low-k_1 value of sidewall spacer can reduce V_{off} (i.e. threshold voltage roll-off). It is because the confining as stated above is strengthened, which is especially obvious for the case with larger values of k_{ox} (see the comparison between the cases of k_{ox}=30 and k_{ox}=40). The influence of sidewall spacer on threshold voltage is described, which is involved for the first time. It is well known that the value of k_{ox} itself is a major factor that causes the threshold voltage to degrade because of the FIBL effect resulting from the high-k_{ox} gate dielectric. However, the function of sidewall spacer cannot be ignored to accurately model the threshold voltage of high-k MOSFET when considering the fringing field effect.

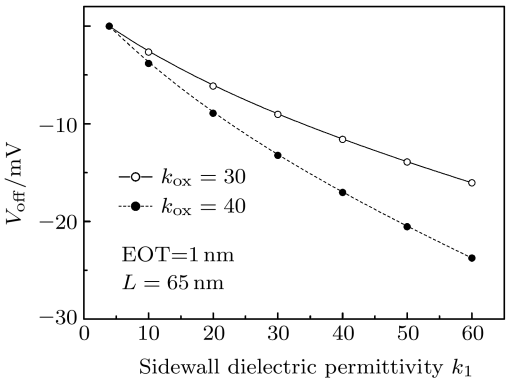


Fig.7. Threshold voltage roll-off caused by sidewall spacer.

In summary, when a high-k material is used to replace SiO_2 as gate dielectric, the fringing-field effect is greatly enhanced, and becomes a dominant factor of causing the threshold-voltage degradation of MOSFET. On the other hand, if a suitable spacer of low-k_1 dielectric is used for a small MOSFET with high-k gate dielectric, the threshold properties can be improved.

4. Conclusions

The fringing potential for the high-k gate dielectric of a small MOSFET is derived by using the conformal mapping transformation method. Base on the potential distribution, a threshold voltage model is developed with more accurate fringing-field effects including the influences of sidewall spacer and high-k gate-dielectric. Thus, the fringing field effect is described. In addition, the short-channel effect is included in this model. The simulated results match well with experimental data, indicating the validity of this model. The influence of device parameters on the threshold voltage behaviour is investigated, and it is found that low-k_1 sidewall spacer can improve the behaviour of the threshold voltage for a small MOSFET with high-k gate dielectric.

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