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Tradeoff between speed and static power dissipation of ultra-thin body SOI MOSFETs*

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The speed performance and static power dissipation of the ultra-thin-body (UTB) MOSFETs have been comprehensively investigated, with both DC and AC behaviours considered. Source/drain extension width (L_{sp}) and silicon film thickness (t_{si}) are two independent parameters that influence the speed and static power dissipation of UTB silicon-on-insulator (SOI) MOSFETs respectively, which can result in great design flexibility. Based on the different effects of physical and geometric parameters on device characteristics, a method to alleviate the contradiction between power dissipated and speed of UTB SOI MOSFETs is proposed. The optimal design regions of t_{si} and L_{sp} for low operating power and high performance logic applications are given, which may shed light on the design of UTB SOI MOSFETs.

Keywords: ultra-thin-body, SOI, MOSFET, simulation
PACC: 7280C, 7340Q, 7360J

1. Introduction

In most applications, low power dissipation and high speed performance of devices are the most important requirements.[1] The ultra-thin-body (UTB) silicon-on-insulator (SOI) MOSFET has been considered as a potential candidate for CMOS devices in the nanoscale regime, due to the effective suppression of short-channel effects and leakage current.[2−9] However, silicon film thickness reduction can result in some negative influence on the driving current of UTB SOI MOSFETs. Moreover, few reports have been presented on dealing with the AC behavior of UTB SOI MOSFETs. The speed and static power dissipation characteristics of UTB SOI MOSFETs have been rarely studied from the AC behavior consideration. So it is necessary for us to make a comprehensive analysis of the speed and the power dissipation of UTB SOI MOSFETs.

In this paper, an extensive study of the speed and the static power dissipation of UTB SOI MOSFETs has been carried out. The influence of fundamental physical and geometric device parameters on the speed and power dissipation is analysed in detail, through the simulated of DC and AC characteristics of UTB SOI MOSFETs. The simulated results show that silicon film thickness cannot decrease incessantly for high performance applications, since the rapid increase of intrinsic gate capacitance (C_{gg}) can cause the intrinsic delay to become larger and thus worsen the performance. It is also shown that source/drain extension width L_{sp} and silicon film thickness t_{si} have independent influence on the speed and the static power dissipation, which provides an effective method to choose the appropriate device parameters for UTB SOI MOSFETs. Here a new procedure is presented to achieve the nanoscale UTB SOI MOSFET design to alleviate the contradiction between the static power dissipation and high speed. Finally, the optimal regions are shown for high performance and low power UTB SOI MOSFET design, which exhibits a relatively wider design window.

This paper is organized as follows. Section 2 presents the simulated structure and simulation methodology. Section 3 gives the obtained simulation results and discussion. Finally the conclusion is given in Section 4.

2. Simulation structure and methodology

UTB SOI MOSFETs with 50nm gate length, quasi-intrinsic channel (5×10^{14} cm^{-3}), 2 nm gate ox-

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ide, and 400 nm buried oxide have been simulated with a two-dimensional device simulator-ISE8.0. The schematic cross sectional view of the simulated structure is shown in Fig.1. To minimize the impact of source/drain parasitic resistance, the elevated S/D structure is adopted. The doping concentration for the deep source/drain and source/drain extension regions are fixed at 1×10^{20} cm^{-3} and 1×10^{19} cm^{-3} respectively. In this work, DC and AC characteristics of UTB SOI MOSFETs dependent on the silicon body thickness $t_{\rm si}$ and the source/drain extension width $L_{\rm sp}$, ranging from 2 to 20 nm and from 5 to 40 nm respectively, are intensively investigated.

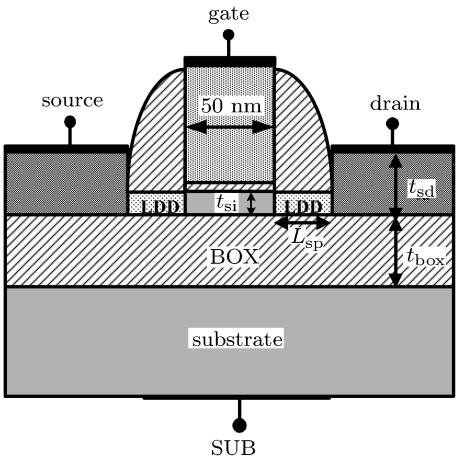


Fig.1. The schematic cross sectional view of a UTB SOI MOSFET with 50nm gate length, quasi intrinsic channel (5×10^{14} cm^{-3}), 2 nm gate oxide, and 400 nm buried oxide.

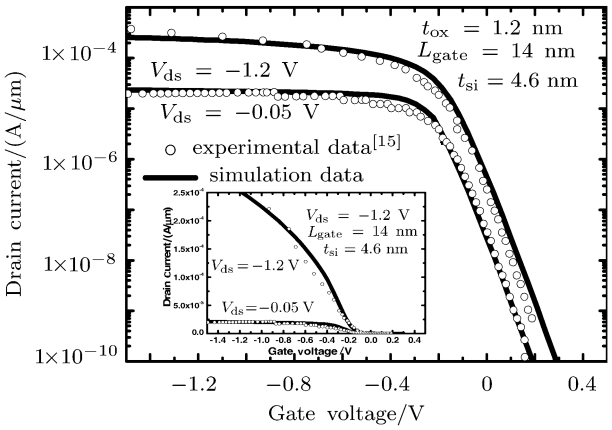


Fig.2. Comparison between experimental data and simulation results for the $I_{\rm ds}-V_{\rm gs}$ characteristic of a UTB SOI p-FET with 14 nm gate length and 4.6 nm silicon film thickness. The inset shows the comparison on a linear scale.

Device AC simulation in simulator DESSIS from ISE is performed in a mixed mode.[10] UTB SOI MOSFET devices have been simulated through self-consistent solution of Poisson, continuity, and thermodynamic equations. Phonon scattering model, doping dependent model, high field saturation model and the model that accounts for the mobility degradation at interfaces are all included in the carrier mobility model. The density gradient model, which accounts for quantum effects, and the hydrodynamic model are included, providing an accurate simulation for transistors with ultra thin bodies. Figure 2 shows the comparison of the current of drain-source against the voltage of gate-source ($I_{\rm ds}-V_{\rm gs}$) characteristic of a 14 nm gate length ($L_{\rm gate}$) UTB SOI p-FET between experimental data and simulated results, and the inset shows the comparison on a linear scale. It can be seen that the simulated results are in a good agreement with the experimental data.

3. Results and discussion

3.1. Impact of the silicon body thickness on the intrinsic gate delay and static power dissipation

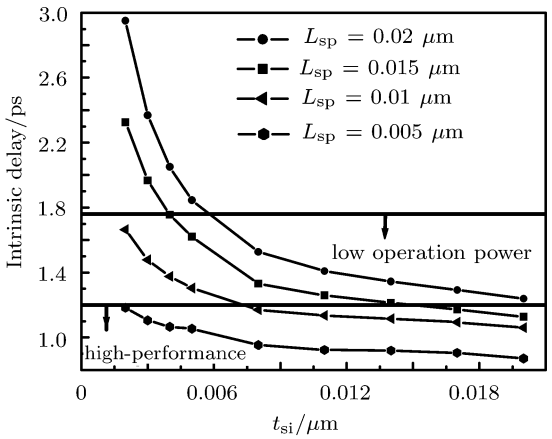


Fig.3. Intrinsic delay (CV/I) as a function of silicon film thickness ($t_{\rm si}$) for different source/drain extension widths ($L_{\rm sp}$).

Silicon body thickness $t_{\rm si}$ is one of the most important parameters in UTB SOI MOSFETs. Figures 3 and 4 show the $t_{\rm si}$ dependence of the intrinsic delay and static power dissipation for different $L_{\rm sp}$ respectively. From Figs. 3 and 4, it is clearly seen that with decreasing $t_{\rm si}$ intrinsic delay increases, while static power dissipation reduces rapidly. This can be understood in terms of both the smaller on-current and off-current corresponding to thinner silicon film because the short channel effects can be effectively sup-

pressed and leakage current can be greatly decreased for a thinner silicon film. It is worth noting that the intrinsic gate delay shows a gentle increase for a thicker film. However, when t_{si} is less than approximate 8 nm, the gate delay rate goes up distinctly.

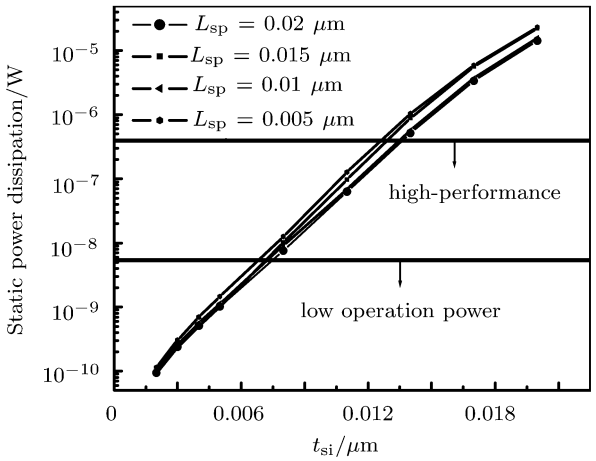


Fig.4. Static power dissipation as a function of silicon film thickness (t_{si}) for different source/drain extension widths (L_{sp}).

To help understand these phenomena, C_{gg} and electron density profiles for different t_{si} are investigated, where C_{gg} is extracted when V_{gs} = 1 V and V_{ds} = 0 V to obtain the worst time delay. Figure 5 plots the curves of C_{gg} versus t_{si}. The curve shows that C_{gg} decreases in the region of $t_{si} > 8$ nm and increases when t_{si} is below 8 nm. Therefore, there is a minimal value at t_{si} = 8 nm. The thinner silicon body gives rise to about 7 percent increase of gate capacitance which will greatly influence the characteristics of UTB SOI MOSFETs, especially in the nano-regime. Figure 6 depicts the electron density distribution across the silicon film ranging from 20 to 2 nm. The peak value of the electron density is at the channel surface in the case of thick silicon film, and changes when the silicon thickness is less than 20 nm. Due to quantization effect, the peak value of the electron density departs gradually from the channel surface and C_{gg} reduces as t_{si} decreases. On the other hand, high electric fields in strong inversion regions and ultra thin silicon film can confine the electron density distribution. When t_{si} further decreases, the confinement becomes more and more serious and G_{gg} increases. Consequently, the increase of G_{gg} results in the rapid rise of the intrinsic delay as t_{si} is thinner than approximately 8 nm. From DC characteristics of UTB SOI MOSFETs, The increased C_{gg} favours device performance. However, it may induce the significant increase of intrinsic delay. Therefore, for high performance requirements, too thin a body of t_{si} is not favourable.

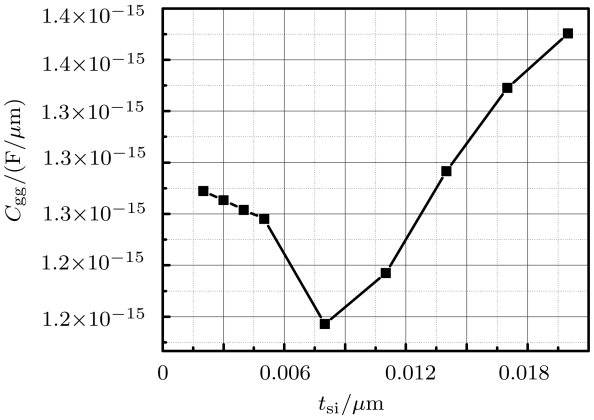


Fig.5. Intrinsic gate capacitance (C_{gg}) as a function of silicon film thickness (t_{si}).

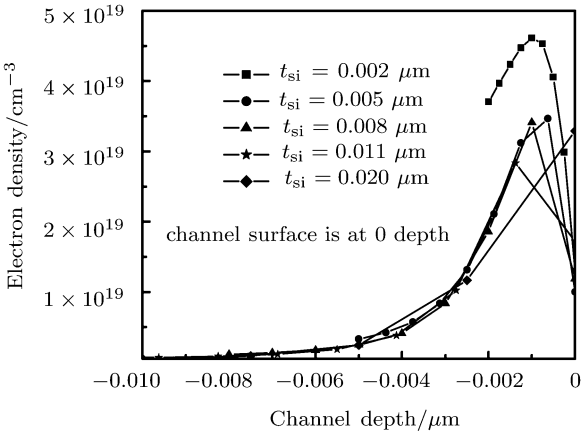


Fig.6. The electron density distribution across the silicon film for different silicon film thickness (t_{si}).

3.2. Impact of source/drain extension width L_{sp} on the intrinsic gate delay and static power dissipation

Because of the ultra thin body thickness of UTB SOI MOSFETs, source/drain extension width L_{sp} plays a very important role in the performance of UTB SOI MOSFETs. The L_{sp} influences not only the drive current due to the series resistance, but also the AC characteristics because of the parasitic capacitance between the gate and source/drain. In this section, the optimization of L_{sp} will be investigated in detail for the first time to the best of our knowledge.

Figure 7 shows the L_{sp} dependence of the intrinsic delay and static power dissipation for different t_{si}. As L_{sp} becomes wider, the curves show a large increase

of intrinsic delay (CV/I) for thin silicon film because of the higher parasitic resistance. From Fig.7, special attention needs to be paid to the lower sensitivity of the static power to $L_{\rm sp}$, which is very helpful to the device design. The most important function of the $L_{\rm sp}$ is the immunity of the drain-induced barrier lowering. The negligible influence of $L_{\rm sp}$ on the suppression of short channel effect leads to the static power dissipation remaining approximately constant.

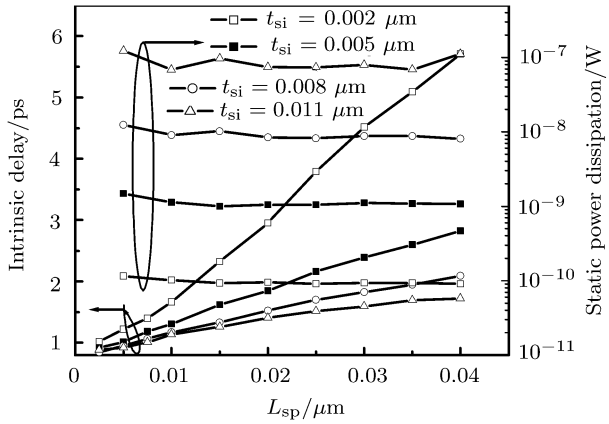


Fig.7. Variation of intrinsic delay and static power dissipation with different silicon film thickness ($t_{\rm si}$) as a function of source/drain

3.3. Method to alleviate the contradiction between power and speed for UTB SOI MOSFETs

A contradiction between power and speed generally exists in the device design. It is difficult to achieve better optimization of both power and speed. In this section, a method is put forward to alleviate the contradiction between power and speed for UTB SOI MOSFETs, which utilizes the different influences of various parameters on device characteristics.

From descriptions in Sections 3.1 and 3.2, it is clearly seen that static power dissipation is insensitive to the change of $L_{\rm sp}$. However, the influence of the $L_{\rm sp}$ on intrinsic delay is significant, especially for thinner silicon film, which can be seen from Fig.7. On the other hand, silicon body thickness $t_{\rm si}$ has great impact on static power dissipation. As $t_{\rm si}$ decreases, intrinsic delay increases moderately, as can be seen from Figs.3 and 4. Therefore, by adjusting $L_{\rm sp}$ and $t_{\rm si}$ separately, both the speed and power dissipation requirements can be satisfied. First, according to the speed specification, $L_{\rm sp}$ is adjusted to achieve the speed satisfaction. At the same time, the influence of the width variation on static power dissipation is negligible. Next, $t_{\rm si}$ can be chosen to satisfy the static power dissipation requirements. Only several iterations are required to meet both static power dissipation and speed requirements satisfactorily. The whole flow chart is illustrated in Fig.8.

From the specifications with 50 nm physical gate length of the intrinsic delay and static power dissipation of the Roadmap'01,[11] Fig.9 gives the design region of $L_{\rm sp}$ and $t_{\rm si}$ to satisfy the low operating power and high-performance logic application requirements. It can be seen that $L_{\rm sp}$ less than 10 nm is necessary in the region of $t_{\rm si} < 8$ nm for the high-performance logic applications, which is very difficult for fabrication.

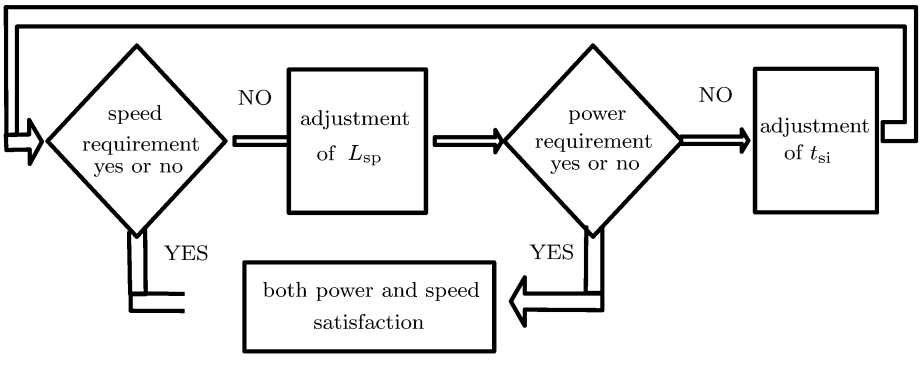


Fig.8. The flow chart for choosing device parameters to achieve excellent performance.

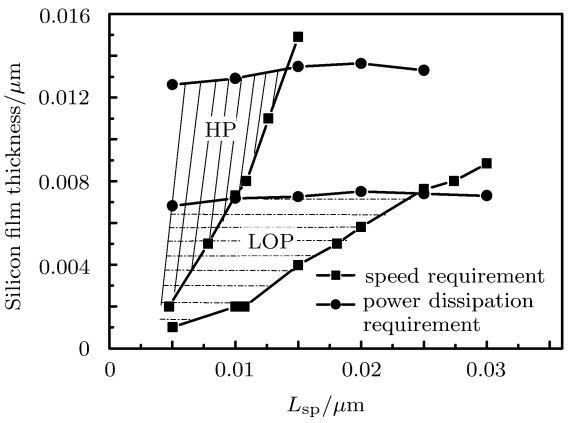


Fig.9. Optimal design regions of silicon film thickness (t_{si}) and source/drain extension width (L_{sp}) for low operating power (LOP) and high-performance (HP) logic applications.

4. Conclusions

A systematic and comprehensive study of speed and static power dissipation of UTB SOI MOSFETs has been performed. The influence of the device parameters (L_{sp} and t_{si}) upon the characteristics, such as intrinsic gate capacitance, gate delay, and static power dissipation, is analysed. The decrease of silicon body thickness reduces the static power dissipation and improves device DC characteristics effectively. However, it is unadvisable to decrease the silicon body thickness t_{si} continually for high performance applications since intrinsic delay may increase significantly with decreasing t_{si} below 8 nm. The influence of L_{sp} on intrinsic delay is obvious, especially for ultra thin body. A method to alleviate the contradiction between power and speed of UTB SOI MOSFETs, which utilizes the independent influence on the speed and static power dissipation of UTB SOI MOSFETs, is proposed in this paper. The optimal design region for high performance and low power applications is presented. The results may provide important guideline for optimal device design.

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