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Degradation characteristics and mechanism of PMOSFETs under NBT–PBT–NBT stress*

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Degradation characteristics of PMOSFETs under negative bias temperature–positive bias temperature–negative bias temperature (NBT–PBT–NBT) stress conditions are investigated in this paper. It is found that for all device parameters, the threshold voltage has the largest shift under the first NBT stress condition. When the polarity of gate voltage is changed to positive, the shift of device parameters can be greatly recovered. However, this recovery is unstable. The more severe degradation appears soon after reapplication of NBT stress condition. The second NBT stress causes in linear drain current to degrade greatly, which is different from that of the first NBT stress. This more severe parameter shift results from the wear out of silicon substrate and oxide interface during the first NBT and PBT stress due to carrier trapping/detrapping and hydrogen related species diffusion.

Keywords: ultra deep submicron PMOSFETs, negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), interface traps

PACC: 7340Q, 7300, 7220J

1. Introduction

As the MOSFET's size is continuously scaled down without reducing supply voltages appropriately, its reliability has become more and more important such as negative bias temperature instability (NBTI),[1−3] hot carrier injection (HCI)[4−6] and time dependent dielectric breakdown (TDDB).[7] Although NBTI has been studied for many years, its further investigation has never stopped. NBTI in PMOSFETs represents a major reliability concern in modern CMOS technologies. Though more than thirty years ago the first observation in nonvolatile memory devices, NBTI has now become an important reliability concern for mainstream digital, as well as analogue CMOS circuits. It has been shown that the device lifetime will be determined by NBTI more than HCI as devices scale down to 0.25 μm.

In general, NBTI is attributed to the generation of interface traps and positive oxide fixed charges during stress at silicon substrate and oxide interface. Though a number of attempts have been made to investigate the mechanism of NBTI, none has attempted to explain the full experimental data within a common framework, and little attention is paid to the interaction of NBTI and positive bias temperature instability (PBTI). This paper shows an understanding of the degradation phenomena of NBT in PMOSFETs under alternating NBT–PBT–NBT stress bias, and presents the role of the hydrogen during NBT–PBT–NBT stress based on the degradation phenomena of PMOSFETs.

2. Experiments

Experiments were performed on surface channel lightly doped drain (LDD) PMOSFETs, having t_{ox} of 5 nm, channel width of 8 μm and length of 0.25 μm. The gate oxides of all devices were annealed in N_2O ambient after thermal growth. All tests were completed by HP4156B high precise semiconductor parameter analyzer in dry air. Stressing was performed at logarithmic time intervals, which were periodically stopped to measure device characteristics. Threshold voltage was measured for all stress cases from I_d–V_g curve by using maximum slope method with drain voltage −0.05 V. The typical stress condition is illus-

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trated in Fig.1.

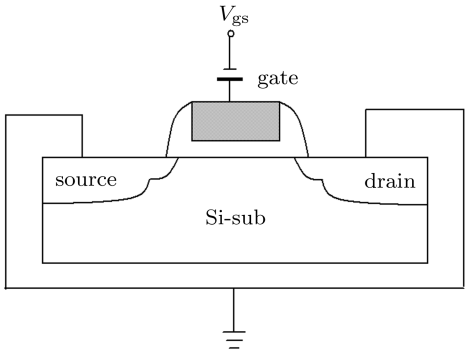


Fig.1. Configuration of stress condition.

The device was stressed with constant negative gate voltage and temperature with source, drain and substrate grounded. PBT stress was also performed after NBT stress, which biases device with a positive gate voltage whose absolute value equals to that of NBT. NBT stress is applied again after the PBT stress. Typical stress temperature lies in 120 °C, ranging with oxide electric field typically around 8MV/cm, such field and temperature are typically encountered during burn in, which also approach high performance ICs during routine operation.

3. Results and discussion

3.1. Device degradation under NBT stress

NBT stress ($V_g = -4.25\,V, T = 120\,°C$, $t = 10000\,s$) is applied to PMOSFETs. Figures 2(a) and 2(b) show the dependence of threshold voltage V_{th}, transconductance G_{mmax}, saturation drain current I_{dsat} and linear drain current I_{dlin} shift on the NBT stress time in linear scale and logarithmic scale respectively. These device parameters shifts obey the linear time dependence in logarithmic scale. $V_{th}, I_{dsat}, I_{dlin}$ and G_{mmax} shift 8.1%, 4.6%, 3.2% and 2.3% respectively.

The whole process can be explained below. Holes are activated thermally and gain enough energy to dissociate the interface defects by the vertical electric field near the LDD regions. The fixed oxide charges and interface states are generated by the impact of hot holes on the hydrogen-terminated silicon dangling bonds, the positive oxide charges mainly contribute to the V_{th} shift.

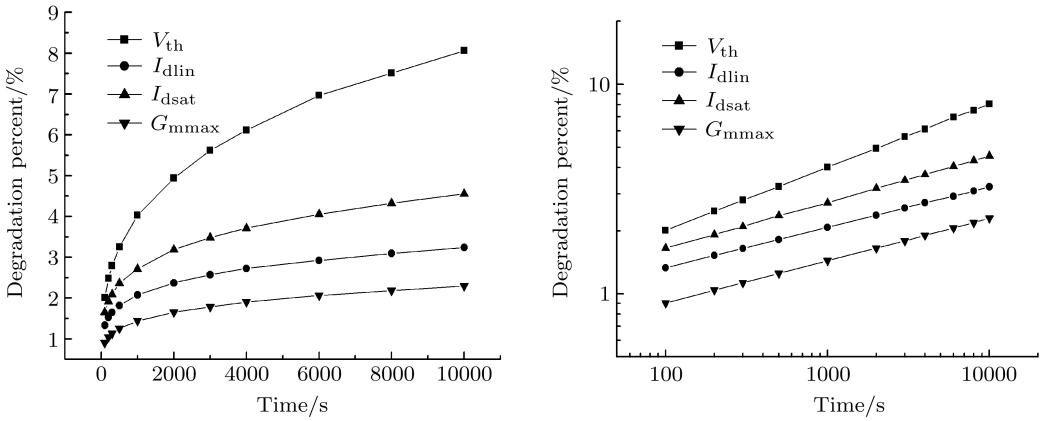


Fig.2. (a) Device parameters degradation induced by NBT stress versus time (linear scale). (b) Device parameters degradation induced by NBT stress versus time (logarithmic scale).

3.2. Device recovery under PBT stress

PBT stress was performed after the first NBT stress, which biases device with a positive gate voltage whose absolute value equals to that of NBT stress. Figure 3 shows the device parameters recovery induced by PBT stress versus time. Device parameters make a quick recovery at the initial stages: $V_{th}, G_{mmax}, I_{dsat}$ and I_{dlin} restore 93.6%, 92.5%, 80.7% and 78.1% respectively. V_{th} shows the most recovery.

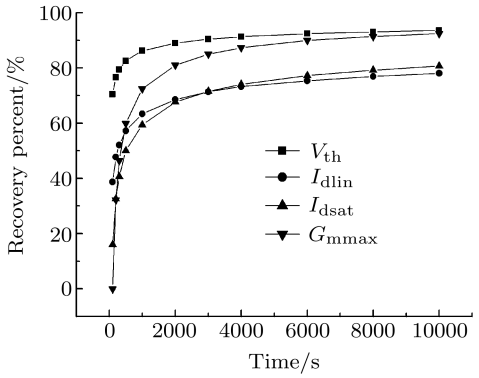


Fig.3. Device parameters recovery induced by PBT stress versus time.

3.3. Device degradation after the second NBT stress

The second NBT stress was applied on PMOSFETs after the PBT stress. Similar to the actual alternating current (AC) working conditions, the typical electrical parameters $I_{dsat}, I_{dlin}, G_{mmax}$ and V_{th} degrade greatly, as shown in Fig.4.

All the parameters shift after the first NBT stress, which restore in some different extent after PBT stress. When we bias the device in the second NBT stress, these parameters degrade greatly in comparison to the first NBT stress. Attention must be paid to the case that I_{dlin} get the worst degradation after the second NBT stress instead of the worst V_{th} degradation after the first NBT stress.

Figure 5 shows PMOSFET parameter degradation versus time after the second NBT stress. V_{th} shows the worst degradation at the initial time, I_{dlin} degradation exceeds V_{th} and is in the ascendant at later time. I_{dlin} shift reaches 31.7% after 10000 seconds, in comparison to the V_{th}, G_{mmax} and I_{dsat} shifts. The typical parameter shifts after NBT–PBT–NBT alternate stress is shown in Table 1.

Table 1. Typical parameter shifts after NBT–PBT–NBT stress.

	V_{th} shift/%	I_{dlin} shift/%	I_{dsat} shift/%	G_{mmax} shift/%
first NBT stress	8.1	3.2	4.6	2.3
PBT stress	93.6	78.1	80.7	92.5
second NBT stress	13.7	31.7	8.3	18.3

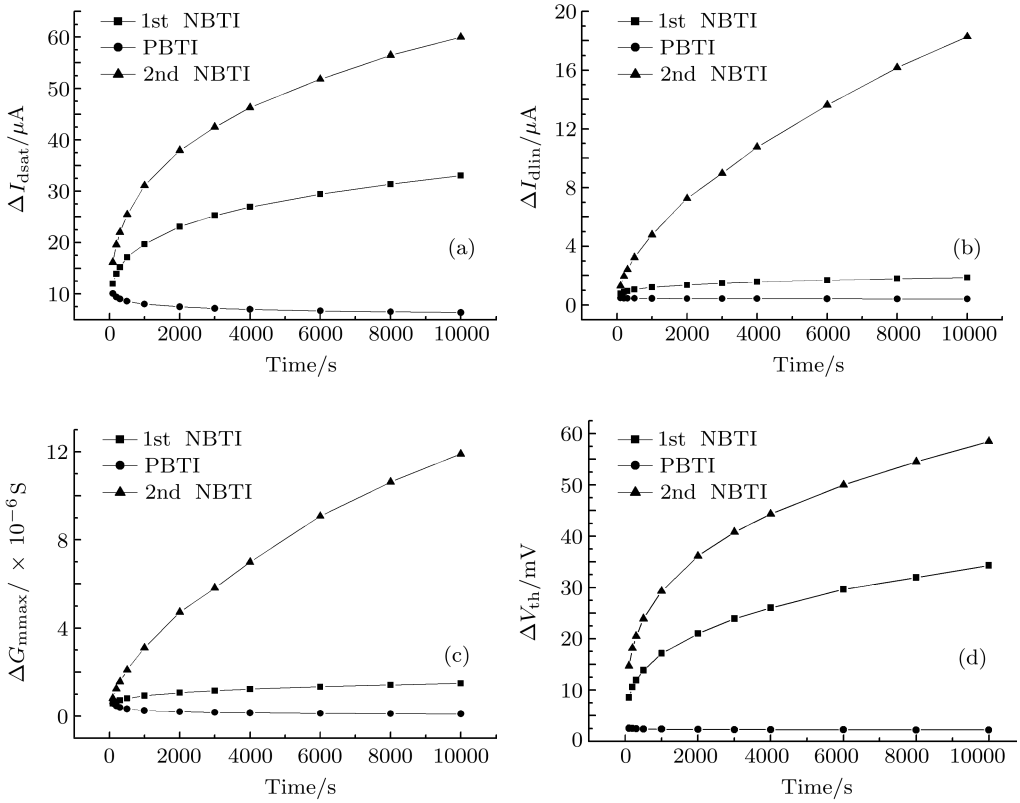


Fig.4. Device parameters degradation induced by NBT–PBT–NBT stress versus time. (a) ΔI_{dsat} versus time, (b) ΔI_{dlin} versus time, (c) G_{mmax} versus time, (d) V_{th} versus time.

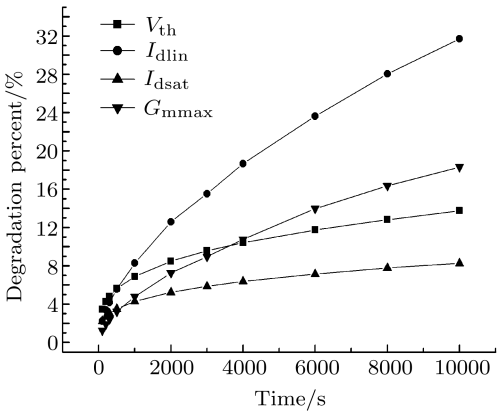


Fig.5. Device parameter degradation after the second NBT stress versus time.

3.4. Physical mechanism

In general, the diffusion species generated at the Si-substrate/oxide interface can migrate into oxide stack or silicon substrate, but in most reports only the direction towards gate oxide is considered.[8−10] Chakravarthi S *et al*[11] compared the two-sided and one-sided diffusion process by numerical simulations, and they found that the two cases predict identical time dependence. For mobile species generated at the Si-substrate/oxide interface, they can migrate towards gate oxide and Si-substrate direction. Threshold voltage can be simply expressed as the following:

$$V_{\rm th} = V_{\rm fb} - 2\phi_{\rm f} - |Q_{\rm B}|/C_{\rm ox}. \tag{1}$$

Where
$\phi_{\rm f} = (kT/q)\ln(N_{\rm D}/n_{\rm i})$, $|Q_{\rm B}| = (4qK_{\rm S}\varepsilon_0\phi_{\rm F}N_{\rm D})^{1/2}$ and $C_{\rm ox}$ is the oxide capacitance per unit area. The flatband voltage $V_{\rm fb}$ is given by

$$V_{\rm fb} = \phi_{\rm ms} - \frac{Q_{\rm f}}{C_{\rm ox}} - \frac{Q_{\rm it}(\phi_{\rm s})}{C_{\rm ox}}. \tag{2}$$

Where $Q_{\rm f}$ is the fixed charge density, $Q_{\rm it}$ is the interface trap density, $\Phi_{\rm ms}$ is the work function. It is always assumed that neither substrate doping density $N_{\rm D}$ nor oxide thickness varies with NBT stress. Only the change of $Q_{\rm f}$ and $Q_{\rm it}$ can cause $V_{\rm th}$ shift. From Eqs.(1) and (2) we obtain the simple $V_{\rm th}$ shift expression.

$$\Delta V_{\rm th} = -\frac{Q_{\rm it} + Q_{\rm f}}{C_{\rm ox}}. \tag{3}$$

It is the formation of positive fixed oxide charges and donor interface states that causes $V_{\rm th}$ degradation greatly.

$I_{\rm dsat}$ and $I_{\rm dlin}$ can be expressed as follows:

$$I_{\rm dsat} = -\mu C_{\rm ox}\frac{W}{2L}(V_{\rm gs} - V_{\rm th})^2, \tag{4}$$

$$I_{\rm dlin} = -\mu C_{\rm ox}\frac{W}{2L}\left[(V_{\rm gs} - V_{\rm th})V_{\rm ds} - \frac{V_{\rm ds}^2}{2}\right]. \tag{5}$$

Where, μ is mobility, W and L is the channel width and length respectively, $V_{\rm g}$ and $V_{\rm ds}$ is the gate voltage and drain voltage respectively. It can be seen that mobility μ has the influence on the drain current except for $V_{\rm th}$. The interface traps are generated during NBT stress, which increase the surface scatter and make mobility degrade. $G_{\rm m}$ has the similar expression as drain current, it is also influenced by the interface traps. The mechanism of NBTI can be expressed according to the reaction and diffusion model

$$\mathrm{Si_3 - Si - H} \rightarrow \mathrm{Si_3 - Si^0 + X_{interface}}, \tag{6}$$

$$\mathrm{X_{interface}} \rightarrow \mathrm{X^+_{bulk}} \tag{7}$$

where $\mathrm{Si_3}$–$\mathrm{Si^0}$ stands for the interface traps, and X is related to the hydrogen species. First, the interface traps $\mathrm{Si_3}$–$\mathrm{Si^0}$ are generated near the Si–$\mathrm{SiO_2}$ interface. $\mathrm{X_{interface}}$ is the reaction production, it diffuses towards the gate and forms the oxide positive charges in the oxide bulk. These interface traps and oxide positive charges make negative $V_{\rm th}$ shift and $I_{\rm dsat}$, $I_{\rm dlin}$, $G_{\rm m}$ degrade after the first NBT stress.

Reaction–diffusion model can explain the NBT degradation in general, it can not give an explanation of above NBT–PBT–NBT experimental phenomena. Based on the experimental results, great $V_{\rm th}$ shift is due to generation of interface states and oxide positive charges after the first NBT stress, which agrees with the model.

It is well known that $V_{\rm th}$ is very sensitive to the positive fixed charges. After a quick PBT stress, most holes are detrapped in a short time, which makes the recovery of $V_{\rm th}$ greater than that of other parameters. When we applied the second NBT stress, $I_{\rm dlin}$ gets the worst shift after the second NBT stress. It indicates that μ degradation is in the ascendant, which is mainly caused by the interface states. So, we concluded that much more interface traps are generated during the second NBT stress.

The second NBT stress results in greater degradation for all the parameters than the first NBT stress. These more severe parameter shifts result from the wear out of silicon substrate and oxide interface during the first NBT and PBT stress due to carriers trapping/detrapping and hydrogen related species diffusion, which make the Si–H bond become weak. It is

much easy for the generation of interface states during the second NBT stress.

The degradation process after NBT–PBT–NBT stress is shown in Fig.6.

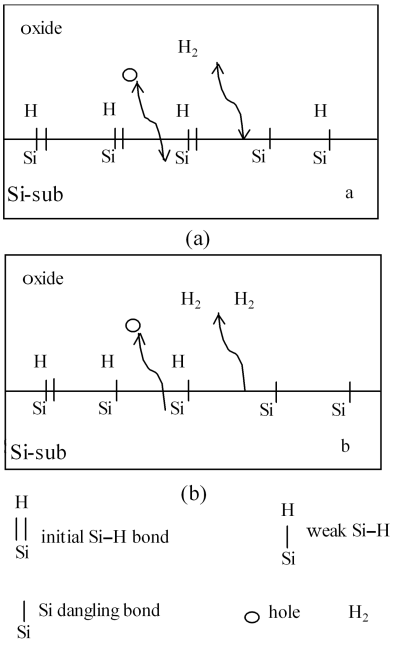


Fig.6. Degradation process after NBT–PBT–NBT stress.

Figure 6(a) shows that hydrogen diffuses in the direction kept away from the $Si–SiO_2$ interface, holes are trapped in the gate oxide. When PBT stress is applied, holes are detrapped because of the opposite electric field, which also make the unbroken Si–H bonds weaker. On the other hand, hydrogen density decreases at $Si–SiO_2$ interface because of stop of the positive chemical reaction, some hydrogen atoms diffuse towards $Si–SiO_2$ interface again, and passivate a part of dangling bonds. For the followed NBT stress, Fig.6(b) shows that the weaker Si–H bonds take part in the NBT reaction and generate much more interface states, so the parameter bears the worse degradation in comparison with the first NBT stress.

4. Conclusion

This paper investigates degradation characteristics of PMOSFETs under NBT–PBT–NBT stress. Threshold voltage has the largest shift under the first NBT stress condition. A fraction of NBT induced degradation can be recovered by the followed PBT process, which can benefit to improve the device lifetime under alternating current operation and also contribute for us to understand the mechanism of NBTI. The second NBT stress results in linear drain current to degrade greatly, a detailed explanation is presented in this paper.

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