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Electrical and optical characteristics of vanadium in 4H-SiC*

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A semi-insulating layer is obtained in n-type 4H-SiC by vanadium-ion implantation. A little higher resistivity is obtained by increasing the annealing temperature from 1450 to 1650 °C. The resistivity at room temperature is as high as $7.6 \times 10^6\,\Omega\cdot$cm. Significant redistribution of vanadium is not observed even after 1650 °C annealing. Temperature-dependent resistivity and optical absorption of V-implanted samples are measured. The activation energy of vanadium acceptor level is observed to be at about $E_C - 1.1$ eV.

Keywords: semi-insulating 4H-SiC, vanadium ion implantation, annealing, activation energy
PACC: 6170T, 6170W, 7155

1. Introduction

Semi-insulating SiC substrates are required for high-power, high-frequency SiC and GaN devices because of their low dielectric losses in the GHz range.[1] Semi-insulating regions can also be applied to device isolation or junction termination which is an important element of integrated circuit fabrication.[2] As a result of contamination, nominally undoped SiC crystals are conducting due to electrically active incorporation of either nitrogen donors or boron acceptors. Semi-insulating behaviour at room temperature is achieved in SiC by intentionally doping with vanadium.[3–5] Due to numerous studies using electron paramagnetic resonance (EPR),[6] photo-EPR,[7] deep level transient spectroscopy (DLTS),[8] photoluminescence (PL),[9] and optical absorption,[10] vanadium is currently the best understood to be used as a deep level impurity in SiC, and found to be able to substitute for silicon sites and act as amphoteric dopant in SiC. Vanadium exists in three possible charge states in SiC: positive ($3d^0$), neutral ($3d^1$), and negative ($3d^2$), and therefore produces two levels within the SiC band gap. Vanadium acts as a donor (V^{4+} ($3d^1$) / V^{5+} ($3d^0$)) in p-type SiC and an acceptor (V^{4+} ($3d^1$) / V^{3+} ($3d^2$)) in n-type SiC.

There is a consensus that the vanadium donor level resides near the middle of the band gap in p-type 4H-SiC, at approximately 1.6 eV below the conduction band.[5,11] The acceptor level is closer to the conduction band, but its location has not yet been unambiguously determined. Several studies indicate that the acceptor level is 0.8 eV below the conduction band.[11,12] In recent years, more and more papers report 1.1 eV of the vanadium acceptor level.[5,13] Post-implantation annealing is performed to repair the lattice damage and activate the dopant. But there has been no paper reporting on the stability of V atoms in SiC so far.

In this paper, we report on the fabrication and characteristics of semi-insulating layer in n-type 4H-SiC by vanadium ion implantation. Ion range distribution is obtained by Monte Carlo simulations using the TRIM program. Resistivity is measured in different annealing conditions. The study about the detailed redistribution of V atoms in SiC during annealing is discussed. Temperature-dependent resistivities of V-implanted samples up to 580 K are measured to determine the activation energy of vanadium acceptor level. To verify the energy representing the vanadium acceptor level we also perform optical absorption measurements in the near infrared region.

2. Experiment

The starting material used for V implantation is a 4.9 μm thick n-type ($N_d = 5.2 \times 10^{15}\,\mathrm{cm}^{-3}$)

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4H-SiC epitaxial layer grown on a Si face, 8° off-axis, (0001)-oriented n-type 4H-SiC substrate from Cree Research, Inc. The resistivity of the substrate is about $0.015\,\Omega\cdot$cm. V ions are implanted with a $1.4\times10^{13}\,\mathrm{cm}^{-2}$ dose at 2.1 MeV. Post-implantation annealing is performed in argon atmosphere at 1450 and 1650 °C for 30 min. To minimize Si evaporation from the sample surface during annealing, the samples are encased in a SiC-coated graphite crucible. The wafers are cut into 1.0 cm × 1.0 cm pieces for optical absorption studies and current–voltage measurements. Unimplanted samples are also prepared for a reference.

Samples are processed into mesa structure with a 300 μm diameter by reactive ion etching with CF_4 and O_2 gases, and surfaces are passivated with thermal oxides to reduce the leakage current during current–voltage measurements. Figure 1 shows the schematic cross section of the sample. Ohmic contacts are formed by depositing 350 nm thick Ni on the top- and back-sides. The contacts are annealed at 1050°C for 10 min in forming gas. Finally, Ti/Au contacts are deposited on the top- and back-sides.

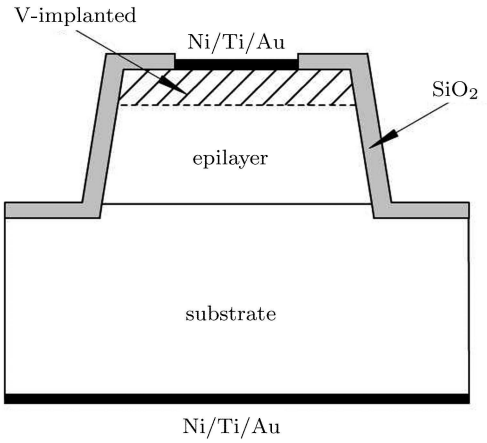


Fig.1. Test structure for V-implanted 4H-SiC sample.

Absorption measurements are performed with the Bruker IFS-120HR FTIR spectrometer, equipped with a tungsten quartz-halogen source, a quartz beam splitter, and an InGaAs detector. The sample is cooled in a continuous flow helium cryostat allowing temperatures to reduce down to 12 K.

Secondary ion mass spectrometry (SIMS) is used to verify the actual dopant distribution after implantation and to explore any possible redistribution after high temperature processing. Depth profiles of the V-implanted SiC samples are obtained by SIMS using a CAMECA-ims-4f instrument with a 10.5 keV O_2^+ primary ion beam. The primary beam current of 1 μA is focused and rastered over an area of 250 μm ×250 μm. The secondary ion signal is extracted from a circular area of 60 μm in diameter centred in the rastered region. The depth is determined by measuring the total crater depth with a surface profiler and assuming a constant sputtering rate during depth profiling. The concentration is determined by assuming that the stated nominal implantation fluence is correct.

3. Results and discussion

The location of peak concentration and the longitudinal straggling of V are computed with the Monte Carlo simulator TRIM. Figure 2 shows the profile of V-ion implantation using the Gaussian model for expressing the V-ion implantation range.

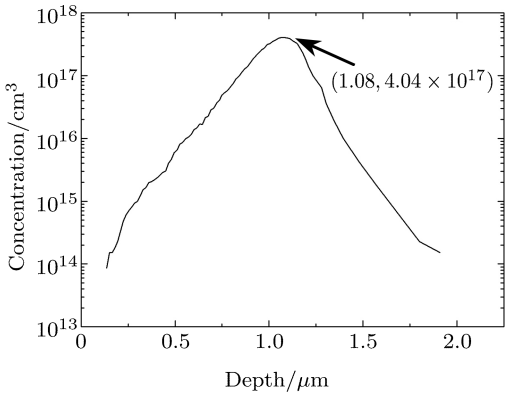


Fig.2. Simulated ion implantation profile for 2.1 MeV V-implanted n-type 4H-SiC.

Low-resistance ohmic contacts are very difficult to fabricate on high-resistivity samples. In this work, most implanted vanadium atoms are located at the deep positions from the surface of sample due to high energy (2.1 MeV) implantation. As a result, a higher free-carrier concentration is attained in the surface region due to lack of compensation. Ohmic contacts are typically formed by the deposition of transition metals on SiC, followed by high-temperature annealing.[14] It has been proved that ohmic contacts are achieved by depositing Ni on n-type 4H-SiC.[15] The specific contact resistance ρ_c as low as $10^{-3}\,\Omega\cdot\mathrm{cm}^2$ is obtained even for Ni contact on n-type 4H-SiC with a low doping concentration.[16] Compared with the high resistivity of V-implanted layer, the contact resistance can be neglected during current–voltage measurements.

The current–voltage measurements are performed with an HP4156B semiconductor parameter analyser. Typical current–voltage characteristics measured from the top circular contact to the bottom blanket contact are shown in Fig.3 for V-implanted and unimplanted samples at room temperature. Neglecting the relatively small resistance of the substrate, $R =$ voltage/current is approximately equal to the resistance of the compensated region. The resistivity of the implanted layer is calculated using the formula $\rho = RA/W$, where A is the cross-sectional area of the top circular metal pad, and W is the thickness of the implanted layer, and it is estimated from TRIM range statistics to be $R_{\mathrm{p}} + 2\Delta R_{\mathrm{p}}$ of the deepest implantation.

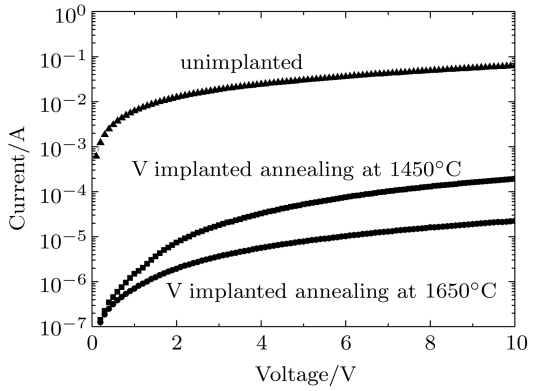


Fig.3. Current–voltage characteristics for V-implanted n-type 4H-SiC samples at room temperature. The characteristic of unimplanted sample is also shown for comparison.

The resistivity of unimplanted sample is $800\,\Omega$·cm. V-implanted samples exhibit much lower current than virgin samples. The V-implanted layers in n-type 4H-SiC are semi-insulating with a resistivity of $7.6 \times 10^6\,\Omega \cdot \mathrm{cm}$ when annealed at 1650 °C. A little higher resistivity is obtained by increasing the annealing temperature from 1450 to 1650 °C, which can be explained in terms of high-temperature activation. Implantation causes lattice damage mainly consisting of point defects such as vacancies and interstitials.[17] Post-implantation annealing can be used to repair ion-induced lattice damage and electrically activate dopants. Higher resistivity is obtained due to more V-atoms activated for compensation by increasing annealing temperature from 1450 to 1650 °C.

Implanted SiC sample is subjected to high-temperature annealing which can result in the excellent activation of the dopants. However, the high-temperature annealing may lead to the redistribution of dopants in SiC especially for light atoms such as beryllium atoms.[18] The SIMS depth profiles of V-implanted layers before and after annealing are shown in Fig.4. Significant redistribution is not observed even after 1650 °C annealing. The V atoms do not show a significant in-diffusion behaviour but show relatively low out-diffusion rate after annealing at 1450 and 1650 °C. The slight shift of the peak of the implanted V-atoms concentration towards the surface can be seen. However, the depletion of V-atoms in the surface region is not observed. The depletion of V atoms in the surface region due to the out-diffusion is not desirable because it results in low resistivity for lack of compensation. If this occurs, achieving better inter-device isolation in semi-insulating SiC will not be possible.

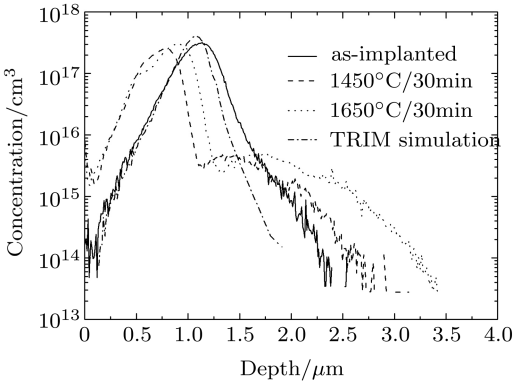


Fig.4. SIMS depth profiles in 4H-SiC epilayers before and after annealing. A simulated depth profile obtained by TRIM is also shown for comparison.

Temperature-dependent resistivity measurements are performed on V-implanted samples at up to 580 K. The resistivity as a function of reciprocal temperature is plotted in Fig.5. The resistivity decreases slightly at lower temperatures, then falls sharply by nearly two orders at higher temperatures. The resistivity versus reciprocal temperature is a straight line in the range from 470 to 580 K suggesting that one deep level dominates the sample. The variation of resistivity with temperature can be explained as follows. Most of the free electrons are captured by the vanadium acceptor level at lower temperatures. The vanadium acceptor level releases some of the previously trapped electrons back to the conduction band at higher temperatures. This produces a rapid decrease in resistivity with temperature increasing.

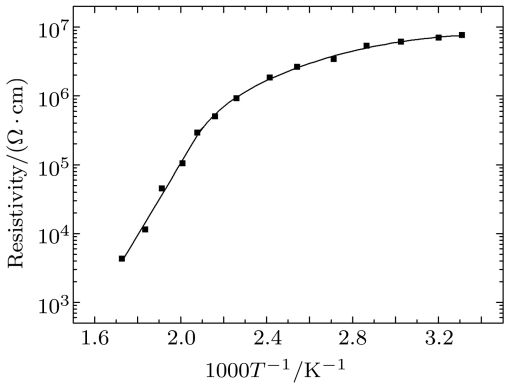


Fig.5. Temperature-dependent resistivity for V-implanted n-type 4H-SiC.

The activation energy E_a is determined from the Arrhenius relationship between temperature and resistivity as follows:

$$\rho = A\mathrm{e}^{E_\mathrm{a}/kT}, \tag{1}$$

where ρ is the resistivity of the sample, k is the Boltzmann constant, and T is the temperature. The activation energy of the V acceptor level is calculated, from the slope of the line fitted to Arrhenius plots of $\ln(\rho)$ versus $1/kT$ in the range from 470 to 580 K, to be 1.08 eV. Zvanut found 1.1 eV of vanadium acceptor level in n-type 4H-SiC by the photo-EPR measurements.[13] This experiment supports the fact that implanted V atoms are electrically active and play an important role in forming the semi-insulating layer.

Figure 6 presents the near-infrared absorption spectra of two 4H-SiC samples. The lower spectrum is observed during examining an unimplanted sample, whereas the upper spectrum is from a V-implanted sample. An absorption line located at $E_\mathrm{c} - 0.97\,\mathrm{eV}$ is observed in the V-implanted sample. This is not seen in the n-type sample. This can be explained as follows. Vanadium is present in its neutral ($3\mathrm{d}^1$) charge state by ion implantation. Most electrons in n-type 4H-SiC are captured by vanadium impurity. This leads to the neutral-to-negative transition of vanadium. Figure 7 shows how such a compensation process can occur. Shown are the band edges of SiC and two major levels: the nitrogen donor level located at $E_\mathrm{c} - 0.1\,\mathrm{eV}$ and the vanadium acceptor level at $E_\mathrm{c} - 0.97\,\mathrm{eV}$. Because the vanadium concentration is higher than that of uncompensated nitrogen, the electrons will be captured by vanadium acceptor level. The Fermi level is pinned near the $\mathrm{V}^{3+}/\mathrm{V}^{4+}$ level. During the near-infrared absorption measurements, the captured electrons are emitted from the vanadium acceptor level back to the conduction band. Thus we conclude that the activation energy at $E_\mathrm{c} - 0.97\,\mathrm{eV}$ is related to the vanadium acceptor level. The energy is similar to the value obtained by temperature-dependent resistivity measurements discussed above.

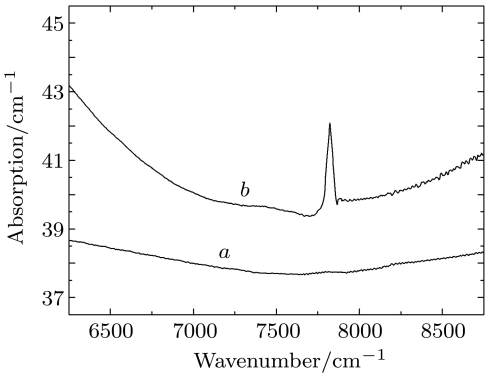


Fig.6. Near-infrared absorption spectra obtained from unimplanted (curve *a*) and from V-implanted (curve *b*) 4H-SiC sample.

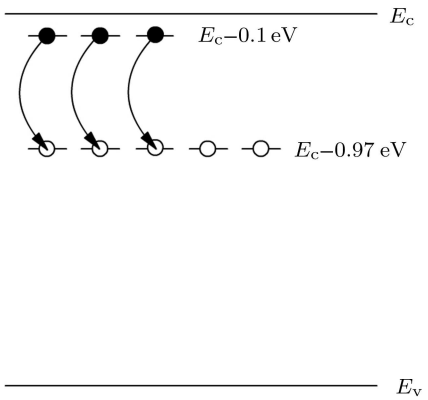


Fig.7. Schematic diagram of compensation in V-implanted n-type 4H-SiC samples.

4. Conclusions

Vanadium-ion implantation has been shown to be effective for creating semi-insulating 4H-SiC layer. A little higher resistivity is obtained by increasing the annealing temperature from 1450 to 1650 °C. The resistivity of V-implanted layer is as high as $7.6 \times 10^6\,\Omega\cdot$cm at room temperature. The V atom profiles measured by SIMS show little redistribution after high-temperature annealing at 1450 and 1650 °C. The depletion of V in the surface region due to the

out-diffusion is not observed even after 1650 °C annealing. The resistivity decreases with increasing temperature. Owing to the compensation process gradually influenced by the ambient temperature, the resultant activation energy changes with the temperature. Temperature-dependent resistivity measurements indicate that the vanadium acceptor level resides at 1.08 eV below the conduction band. A similar level has also been observed by measuring the optical absorption.

Acknowledgments

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