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Polymer thin-film transistor based on a high dielectric constant gate insulator*

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In this paper full polymer thin-film transistors (PTFTs) based on Poly (acrylonitrile) (PAN) as the gate dielectric and poly (2-methoxy-5-(2'-ethyl-hexyloxy)-1,4-phenylene-vinylene) (MEH-PPV) as the semiconductor layer were investigated by using different channel width/length ratios. Relatively high dielectric constant of the polymer dielectric layer (6.27) can remarkably reduce the threshold voltage of the transistors to below −3 V. Hole field-effect mobility of MEH-PPV of the PTFTs was about 4.8×10^{-4}cm^2/Vs, and on/off current ratio was larger than 10^2, which was comparable with that of transistors with widely used Poly (4-vinyl phenol) (PVP) or SiO_2 as gate dielectrics.

Keywords: Polymer, Dielectric, Field effect transistor, Field-effect mobility
PACC: 7340Q, 7360, 8160J

1. Introduction

During the past few years, the performances of organic thin-film transistors (OTFT) have been improved drastically. To date, the mobility of OTFTs with vacuum-deposited pentacene films at room temperature reached as high as 2.7 cm^2/Vs, and the on/off current ratio was larger than 10^6, which was close to that of amorphous silicon thin-film transistor (TFT).[1,2] The results would lead to commercial applications in flat-panel displays,[3] smart cards, electronically identification tags and sensing devices.[4] However, the OTFTs based on pentacene were suspected in relation to stability due to the ease of recrystallizing.

For OTFTs which are targeting a wide range of potentially inexpensive applications, polymer based TFTs (PTFTs) with solution processing seem better suited for the purpose. Solution-processable polymer gate dielectrics and active semiconducting layers can be deposited by spin coating, spray coating or printing rather than by vacuum deposition. So they can be competitive for novel TFT applications to meet the requirements of large area, flexibility, low-temperature processing and especially low-cost. In the last few years, mobilities up to 0.1 cm^2/Vs have been demonstrated by using active layers of soluble regioregular poly (3-alkylthiophene),[5] poly (9,9-dioctylfluoren-bithiophene)[6] or pentacene from soluble precursors.[7]

However, the best electrical performance for OTFTs has been obtained by employing high quality inorganic dielectrics such as ion-beam sputtered SiO_2[8] chemical vapour deposition silicon nitride,[9] or silicon dioxide thermally grown on single-crystalline silicon[10] etc. For low cost, full organic or full polymer devices are necessary. So recently, polymer gate dielectrics like polyimide,[11,12] poly (vinyl phenol) (PVP),[13] poly (vinyl alcohol),[14] and poly(vinylcabonate) have tended to replace the established conventional inorganic dielectrics.

In this work, MEH-PPV-based TFTs with a relative high dielectric constant polymer insulating layer (Poly (acrylonitrile) (PAN)) were fabricated.[15] Hole carrier mobility of 4.8×10^{-4} cm^2/Vs and threshold voltage of −2.98 V have been obtained, which were comparable with the reported hole carrier mobility of 1.8×10^{-4} cm^2/Vs and threshold of −4.0 V with inor-

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ganic dielectric.[16] These results show that polymer gate dielectrics not only provide low-cost fabrication methods, but also may produce similar or better electrical performances.

2. Experimental

The structure of PTFT is shown in Fig.1, which was fabricated in inverted staggered configuration. During the processing, the gate electrode of indium tin oxide (ITO, 110 nm-thick) was first thermally deposited on a glass substrate, then patterned by photolithography. The thickness of the ITO was measured by the surface profile (TENCOR Alfa step-500). The output characteristics were measured under nitrogen atmosphere by means of a Keithley 2400 and a computer-controlled source meter (Keithley 236 source-measure units), which controlled the gate voltage and drain voltage respectively.

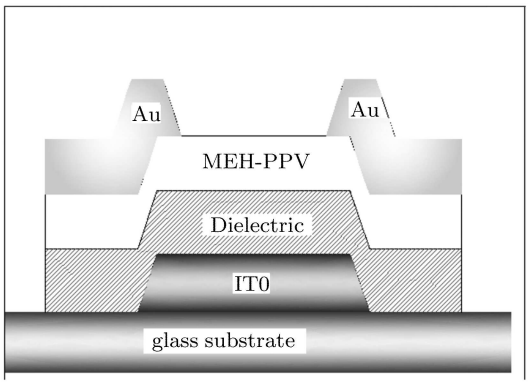
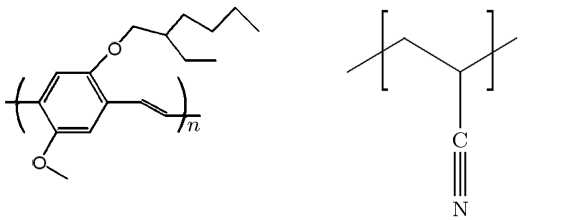


Fig.1. Schematic structures of OTFT.



MEH-PPV Poly (acrylonitrile) (PAN)

Fig.2. Chemical structures of PAN gate insulator and MEH-PPV active layer.

The gate dielectric layers (chemical structures shown in Fig.2) were deposited on the ITO gate electrode by a spin coating method under ambient condition. Insulator PAN was spin-coated from a solution of N, N-Dimethylformamide and dried under N_2 atmosphere at 90°C for 20 hours. The thickness of PAN film was 400 nm. The active layer of MEH-PPV was obtained by spinning from a 0.36 wt% mixing solution of THF (tetrahydrofuran) and xylene (THF: xylene =1:1) under N_2 atmosphere followed by an annealing at a temperature of 70°C for 1 hour. The average thickness of MEH-PPV film was about 60 nm.

On top of the active layer a gold layer of 50 nm thick was thermally deposited under vacuum condition through a shadow mask to form source and drain electrodes. The channel was formed with an inter-digital structure, as shown in Fig.3. Two transistors with channel width/length ratios of 100 and 1000 respectively were fabricated for comparison.

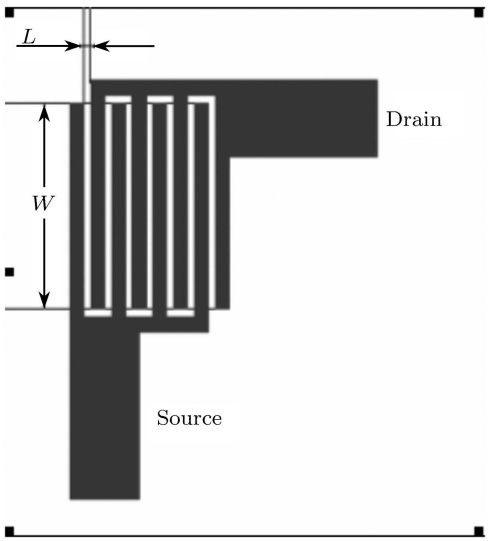


Fig.3. Inter-digital source and drain structure of MEH-PPV transistor.

Normally, OTFTs as to drain–source contacts can be classified two configurations: top contact and bottom contact. The PTFTs investigated here were top contact. Because the field-induced carrier are confined to a very thin layer close to the interface of insulator and the active layer, top drain–source contacts avoid the morphological defects of the active layer due to the influences of source/drain electrodes.[17] In addition, for metal Au, the barrier height for hole injection is only about 0.5 eV. It was proposed that the contacts between the semiconductor MEH-PPV and drain/source Au electrodes were ohmic. The capacitances of the devices were measured by Hewlett Packard 4192 impedance analyser.

3. Results and discussion

3.1. Dielectric properties

The morphology of the deposited dielectric layer can affect the semiconducting layer and hence significantly influence the PTFTs's properties. Figure 4 shows the polarizing microscope pictures of PAN dielectric layer, exhibiting uniform and few defects on the surface of PAN film.

In order to analyse the dielectric properties, a capacitor with metal–insulator–metal (MIM) structure was made. The capacitance was about $1.39 \times 10^{-4}\mathrm{F/m^2}$ at the range of 10 kHz to 1 MHz. According to the capacitance data, the PAN gate dielectric constant was calculated to be 6.27, which was higher than that of the cross-linked PVP ($\varepsilon = 5$)[18] and SiO_2. The field-induced carriers were confined in a thin film close to the interface between MEH-PPV and insulating layer. The number of the field-induced carriers per unit area in the channel was calculated by the formula $N_C = \dfrac{k\varepsilon_0}{ed}V_{GS}$, where $(k\varepsilon_0)$ is the dielectric constant of the gate insulator, e the electron charge. Low threshold voltage could be expected in the OTFT with high dielectric constant gate insulator since there are enough charges to fill the traps in the active layer at a low gate voltage.

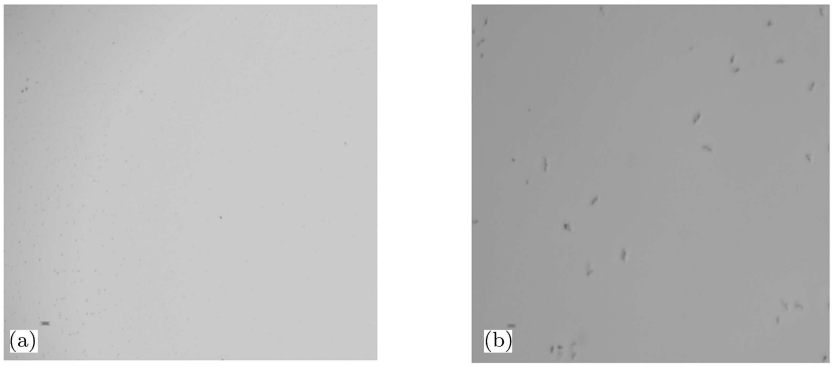


Fig.4. Polarizing microscope (PM) pictures of the dielectric layer. (a) ×10; (b) ×50.

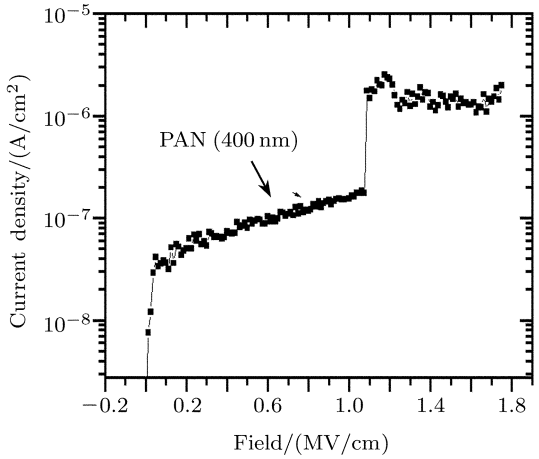


Fig.5. Leakage current as a function of the applied electric field for PAN film.

Another important characteristic about polymer gate dielectric is the leakage current. Figure 5 shows the leakage current as a function of the applied field. The average gate dielectric leakage for PAN is $5.53 \times 10^{-8}\,\mathrm{A/cm^2}$ at 0.5 MV/cm, which is similar to the leakage currents observed in the transistor with cross-linked PVP and thermally grown SiO_2 insulators.[19] The breakdown electric field is about ∼1.1 MV/cm.

3.2. PTFTs characterizations

Figures 6(a) and (b) illustrate the typical I-V curves for a p-channel device operating in the accumulation mode, including the drain currents I_{DS} versus drain voltages V_{DS} at different gate voltages, V_{GS}. Both of the two transistors exhibit typical saturation behaviour.

Figures 6(c) and (d) show the transfer characteristics of different channel width/length ratios. The drain–source voltages remain constant at −30 V and −40 V respectively to keep the devices operating in the saturation range. There is only a small difference in the threshold voltage between the two transistors. But the currents at the same drain and gate voltage differ from each other essentially because of the different channel width/length ratio. The insets of Figs.6(a) and (b) illustrate the linear current–voltage characteristics at source–drain voltages (V_{DS}) lower than gate voltages (V_{GS}).

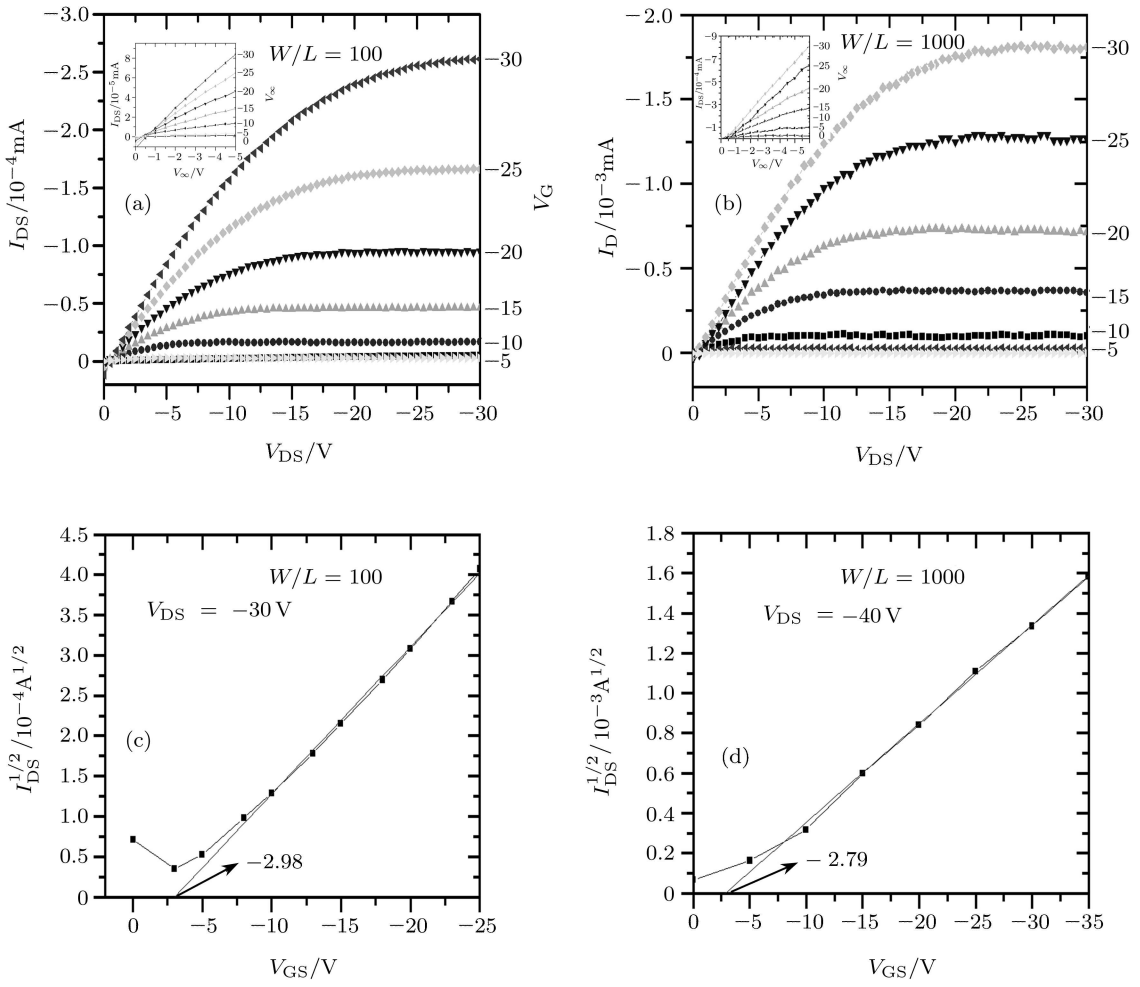


Fig.6. Output characteristics of MEH-PPV PTFT using poly(acrylonitrile) as the insulating layer with different channel width/length ratios (a), (b). Analyses of the saturation regime transfer characteristics ($I_{DS}^{1/2}$ versus V_{GS}) (c), (d), keeping drain–source voltages at −30 V and −40 V respectively. The insets of Figs.6(a) and (b) are the linear current–voltage characteristics at source–drain voltage V_{DS} lower than gate voltages V_{GS}.

From the output characteristics of an OTFT, The drain current is a function of the applied voltage V_{GS} and V_{DS}:[20]

$$I_D = \begin{cases} \dfrac{W}{L}\mu C_i(V_{GS} - V_T)\cdot V_{DS}, & V_{DS} \le V_{GS} - V_T, \quad (1) \\ \dfrac{W}{L}\mu C_i\dfrac{(V_{GS} - V_T)^2}{2}, & V_{DS} \ge V_{GS} - V_T. \quad (2) \end{cases}$$

where W and L are the channel width and length, C_i the capacitance per unit area of the insulator, V_T the threshold voltage, and μ the field-effect mobility of MEH-PPV. The mobility in the linear region is determined by the following equation:

$$\left(\frac{\partial}{\partial V_{GS}}\right)\left[\left(\frac{\partial I_D}{\partial V_{DS}}\right)\right] = \frac{WC_i}{L}\mu, \quad (3)$$

where $V_{GS} - V_T \le V_{DS} \le 0$.

The mobility in the saturated region and the threshold voltage can be obtained by plotting the saturated drain current in the form of $\sqrt{I_{Dsat}}$ vs. V_{GS} (shown in Figs.6(c), (d)). The mobility in the saturated region can be calculated from the slope of the straight line shown in Figs.6(c), (d) by using the following equation derived from Eq.(2)

$$\left(\frac{\partial\sqrt{I_{Dsat}}}{\partial V_{GS}}\right) = \frac{WC_i}{L}\mu. \quad (4)$$

The threshold voltage can be obtained from the interception of the straight line and the axis. It is noted that the square root of the saturation current does

not align along a straight line (Figs.6(c) and (d)), but tends upward at low gate voltage. It is probably for the reason that the charge mobility is assumed to be constant in the Eq.(2). In fact the mobility normally exhibited gate bias dependence and saturates at large gate bias.[21] The performances of the PTFTs with different channel width/length ratios are summarized in Table 1.

Table 1. Summary of the parameters of the PTFT with different width/length ratios.

Dielectric	Channel W/L ratio	Threshold voltage ($V_{\rm T}$)/V	Hole mobility (μ)/(cm^2/Vs)	$I_{\rm on}/I_{\rm off}$
poly (acrylonitrile)	100	−2.98	4.84×10^{-4}	1.33×10^2
poly (acrylonitrile)	1000	−2.79	3.50×10^{-5}	5.28×10^2

Table 1 clearly shows that the threshold voltage is not significantly dependent on the channel width/length ratios, but the mobilities of the two TFTs differed from each other significantly. The lower mobility of the PTFT with larger channel width/length ratio of 1000 is not understood well, probably due to the contact resistor predominated or larger leakage current. The on/off ratio is about 10^2, smaller than other report with on/off ratio of 10^3–10^4,[16] which is probably due to the impurity of the MEH-PPV. Further work on improving PTFT performances is undertaking.

4. Conclusions

MEH-PPV PTFTs with different channel width/length ratios were fabricated. An organic layer PAN is firstly used as the gate dielectric. The devices possess low leakage current and low threshold voltage. Typical I-V characteristics of the PTFT are observed. The hole mobility is $4.8\times10^{-4}\,\mathrm{cm}^2/\mathrm{Vs}$ and the threshold voltage $V_{\rm T}$ is below 3 V. The threshold voltage is almost independent on the channel width/length ratios. These results suggest that the use of polymer gate dielectric in fabrication of TFT can not only simplify the process and lower the cost, but also provide promising electric performances.

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